Ken Jennings

The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

TMM20000 SERIES ADD-IN MEMORY FOR PDP-11 COMPUTERS USER'S MANUAL

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REVISION B

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. INTRODUCTION

1.1 SCOPE

This document contains the information necessary to install and operate the Texas Instruments (TI) TMM20000 Series Add-In Memory modules. These boards are fully designed to be compatible with the PDP-11 Unibus* Computers, manufactured by Digital Equipment Corporation (DEC).

Onboard circuitry performs single bit error correction and error detection. Control (CSR) and error (ESR) status registers, with single and double bit error display capture in real time all information necessary to trace a single bit failure to the failing memory component. All error dection and correction operations are transparent to the operating system.

Battery backup is jumper selectable.

1.2 REFERENCE DOCUMENTS

PDP-11 Processor Handbook, Digital Equipment Corporation.

1.3 DOCUMENT CONTROL

Distribution of this user's manual is controlled by the Drafting Department of TI Integrated Memory Systems.

1.4 SPECIFICATIONS

1.4.1 Memory Capacity

MODEL NO.	TMM20000-01	256KW x 22 Bits (262,144 Words)
	TMM20000-02	128KW x 22 Bits (131,072 Words)
	TMM20000-03	96KW x 22 Bits (98,304 Words)
	TMM20000-04	512KW x 22 Bits (524,288 Words)
	TMM20000-05	64KW x 22 Bits (65,536 Words)

1.4.2 Memory Access and Cycle Times[1]

Memory

OPERATION		STATUS REGISTERS		MEMORY REGISTERS			
		ACCESS TIME (ns)		ACCESS TIME (ns)		CYCLE TIME (ns)	
		TYP	MAX	TYP	MAX	TYP	MAX
DATI	No error detected (see Note 2)		125	400	430	620	665
	Error detected (see Note 2)		125		540		965
DATO			125	40	60	620	665
DATOB			125	40	60	920	965

NOTES: 1. Access and cycle times are measured from receipt of Bus MSYN to transmission of Bus SSYN.
2. An error correction code extends access and cycle time when an error is detected and corrected.

* Trademark of Digital Equipment Corporation.

1.4.3 Power (Typical 256K words)

Timing is shown in Figure 1-1.

MODE	CONDITIONS	WATTS	NOTES
Operating	+5 V (±5%)	20	Continuous read/ write cycles.
Standby		12	Memory refresh every 15 μs.
Battery Backup	Standby	12	Memory array and refresh support circuits operating in standby modes.

1.4.4 Interface Requirements

The Unibus* enables a TMM20000 Add-In Memory Module to interface with a PDP-11 computer and other peripherals. Jumpered options permit the module to operate with either a Standard, Modified, or Extended Unibus*.

* Trademark of Digital Equipment Corporation

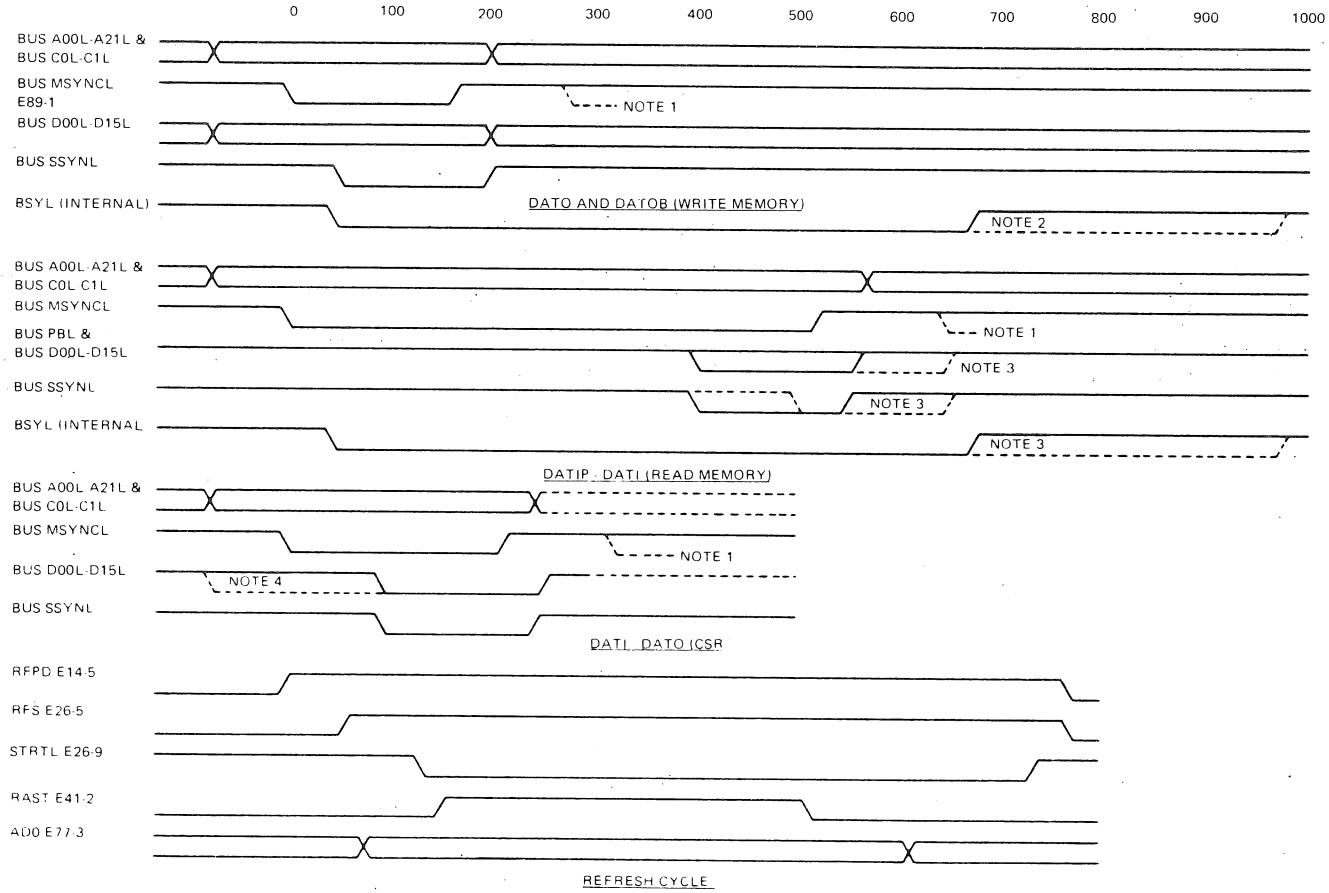


FIGURE 1-1 – TIMING DIAGRAM

NOTES:
1. MSYNCL may occur prior to BSYL in which case cycle will start when BSYL goes high.
2. BSYL will be extended 300 ns typical for byte write.
3. SSYN and DATA will be delayed 90 ns typical and BSYL will be delayed 300 ns typical on read with error. SSYN and data will be delayed up to 700 ns by refresh.
4. Solid line is for read and dashed line is for write.
5. Solid line is for read and dashed line is for write byte.

1.4.4.1 *Input Signals*

The signals required by the TMM20000 are:

A0 - A17	ADDRESS LINES
C0, C1	CONTROL LINES
MSYN	MASTER SYNC
INIT	INITIALIZE
DC LO	DC POWER OK
D0 - D15	DATA LINES
PB	PARITY DATA LINE
A18 - A21	EXTENDED ADDRESS LINES (EXTENDED UNIBUS ONLY)

Input characteristics are:

PARAMETER	CONDITIONS	SPECIFICATION
$V_{in}1$		+2.0 MIN
$V_{in}0$		+0.8 MAX
I_{in}	V_{CC} = 5 V	50 μA MAX
I_{in}	V_{CC} = 0 V	50 μA MAX

1.4.4.2 *Output Signals*

The signals generated by TMM20000 are:

D0 - D15	DATA LINES
PB	PARITY DATA LINE
SSYN	SLAVE SYNC
PB	PARITY ERROR FLAG (CSR OPTION)

Output characteristics are:

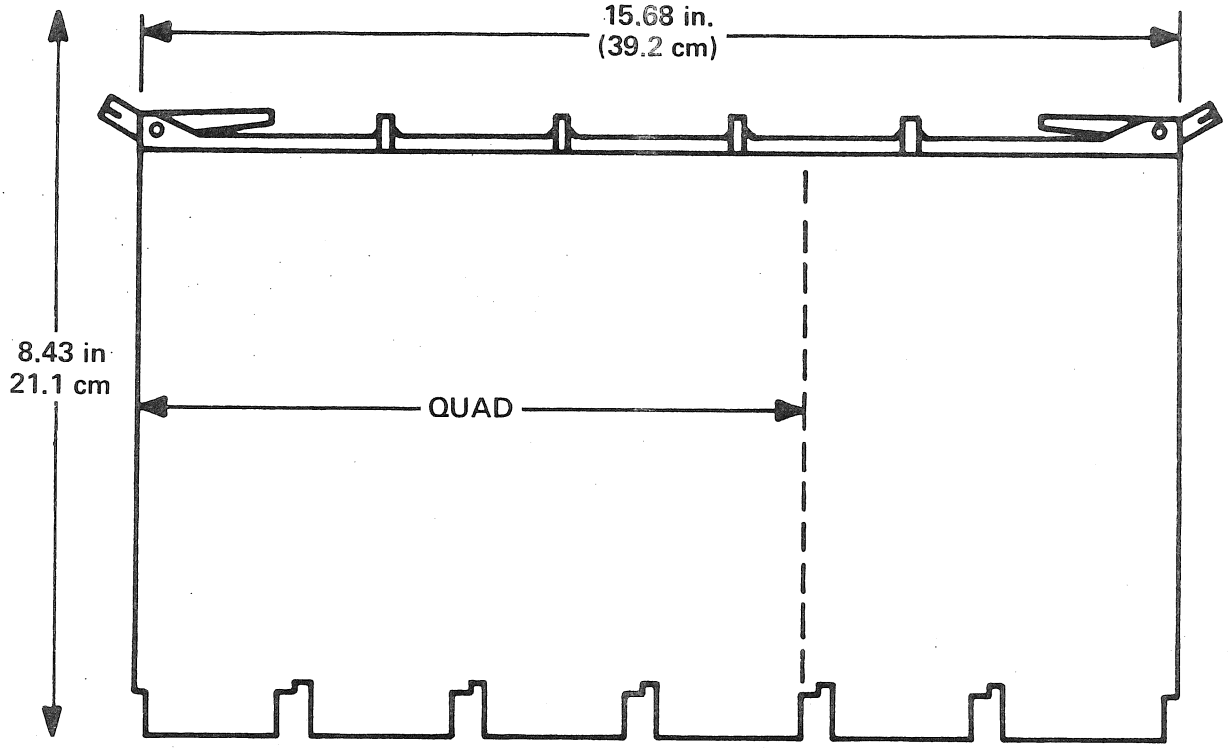
PARAMETERS	CONDITIONS	SPECIFICATION
V_{OL}	V_{CC} = MIN @ I_{OL} = 50 mA	.7 V MAX
I_{OH}	V_{CC} = MAX, V_{OH} = V_{CC}	150 μA MAX
	V_{IL} = 0.8 V MAX	

1.4.5 Environmental

	TEMPERATURE	RELATIVE HUMIDITY
Operating	5°C to 50°C	10% to 95%
Storage	–40°C to +85°C	Noncondensing

1.4.6 Dimensions (See Figure 1-2)

15.68 in. (39.2 cm) X 8.47 in. (21.0 cm), single width, hex height.



HEX
PDP-11 SERIES

FIGURE 1-2 – TMM20000 MODULE DIMENSIONS

2. FUNCTIONAL DESCRIPTION

2.1 NORMAL DEC SYSTEM OPERATION

The TMM20000 Add-In Memory module interrupts system operation when a double bit error occurs. A red LED on the card edge indicates the failing module. A double bit error is seen by the bus as a parity error and the PBL signal is enabled. When a single bit error occurs, TMM20000 corrects the error before putting data on the Unibus and rewrites the corrected data into the memory array.

2.2 CONTROL, EXTENDED CONTROL AND ERROR STATUS REGISTERS AND DISPLAY USAGE

The TMM20000 has three onboard registers; the control status register (CSR), the extended control status register (ECSR), and the error status register (ESR). The CSR and ECSR provide memory control and also store error information, as well as being used in memory diagnostic testing. The ESR provides information about the exact location of a failed memory device. The CSR and ECSR are fully compatible with the DEC M7850 parity module.

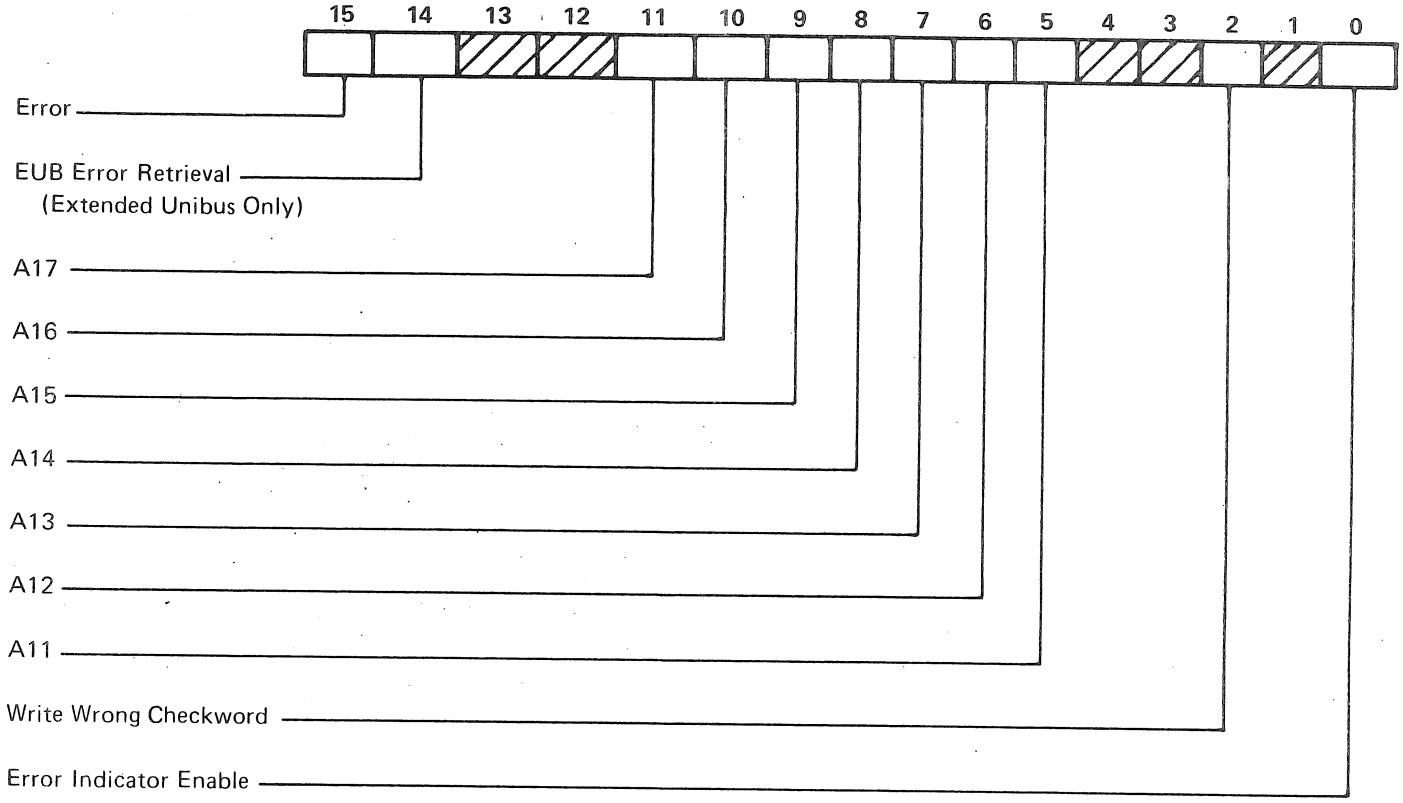
All three registers share a common address with the ECSR and ESR being addressed following a write operation to the CSR. The ECSR is accessed by first doing a write operation to the CSR address with Bit 14 set to a logic 1. The ESR is accessed by first doing a write byte operation to the lower byte of the CSR address.

An error status display is provided on the memory to show the presence of an error and to indicate the failed memory device.

The three registers and the error status display are described in the following paragraphs.

2.2.1 Control and Status Register (CSR) Usage Description (See Figure 2-1)

BIT	NAME		FUNCTION
15	Error	R/W	This bit is set to a one when an error occurs on a DATI or DATIP cycle. The user selects either double only or single and double error indication. Once set, it is reset by INIT or by writing a zero via a CSR write cycle.
14	Modified Unibus (jumper selected) Unused	R/O	Read as zeroes
	Extended Unibus (EUB) (jumper selected) EUB Error Retrieval	R/W	In normal operation, this bit is zero and when an error occurs, address bits A17-A11 are obtained from CSR bits 11-5 as in the Standard or Modified Unibus. If bit 14 is set to one (via a CSR write cycle) and Extended Unibus is jumper selected, then A21-A18 are obtained from CSR bits 8-5 (Paragraph 2.2.2). This bit is cleared by INIT or by a zero via a CSR write cycle.
13-12	Unused	R/O	Read as zeroes
11-5	Bus Address	R/W	If an error occurs on a DATI or DATIP cycle, then address bits A17-A11 are stored in these bits. This locates the error to within a 1K segment of memory. The error can be either double only or single and double as selected by the user. If another error occurs, the new error address overlays the previous address even if the master failed to read it. These bits are cleared by writing a zero via a CSR write cycle.
4-3	Unused	R/O	Read as zeroes



NOTE: All unused bits are read as zeroes.

FIGURE 2-1 – CONTROL AND STATUS REGISTER

2	Write Wrong Checkword	R/W	If bit 2 is a one, then the memory's control logic inverts two checkbits during a DATO or DATOB cycle into memory. This in effect produces a dual error in a subsequent read cycle. This bit is set by writing a one via a CSR write cycle. This bit is cleared by INIT or by writing a zero via a CSR write cycle.
1	Unused	R/O	Read as zero
0	Error Indicator Enable	R/W	During a DATI or DATIP cycle, if this bit is a one and a double error occurs or a single error occurs (and ESR bit 1 is a one and CSR bit 15 was zero) then the PB line on the Unibus is asserted at the same time as data. This bit is set by writing a one via a CSR write cycle. This bit is cleared by INIT or by writing a zero via a CSR write cycle.

2.2.2 Extended Control Status and Register (ECSR) Usage Description (See Figure 2-2)

BIT	NAME		FUNCTION
15	Error	R/O	Same as in Paragraph 2.2.1.
14	EUB Error Retrieval	R/O	Same as in Paragraph 2.2.1.
13-9	Unused	R/O	Read as zeroes
8-5	Address	R/O	If an error occurs on a DATI or DATIP cycle, then A21-A18 are stored in these bits regardless of the value of bit 14. If another error occurs the new error address overlays the previous address even if the master failed to read it. The failing address is obtained by setting bit 14 to 1 and reading the CSR.
4-3	Unused	R/O	Read as zeroes
2	Write Wrong Checkword	R/O	Same as in Paragraph 2.2.1.
1	Unused	R/O	Read as zero
0	Error Indicator Enable	R/O	Same as in Paragraph 2.2.1.

2.2.3 Error Status Register (ESR) Usage Description (See Figure 2-3)

The Error Status Register (ESR) provides information about the exact location of a failed RAM device. The ESR is accessed by preceding the DATI, DATIP, or DATO with a DATOB to the lower byte of the CSR. DATOB cycles to the ESR register generate undefined results.

BIT	NAME		FUNCTION
15	Error	R/O	Same as in Paragraph 2.2.1.
14	EUB Error Retrieval	R/O	Same as in Paragraph 2.2.1.

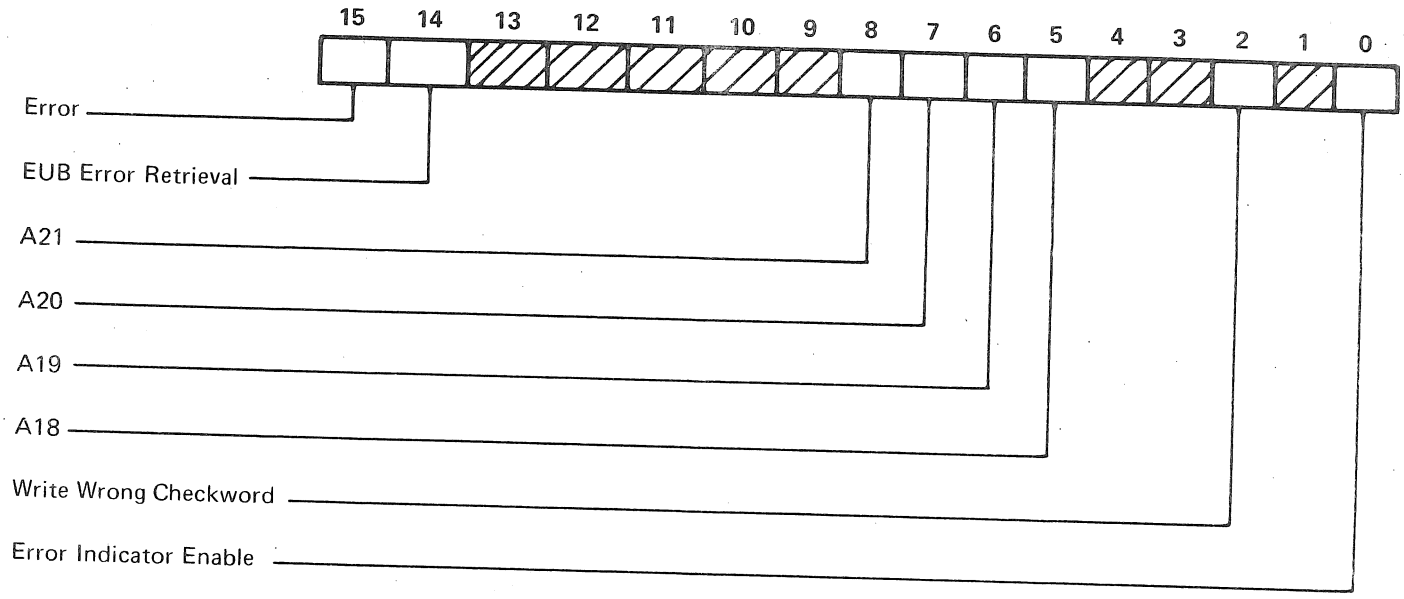


FIGURE 2-2 – EXTENDED CONTROL AND STATUS REGISTER

2.2.3 Error Status Register (ESR) Usage Description (Figure 2-3) (Continued)

13	Short Cycle on Double Error	R/W	If bit 13 is a one (set via a DATA cycle to the ESR), then an extended Read Cycle will not occur when a double bit error is detected. This bit is cleared by INIT or by writing a zero via an ESR write cycle.
12	Single Error	R/W	If bit 12 is a one (set via a DATO cycle to the ESR), then single bit errors will be logged, as well as double bit errors. This bit is cleared by INIT or by writing a zero via an ESR write cycle, or at the first occurrence of an error.
11-9	Row Number	R/O	If error bit 15 is set, then these three bits indicate the physical row that was being read when the last error occurred (Table 2-1).
8-3	Syndrome	R/O	If error bit 15 is set and ESR bit 1 is cleared then these six bits indicate the chip within the row that has generated the error (Table 2-2) meaningless at all other times.
2	Write Wrong Checkword	R/O	Same as in Paragraph 2.2.1.
1	Double Error	R/O	This flag is set unconditionally by the TMM20000 upon detecting a double bit error. Reset by INIT or during a subsequent single bit error if single error detection is enabled.
0	Error Indicator Enable	R/O	Same as Paragraph 2.2.1.

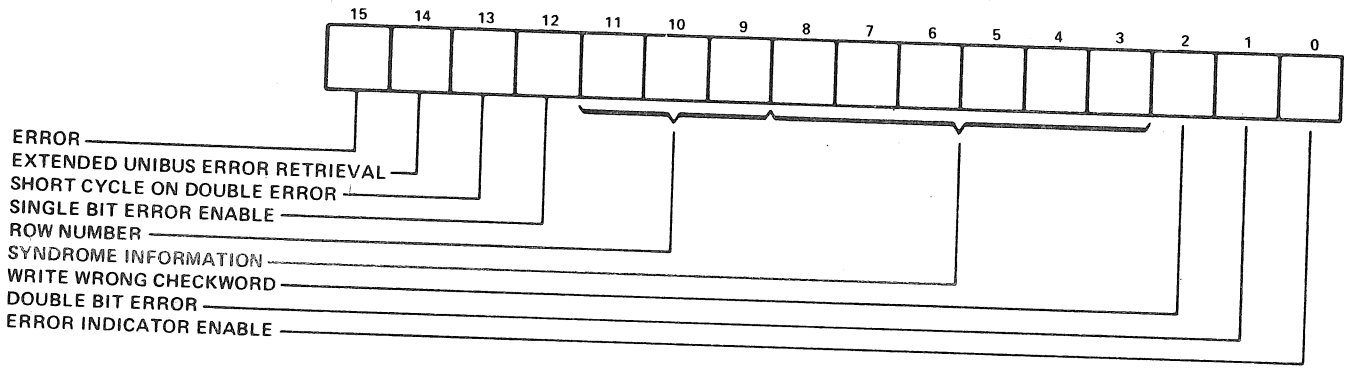


FIGURE 2-3. ERROR STATUS REGISTER

TABLE 2-1 – ROW LOCATION OF FAILED DEVICES*

PHYSICAL ROW	LEDS ESR BIT		
	D25** 11	D24** 10	D23** 9
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

* Location as defined by ESR bits 9, 10 and 11.
** A logic 0 is indicated by a lighted LED.

TABLE 2-2 – BIT LOCATION OF FAILED DEVICES*

LEDs / Syndrome Bit Position In ESR	D33 5 8	D32 4 7	D31 3 6		D30 2 5	D29 1 4	D28 0 3	Equivalent Octal Code	Location of Single Failed Bit
	0	0	1		0	1	1	13	DATA 15
	0	0	1		1	0	1	15	DATA 14
	0	0	1		1	1	0	16	DATA 13
	0	1	0		0	1	1	23	DATA 12
	0	1	0		1	0	1	25	DATA 11
	0	1	0		1	1	0	26	DATA 10
	0	1	1		0	1	0	32	DATA 9
	0	1	1		1	0	0	34	DATA 8
	0	1	1		1	1	1	37	CHECK 5
	1	0	0		0	1	1	43	DATA 7
	1	0	0		1	0	1	45	DATA 6
	1	0	1		0	0	1	51	DATA 5
	1	0	1		0	1	0	52	DATA 4
	1	0	1		1	0	0	54	DATA 3
	1	0	1		1	1	1	57	CHECK 4
	1	1	0		0	0	1	60	DATA 2
	1	1	0		0	1	0	62	DATA 1
	1	1	0		1	0	0	64	DATA 0
	1	1	0		1	1	1	67	CHECK 3
	1	1	1		0	1	1	73	CHECK 2
	1	1	1		1	0	1	75	CHECK 1
	1	1	1		1	1	0	76	CHECK 0

* As defined by the six syndrome bits.

2.3 ERROR STATUS REGISTER ACCESS

The ESR is accessible only via a preceding DATOB to the low byte of the CSR address. The next DATO or DATI cycle to the CSR address accesses the contents of the ESR. Subsequent accesses to this location automatically revert to the CSR contents. Thus, the ESR is totally invisible with all normal access protocols to the CSR.

2.4 ERROR STATUS DISPLAY

The error Status Display is composed of LEDs clearly visible on the edge of the TMM20000 and lighted as follows:

ERROR	BITS IN ESR	LED INDICATORS	COLOR	
Error Flag	15	D26	RED	
Row Number	11 through 9	D23 through D25	GREEN	(Low logic level
Syndrome	8 through 3	D28 through D33	YELLOW	when lighted)

The array Power LED (D27) lights GREEN.

3. INSTALLATION

3.1 GENERAL

This chapter includes all information required to install and configure the TMM20000 Series Add-In Memory Modules in the PDP-11 system backplane.

3.2 UNPACKING

Carefully lift the module from the special shipping carton and remove the protective urethane foam packing.

CAUTION

Each module is enclosed in an antistatic bag to protect the random access memories (RAM) from the highly static urethane foam. Appropriate precautions should be taken when removing this covering.

After removing the antistatic bag, check the memory board for damage such as cracks, broken leads and ceramics. Report any discrepancies to the supplier.

3.3 CONFIGURING A TMM20000

Configuring the modules involves selecting the address range by means of switches and implementing functional operations with jumpers. See Figure 3-1.

3.3.1 Switch Position Selection

The switch positions for the TMM20000 bus type (Modified Unibus or Extended Unibus), selected Starting Address, Status Register Address and size of the Reserve I/O Space are given in Tables 3-1, 3-2, 3-3, 3-4, and 3-5. Examples of typical switch configurations are shown in Table 3-6.

3.3.1.1 Selecting Bus Type

Set E52-8 to the appropriate position according to Table 3-1 for either a Modified Unibus or an Extended Unibus system.

TABLE 3-1 – BUS TYPE SELECT TABLE

BUS TYPE	E52-8
MODIFIED UNIBUS (18 ADDRESS LINES)	OPEN
EXTENDED UNIBUS (22 ADDRESS LINES)	CLOSED

3.3.1.2 Selecting a Starting Address in Modified Unibus System

Set switches E52-4, E52-5, E52-6 and E52-7 to the OPEN switch position. Select the Starting Address according to Table 3-2.

For example: For Starting Address = 64KW = 400000.

E52-8 = OPEN for Modified Unibus
E52-7 = E52-6 = E52-5 = E52-4 = OPEN
E52-3 = CLOSED, E52-2 = OPEN
E52-1 = OPEN.

3.3.1.3 *Selecting a Starting Address in Extended Unibus System*

Select the 128KW block of the address space in which the Starting Address is desired according to Table 3-3. Next select the Starting Address within the 128KW block according to Table 3-2.

For example: For Starting Address = 160KW = 01200000.

E52-8 = CLOSED for Extended Unibus
E52-7 = OPEN, E52-6 = OPEN
E52-5 = OPEN, E52-4 = CLOSED
E52-3 = OPEN, E52-2 = CLOSED
E52-1 = OPEN.

TABLE 3-2 – STARTING ADDRESS SELECT TABLE MODIFIED UNIBUS AND EXTENDED UNIBUS

STARTING ADDRESS		SWITCH POSITIONS		
DECIMAL	OCTAL	E52-3	E52-2	E52-1
0KW	000000	OPEN	OPEN	OPEN
16KW	100000	OPEN	OPEN	CLOSED
32KW	200000	OPEN	CLOSED	OPEN
48KW	300000	OPEN	CLOSED	CLOSED
64KW	400000	CLOSED	OPEN	OPEN
80KW	500000	CLOSED	OPEN	CLOSED
96KW	600000	CLOSED	CLOSED	OPEN
112KW	700000	CLOSED	CLOSED	CLOSED

TABLE 3-3 – STARTING ADDRESS SELECT TABLE –EXTENDED UNIBUS

PARTIAL STARTING ADDRESS		SWITCH POSITIONS			
DECIMAL	OCTAL	E52-7	E52-6	E52-5	E52-4
0KW	00RRRRRR	OPEN	OPEN	OPEN	OPEN
128KW	01RRRRRR	OPEN	OPEN	OPEN	CLOSED
256KW	02RRRRRR	OPEN	OPEN	CLOSED	OPEN
384KW	03RRRRRR	OPEN	OPEN	CLOSED	CLOSED
512KW	04RRRRRR	OPEN	CLOSED	OPEN	OPEN
640KW	05RRRRRR	OPEN	CLOSED	OPEN	CLOSED
768KW	06RRRRRR	OPEN	CLOSED	CLOSED	OPEN
896KW	07RRRRRR	OPEN	CLOSED	CLOSED	CLOSED
1024KW	10RRRRRR	CLOSED	OPEN	OPEN	OPEN
1152KW	11RRRRRR	CLOSED	OPEN	OPEN	CLOSED
1280KW	12RRRRRR	CLOSED	OPEN	CLOSED	OPEN
1408KW	13RRRRRR	CLOSED	OPEN	CLOSED	CLOSED
1536KW	14RRRRRR	CLOSED	CLOSED	OPEN	OPEN
1664KW	15RRRRRR	CLOSED	CLOSED	OPEN	CLOSED
1792KW	16RRRRRR	CLOSED	CLOSED	CLOSED	OPEN
1920KW	17RRRRRR	CLOSED	CLOSED	CLOSED	CLOSED

NOTE: RRRRRR is the portion of the address listed in Table 3-2.

3.3.1.4 *Selecting a Status Register (CSR/ESR) Address*

Select switch positions for the desired Status Register Address according to Table 3-4. Note that proper software operation requires that each parity controller within the total memory system have a unique CSR address.

3.3.1.5 *Selecting a Reserve I/O Space*

Select switch positions for the desired Reserve I/O Space size according to Table 3-5.

TABLE 3-4 – CSR ADDRESS SELECTION

UNIBUS ADDRESS	SPECIAL BUS ADDRESS	SWITCH POSITIONS				
		E50-8 (DISABLE)	E50-7 (A04)	E50-6 (A03)	E50-5 (A02)	E50-4 (A0)
772100	17772100	OPEN	CLOSED	CLOSED	CLOSED	CLOSED
772102	17772102	OPEN	CLOSED	CLOSED	CLOSED	OPEN
772104	17772104	OPEN	CLOSED	CLOSED	OPEN	CLOSED
772106	17772106	OPEN	CLOSED	CLOSED	OPEN	OPEN
772110	17772110	OPEN	CLOSED	OPEN	CLOSED	CLOSED
772112	17772112	OPEN	CLOSED	OPEN	CLOSED	OPEN
772114	17772114	OPEN	CLOSED	OPEN	OPEN	CLOSED
772116	17772116	OPEN	CLOSED	OPEN	OPEN	OPEN
772120	17772120	OPEN	OPEN	CLOSED	CLOSED	CLOSED
772122	17772122	OPEN	OPEN	CLOSED	CLOSED	OPEN
772124	17772124	OPEN	OPEN	CLOSED	OPEN	CLOSED
772126	17772126	OPEN	OPEN	CLOSED	OPEN	OPEN
772130	17772130	OPEN	OPEN	OPEN	CLOSED	CLOSED
772132	17772132	OPEN	OPEN	OPEN	CLOSED	OPEN
772134	17772134	OPEN	OPEN	OPEN	OPEN	CLOSED
772136	17772136	OPEN	OPEN	OPEN	OPEN	OPEN
DISABLE	DISABLE	CLOSED	X	X	X	X

X = Don't Care

TABLE 3-5 – RESERVE I/O SPACE

I/O PAGE SIZE	MODIFIED UNIBUS LOCATION	EXTENDED UNIBUS LOCATION	SWITCH POSITIONS		
			E50-3	E50-2	E50-1
2KW	126KW – 128KW	2046KW – 2048KW	OPEN	CLOSED	CLOSED
4KW	124KW – 128KW	2044KW – 2048KW	OPEN	CLOSED	OPEN
8KW	120KW – 128KW	2040KW – 2048KW	OPEN	OPEN	OPEN
DISABLE	N/A	N/A	CLOSED	X	X

X = don't care.

TABLE 3-6 – EXAMPLES OF COMMON SWITCH CONFIGURATIONS

SWITCH	SETTING
E50-1	OPEN
-2	CLOSED
-3	OPEN
-4	CLOSED
-5	CLOSED
-6	CLOSED
-7	CLOSED
-8	OPEN

SWITCH	SETTING
E52-1	OPEN
-2	OPEN
-3	OPEN
-4	OPEN
-5	OPEN
-6	OPEN
-7	OPEN
-8	OPEN

Modified Unibus (18 Address Lines)
Memory Starting Address = 000000
Parity Register (CSR/ESR) = 772100
Reserve I/O Space = 4 KW

SWITCH	SETTING
E50-1	OPEN
-2	CLOSED
-3	OPEN
-4	OPEN
-5	CLOSED
-6	CLOSED
-7	CLOSED
-8	OPEN

SWITCH	SETTING
E52-1	OPEN
-2	OPEN
-3	OPEN
-4	CLOSED
-5	OPEN
-6	OPEN
-7	OPEN
-8	CLOSED

Extended Unibus (22 Address Lines)
Memory Starting Address = 128 KW = 01000000
Parity Register (CSR/ESR) = 17772102
Reserve I/O Space = 4 KW

3.3.2 System Application (Deleted)

3.3.3 Interleave/Noninterleave Switch Positions

A continuous (noninterleaved) address block may be assigned to each TMM20000 module or an address block may be interleaved between two TMM20000 modules having the same storage capacity. Both modules should be assigned the same starting address.

Jumper installation and removal for the interleave options are given in Table 3-8. Note that one card must be configured to respond to even addressed, while the other is configured to respond to all odd addresses. In addition, each module must have a unique CSR address. Figure 3.1 shows jumper locations.

TABLE 3-8 – INTERLEAVE JUMPER SELECTION

JUMPER	NON INTL	64KW INTL	128KW INTL	256KW INTL	512KW INTL
J38 – J39	I	I	I	I	I
J40 – J42					I
J41 – J43					I
J42 – J43	I	I	I	I	
J44 – J45	I	I	I		I
J44 – J46				I	
J45 – J47				I	
J48 – J49	I	I		I	I
J49 – J47			I		
J50 – J51	I		I	I	I
J51 – J52		I			
J52 – J53	I				
J48 – J46			I		
SWITCH ON = ODD OFF = EVEN		E52-3	E52-4	E52-5	E52-6

3.3.4 Memory Array Size

Table 3-9 lists the required jumper arrangement for the eight array sizes. Figure 3-1 shows the jumper locations.

TABLE 3-9 – MEMORY ARRAY SIZE JUMPER SELECTION

JUMPER		NUMBER OF ROWS							
TO	FROM	1	2	3	4	5	2	7	8
21	24	1	1	1	1	0	0	0	0
22	25	1	1	0	0	1	1	0	0
23	26	1	0	1	0	1	0	1	0

3.3.5 Battery Backup Option

Table 3-10 shows the jumper configurations for standard battery backup modes of TMM20000 operation. Figure 3-2 illustrates these modes.

TABLE 3-10 – BATTERY BACKUP JUMPER SELECTION

JUMPERS	BATTERY BACKUP	NON-BATTERY BACKUP
J57-J58	YES	NO
J58-J59	NO	YES

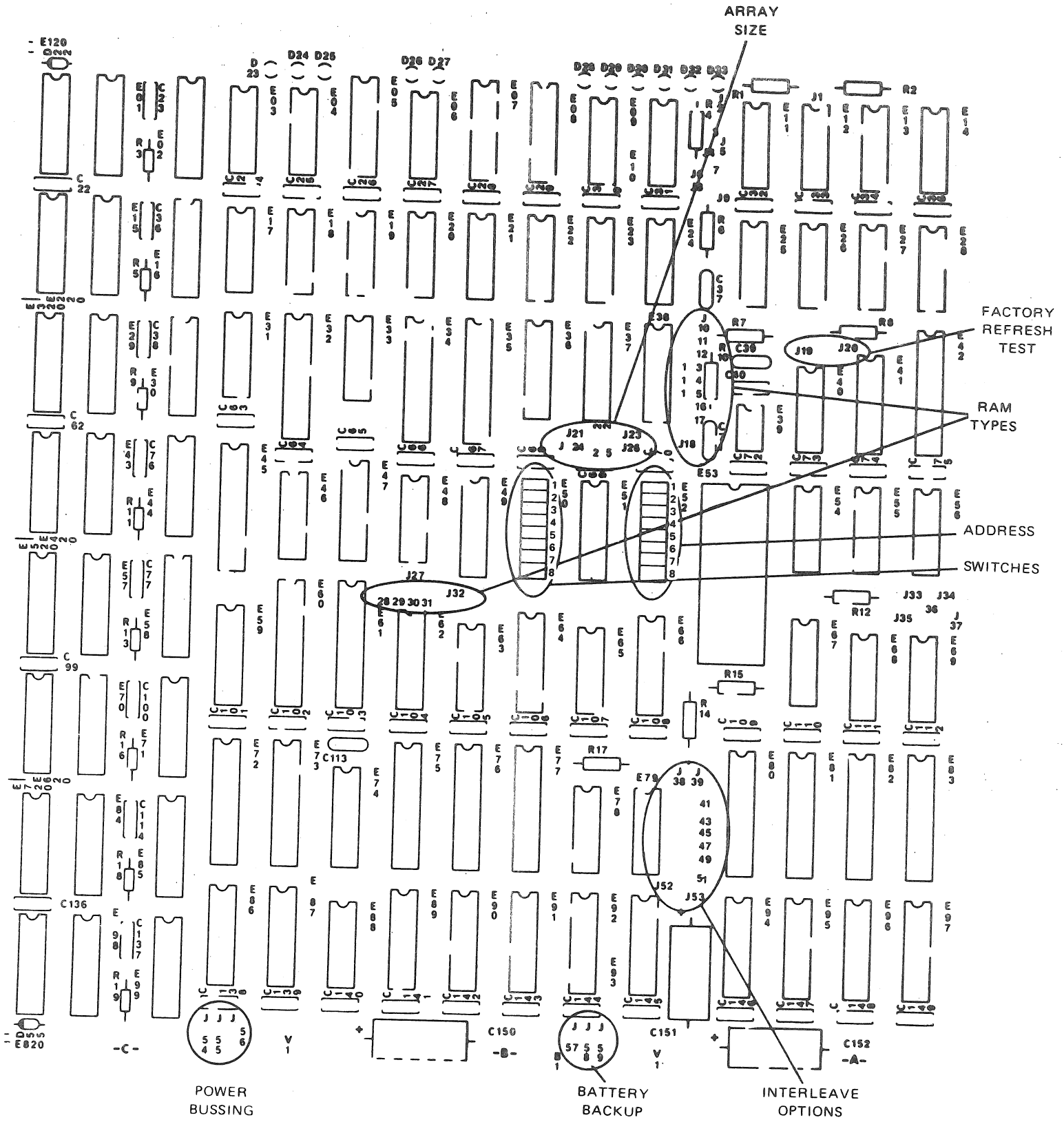


FIGURE 3-1 – SWITCH AND JUMPER LOCATIONS

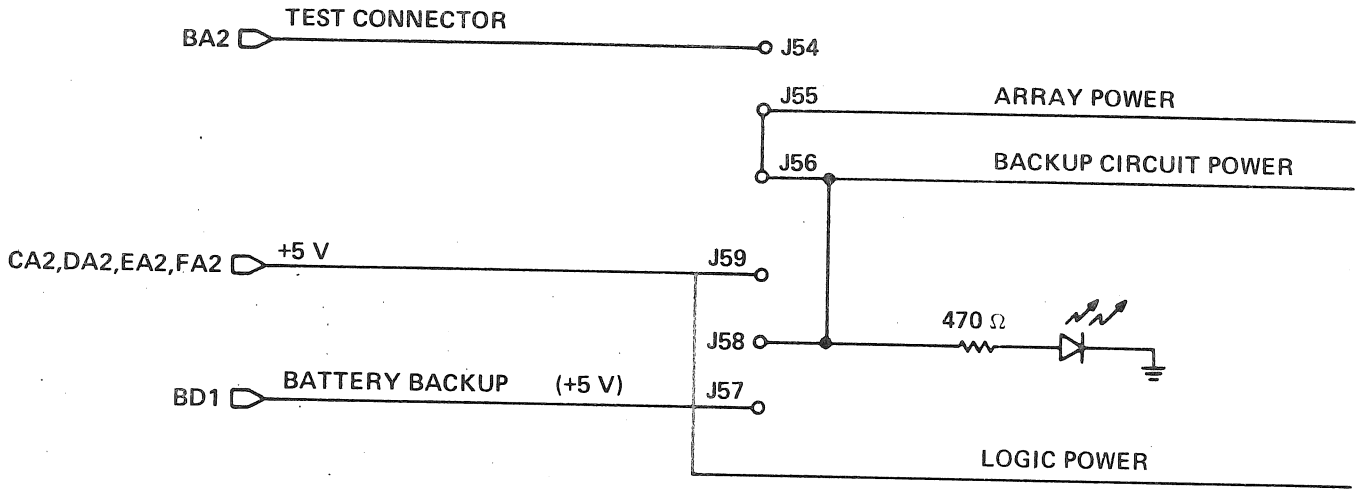


FIGURE 3-2 – STANDARD AND BATTERY BACKUP JUMPER CONFIGURATIONS

3.4 INSTALLATION INTO SYSTEM

Proper installation ensures normal TMM20000 module operation in the PDP-11 system and prevents possible damage to the module or the backplane in which it is installed.

A module must be installed or removed only when DC power is removed from the backplane.

CAUTION

The TMM20000 Add-In Memory and the backplane assembly mounting blocks may be damaged if a module is plugged in backwards.

The TMM20000 pin list is shown in Table 3-11.

3.5 DEC DIAGNOSTICS

There are two DEC memory exerciser diagnostic programs available to verify proper operation of a TMM20000 Add-In Memory Module with a PDP-11 computer. MAINDEC-11 CZOMC should be run in conjunction with a PDP-11/34 and MAINDEC-11 CZMSD with a PDP-11/44. No errors are permitted during two complete passes. Notify agency where purchased (TI Sales Office or Authorized Distributor) if a failure occurs.

TABLE 3-11 – PIN LIST (UNIBUS PIN ASSIGNMENT)

PIN	STANDARD	MODIFIED	EXTENDED	PIN	STANDARD	MODIFIED	EXTENDED
AA1	INIT L			BA1	Not Used		
AA2	+5 V			BA2	+5 V		
AB1	Not Used			BB1	Not Used		
AB2	Not Used			BB2	Not Used		
AC1	D00 L			BC1	Not Used		
AC2	Ground			BC2	Ground		
AD1	D02 L			BD1	Not Used	+5 Batt	+5 Batt
AD2	D01 L			BD2	Not Used		
AE1	D04 L			BE1	Not Used	Not Used	A19 L
AE2	D03L			BE2	Not Used	Not Used	A18 L
AF1	D06 L			BF1	Not Used		
AF2	D05 L			BF2	DCL0 L		
AH1	D08 L			BH1	A01 L		
AH2	D07 L			BH2	A00 L		
AJ1	D10 L			BJ1	A03 L		
AJ2	D09 L			BJ2	A02 L		
AK1	D12 L			BK1	A05 L		
AK2	D11 L			BK2	A04 L		
AL1	D14 L			BL1	A07 L		
AL2	D13 L			BL2	A06 L		
AM1	Not Used			BM1	A09 L		
AM2	D15 L			BM2	A08 L		
AN1	Not Used	Not Used	A21 L	BN1	A11 L		
AN2	PB L			BN2	A10 L		
AP1	Not Used	Not Used	A20 L	BP1	A13 L		
AP2	Not Used			BP2	A12 L		
AR1	Not Used			BR1	A15 L		
AR2	Not Used			BR2	A14 L		
AS1	Not Used			BR1	A17 L		
AS2	Not Used			BR2	A16 L		
AT1	Ground			BT1	Ground		
AT2	Not Used			BT2	C1 L		
AU1	Not Used			BU1	SSYNL		
AU2	Not Used			BU2	C0 L		
AV1	Not Used			BV1	MSYN L		
AV2	Not Used			BV2	Not Used		