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decgraphic 11 GT Series Reference Card



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GRAPHIC INSTRUCTIONS

The information provided here is meant to serve the user as a quick look-up reference for the graphic instructions. More detailed explanations and examples are given in the GRAPHICS User's Manual.

The operator can view the terminal as two separate programmable processors: 1.) the Central Processor (CPU) which initiates the Display Processor (DPU) and executes PDP-11 type code; and 2.) the Display Processor (DPU) which fetches and executes its own instructions and data from memory but, in general, uses the CPU to drive dispatch tables, answer interrupts, and perform arithmetic and logical functions on complex data structure.

A. IMPORTANT ADDRESSES

1.) DISPLAY Addresses

START ADDRESS (SA) = 172000 = DPC (Read/Write)

The SA is the UNIBUS address in which the data being MOV'ed is the start address of the display list. This data then becomes the Display Program Counter (DPC). The address should be a word address—i.e., an even number. When read, this register produces the DPC to the user.

RESUME ADDRESS (RA) = 172000 (Write)

To RESUME a display, for example, after a light pen hit, a one in bit zero (LSB) should be MOV'ed to the RA.

Display Status Register (DSR) = 172002 (Read/Write)

STOP FLAG	Bit(s)	(15)	(MSB)	(READ)
MODE		(14:11)		
INTENSITY		(10:8)		
LIGHT PEN FLAG		(7)		
SHIFT OUT		(6)		
EDGE INDICATOR		(5)		
ITALICS		(4)		
BLINK		(3)		
SPARE (Unused)		(2)		
LINE		(1:0)		

When the DSR is "written" the effect is to ring the "Bell."

X STATUS REGISTER = 172004 (READ)

X Position = bits (9:0)
Graphplot
Increment = bits (15:10)

Y STATUS REGISTER = 172006 (READ)

Y Position = bits (9:0)
Character
Register = bits (15:10)

When in "SHIFTED OUT" character mode and a code 40→137₈ is fetched, the program is interrupted and this register can be read to find the index to a user routine to draw, for example, a user defined character (in software).

Interrupt Vectors

There are three Display Interrupts*:

Interrupt	Vector Address
1.) STOP	320/322
2.) Light Pen	324/326
3.) Time Out Shift Out	330/332

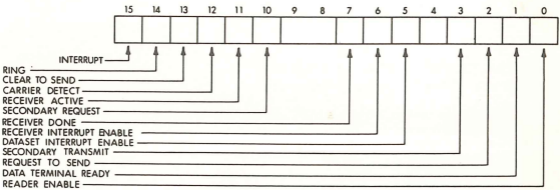
*All Interrupts are requested at level BR4.

2.) Communications Interface Addresses (DL11)

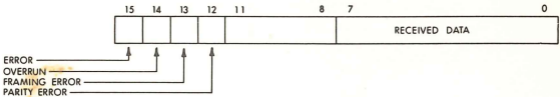
Receive Command & Status Register (RCSR)	= 175610
Receive Buffer (RBUF)	= 175612
Transmit Command & Status Register (XCSR)	= 175614
Transmit Buffer (XBUF)	= 175616

The register configurations are shown below for completeness only. Details are available in the DL11 Manual.

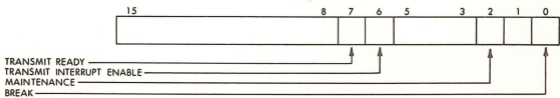
RCSR = 175610



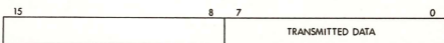
RBUF = 175612



XCSR = 175614



XBUF = 175616



Interrupt Vectors for DL11's are exhibited below:

- 300/302 = Receiver Interrupt
- 304/306 = Transmitter Interrupt

Interrupts are requested on level BR5.

3.) Other useful registers are also listed for reference

CPU GENERAL REGISTERS (only console addressable)	R0 : : R7	177700 : : 177707
CPU Console Switches (console & CPU addressable)	SWR	177570
CPU Status (console & CPU addressable)	PS	177776
Keyboard Command & Status	KCSR	177560
Keyboard Data Buffer	KDBR	177562
Keyboard Interrupt Vector		60/62
Line Frequency Clock (KW11-L)		177546
DL-11 Bootstrap S.A. (GT40)		166000
RK Bootstrap S.A. (GT44) (Word Count = 177406)		173100

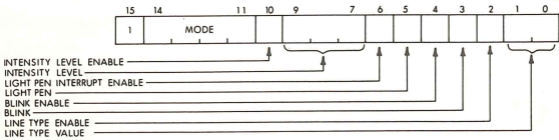
B. INSTRUCTION SET

1.) GRAPHICS

The graphics instruction set as presented here is simple, yet concise and powerful consisting of basic instructions:

- Set Graphic Modes
- Jump
- No-Op
- Load Status Registers

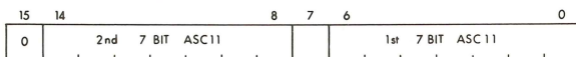
Set Graphic Mode



Bits	Title	Description
(15)	—	“1” indicates control word
(14:11)	Mode	0000 set character mode 0001 set short vector mode 0010 set long vector mode 0011 set point mode 0100 set graph X mode 0101 set graph Y mode 0110 set relative point mode 0111 spare
(10)	Intensity level enable	“1” enables bits 9-7 into the intensity register
(9:7)	Intensity level	3-bit intensity value 000 = minimum intensity 111 = maximum intensity
(6)	Light Pen Interrupt Enable	When set, enables bit 5 into LP interrupt enable register
(5)	Light Pen	1 = L.P. interrupt enabled 0 = No L.P. interrupt

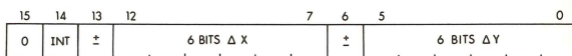
Bits	Title	Description
(4)	Blink enable	When set, enables bit 3 into blink register
(3)	Blink	1 = blink on; 0 = blink off
(2)	Line type enable	"1" enables bits 1-0 into the line register
(1:0)	Line type value	2-bit line type value 00 = solid line 01 = long dash 10 = short dash 11 = dot dash

Character Data Format—Mode 0000



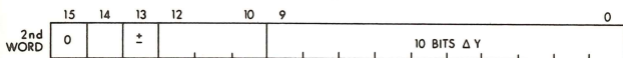
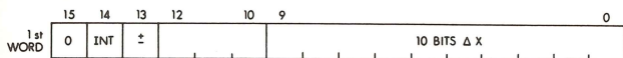
- | | | |
|--------|-------------|-------------------------|
| (15) | — | "0" indicates data word |
| (14:8) | 7 Bit ASCII | 7 bit ASCII code |
| (7) | — | Spare |
| (6:0) | 7 Bit ASCII | 7 bit ASCII code |

Short Vector Data Format—Mode 0001



- | | | |
|--------|-------------------|---|
| (15) | — | "0" indicates data word |
| (14) | Intensify | If a "1" then intensify vector |
| (13) | Positive/negative | "0" indicates ΔX component moves to the right, "1" indicates ΔX moves to the left |
| (12:7) | 6 bits ΔX | 6 bit magnitude of the X component of the vector |
| (6) | Positive/negative | "0" indicates ΔY component moves up; "1" indicates ΔY moves down |
| (5:0) | 6 bits ΔY | 6 bit magnitude of the vector |

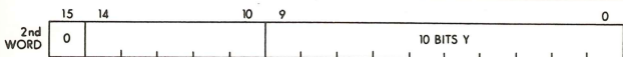
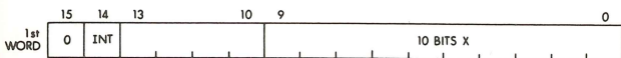
Long Vector Data Format—Mode 0010



1st word	{	15	—	"0" indicates data word
		14	Intensify	"1" indicates intensify vector
		13	Positive/negative	"0" = + ΔY "1" = - ΔY
		12:10	—	Spare
		9:0	10 bits ΔX	10 bit magnitude of the X component

2nd word	{	15	—	"0" indicates data word
		14	—	Spare
		13	Positive/negative	"0" = + ΔY "1" = - ΔY
		12:10	—	Spare
		9:0	10 bits ΔY	10 bit magnitude of the Y component

Point Data Format—Mode 0011



1st word	{	15	—	"0" indicates data word
		14	Intensify	"1" indicates intensify point
		13:10	—	Spare
		9:0	10 bits X	10 bit x coordinate

2nd word	{	15	—	"0" indicates data word
		14:10	—	Spare
		9:0	10 bits Y	10 bit Y coordinate

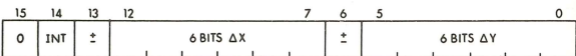
Graphplot X Data Format—Mode 0100

Graphplot Y Data Format—Mode 0101



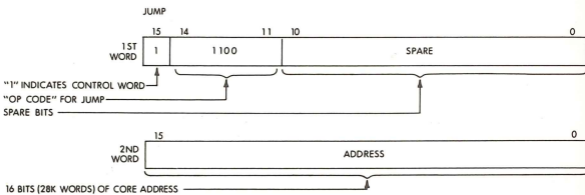
- (15) — "0" indicates data word
- (14:10) — Spare
- (9:0) 10 bit X(Y) 10 bit X (Y if graph Y) coordinate

Relative Point Data Format—Mode 0110



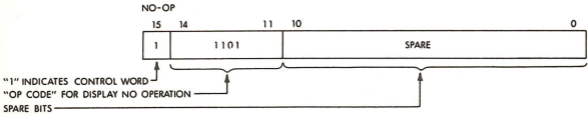
- (15) "0" indicates data word
- (14) Intensify If a "1," then intensify the point
- (13) Positive/negative "0" indicates ΔX moves to the right, "1" indicates ΔX moves to the left
- (12:7) 6 bits ΔX 6 bit magnitude of the X component of the move
- (6) Positive/negative "0" indicates ΔY moves up "1" indicates ΔY moves down
- (5:0) 6 bits ΔY 6 bit magnitude of the Y component of the move

Jump—160000



- | | | | | |
|----------|---|-------|---------|-------------------------------------|
| 1st word | } | 15 | — | "1" indicates control word |
| | | 14:11 | — | "op-code" for jump |
| | | 10:0 | Spare | Unused |
| 2nd word | } | 15:0 | Address | 16 bits (28K words) of core address |

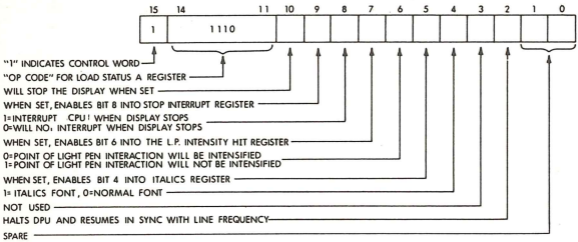
DNOP—164000



- | | | |
|---------|-------|------------------------------------|
| (15) | — | "1" indicates control word |
| (14:11) | — | "op-code" for display no operation |
| (10:0) | Spare | Spare Bits |

Performs no operation

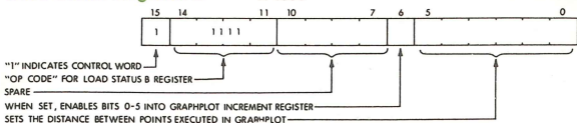
Load Status Register A 170000



- | | | |
|---------|-----------------------|--|
| (15) | — | "1" indicates control word |
| (14:11) | — | "op-code" for load status A register |
| (10) | Stop | Will stop the display when set |
| (9) | Stop Interrupt Enable | When set, enables bit 8 into stop interrupt register |
| (8) | Interrupt | 1 = interrupt PDP-11 when display stops
0 = will not interrupt when display stops |
| (7) | LP Intensity HIT ENA | When set, enables bit 6 into the LP Intensity HIT register |
| (6) | LP Intensity HIT | 0 = point of light pen interaction will be intensified
1 = point of light pen interaction will not be intensified |
| (5) | Italics Enable | When set, enables bit 4 into italics register |
| (4) | Italics | 1 = italics font
0 = normal font |
| (3) | Spare | Not used |
| (2) | Sync | Halts DPU and resumes in sync with the line frequency |
| (0) | Spare | Not used |

Load Status Register B

174000



(15)	—	"1" indicates control word
(14:11)	—	"Op-code" for load status B register
(10:7)	—	Spare
(6)	Graphplot Increment Enable	When set enables bits 5-0 into graphplot increment register
(5:0)	Graphplot Increment	Sets the distance between points executed in graphplot

CPU Instructions

A synopsis of the PDP-11 instructions is presented below:

GENERAL REGISTER ADDRESSING

Mode	Description	Symbolic
0	register	R
1	register deferred	@R or (R)
2	auto-increment	(R)+
3	auto-increment deferred	@(R)+
4	auto-decrement	-(R)
5	auto-decrement deferred	@-(R)
6	indexed	±X(R)
7	indexed deferred	@±X(R) or @(R)

(±X is an index word)

PC REGISTER ADDRESSING

Mode	Description	Symbolic
2	immediate	#n
3	absolute	@#n
6	relative	A
7	relative deferred	@A

Legend

OP FIELDS

■	Byte(1)/Word(0)	R	Register
SS	Source Field (6 bits)	XXX	Offset (8 bits)
DD	Destination Field (6 bits)	v	Exclusive or
		v	Inclusive or
		Λ	And

Note:

▲ = Applies to the 11/40 computer

MNEMONIC INSTRUCTION

OP
CODE

Double Operand Group: OPR src, dst

MOV(B)	MOVE	■1SSDD
CMP(B)	CoMPare	■2SSDD
BIT(B)	Bit Test	■3SSDD
BIC(B)	Bit Clear	■4SSDD
BIS(B)	Bit Set	■5SSDD
ADD	ADD	06SSDD
SUB	SUBtract	16SSDD

Subroutine Call: JSR reg, dst

JSR	Jump to SubRoutine	004RDD
-----	--------------------	--------

Subroutine Return: RTS reg

RTS	ReTURN from Subroutine	00020R
-----	------------------------	--------

Operate Group: OPR

HALT	HALT	000000
WAIT	Wait for InTerrupt	000001
RTI	ReTurn from Interrupt	000002
▲RTT	ReTurn from InTerrupt inhibit T bit trap	000006
—	breakpoint trap (vector at 14)	000003
IOT	Input/Output Trap (vector at 20)	000004
RESET	RESET	000005
EMT	EMulator Trap (vector at 30)	104000- 104377
TRAP	TRAP (vector at 34)	104400- 104777

Single Operand Group: OPR dst

CLR(B)	CLear	■050DD
COM(B)	COMplement	■051DD
INC(B)	INCrement	■052DD
DEC(B)	DECrement	■053DD
NEG(B)	NEGate	■054DD
ADC(B)	ADd Carry	■055DD
SBC(B)	SuBtract Carry	■056DD
TST(B)	TeST	■057DD
ROR(B)	ROtate Right	■060DD
ROL(B)	ROtate Left	■061DD
ASR(B)	Arith. Shift Right	■062DD
ASL(B)	Arith. Shift Left	■063DD
JMP	JuMP	0001DD
SWAB	SWap Bytes	0003DD
▲SXT	Sign eXTend	0067DD

Condition Code Operator: OPR

Condition Code Operators set or clear condition code bits.
Indicated bits are set if S = 1 and cleared otherwise.

0	0	0	2	4	s	n	z	v	c			
15	14	12	11	9	8	6	5	4	3	2	1	0

CLC	CLEAR C	000241
CLV	CLEAR V	000242
CLZ	CLEAR Z	000244
CLN	CLEAR N	000250
SEC	SET C	000261
SEV	SET V	000262
SEZ	SET Z	000264
SEN	SET N	000270
—	No Operation	000240
—	No Operation	000260

Conditional Branches: B-- Location

BR	BRanch always	000400+XXX
BNE	Branch if Not Equal (zero) (Z=0)	001000+XXX
BEQ	Branch if Equal (zero) (Z=1)	001400+XXX
BGE	Branch if Greater or Equal (zero) (NvV=0)	002000+XXX
BLT	Branch if Less Than (zero) (NvV=1)	002400+XXX
BGT	Branch if Greater Than (zero) (Zv(NvV)=0)	003000+XXX
BLE	Branch if Less or Equal (zero) (Zv(NvV)=1)	003400+XXX
BPL	Branch if Plus (N=0)	100000+XXX
BMI	Branch if Minus (N=1)	100400+XXX
BHI	Branch if Higher (CvZ=0)	101000+XXX
BLOS	Branch if LOwer or Same (CvZ=1)	101400+XXX
BVC	Branch if oVerflow Clear (V=0)	102000+XXX
BVS	Branch if oVerflow Set (V=1)	102400+XXX
BCC (or BHIS)	Branch if Carry Clear (C=0)	103000+XXX
BCS (or BLO)	Branch if Carry Set (C=1)	103400+XXX
	XXX Offset (8 bits)	0064NN
▲MARK	Mark	
▲SOB	Subtract 1 & Br (if = 0)	077RNN

7-bit code octal	ASCII Representation	Keyboard	GT40 Printing	When preceded by Shift-Out=016†
000	NUL	CTRL @		λ
001	SOH	CTRL A		
002	STX	CTRL B		φ
003	ETX	CTRL C		Σ
004	EOT	CTRL D		δ
005	ENQ	CTRL E		Δ
006	ACK	CTRL F		
‡007	Bel	CTRL G		
*010	BS	CTRL H	Backspace	∩
011	HT	CTRL I (TAB)		ψ
*012	LF	CTRL J (LF)	Line Feed	÷
013	VT	CTRL K		ο
014	FF	CTRL L		. .
*015	CR	CTRL M (CR)	Carriage Return	μ
016	SO	CTRL N		£
017	SI	CTRL O		Shift In
020	DLE	CTRL P		π
021	DC1	CTRL Q		
022	DC2	CTRL R		Ω
023	DC3	CTRL S		σ
024	DC4	CTRL T		τ
025	NAK	CTRL U		ε
026	SYN	CTRL V		←
027	ETB	CTRL W		→
030	CAN	CTRL X		↑
031	EM	CTRL Y		↓
032	SUM	CTRL Z		∟
033	ESC	CTRL [(ALT)		T
034	FS	CTRL		=
035	GS	CTRL]		
036	PS	CTRL v		V
037	US	CTRL ____		□
†040	SP	SPACE BAR	Space 1 character	
041	!	SHIFT 1	!	
042	"	SHIFT 2	"	
043	#	SHIFT 3	#	
044	\$	SHIFT 4	\$	
045	%	SHIFT 5	%	
0466	&	SHIFT 6	&	
047	'	SHIFT 7	'	

* CR, LF and BS are performed by the display hardware. All other control characters are ignored except in S.O. (Shift Out) mode.

‡ The "Bell" is sounded in the keyboard by MOV'ing a number to Address 172002.
e.g. MOV #2, 172002

† All codes from 40₈ up are illegal under "Shift Out" and will cause an interrupt through the "Shift Out" vector and will set the SHIFT OUT indicator in the Status Register.

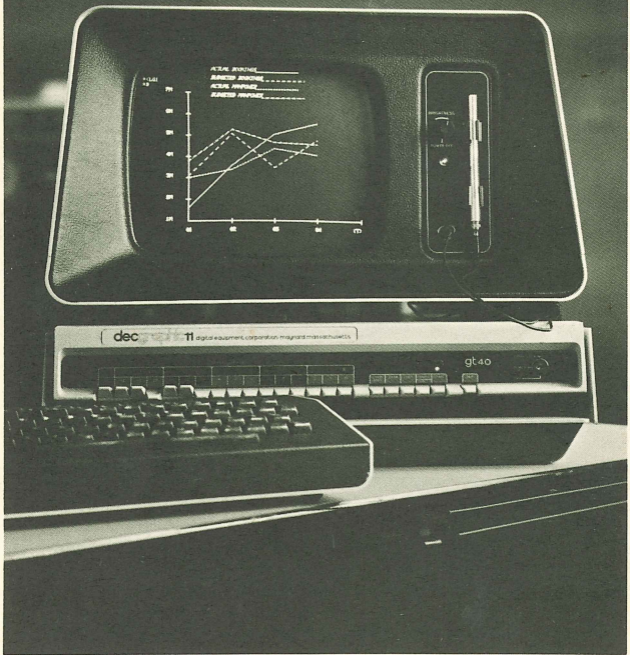
050	(SHIFT 8	(
051)	SHIFT 9)
052	*	SHIFT :	*
053	+	SHIFT ;	+
054	,	,	,
055	- (minus)	-	-
056	.	.	.
057	/	/	/
060	0	0	0
061	1	1	1
062	2	2	2
063	3	3	3
064	4	4	4
065	5	5	5
066	6	6	6
067	7	7	7
070	8	8	8
071	9	9	9
072	:	:	:
073	;	;	;
074	<	SHIFT ,	<
075	=	SHIFT -	=
076	>	SHIFT .	>
077	?	SHIFT /	?
100	@	@	@
101	A	SHIFT A	A
102	B	SHIFT B	B
103	C	SHIFT C	C
104	D	SHIFT D	D
105	E	SHIFT E	E
106	F	SHIFT F	F
107	G	SHIFT G	G
110	H	SHIFT H	H
111	I	SHIFT I	I
112	J	SHIFT J	J
113	K	SHIFT K	K
114	L	SHIFT L	L
115	M	SHIFT M	M
116	N	SHIFT N	N
117	O	SHIFT O	O
120	P	SHIFT P	P
121	Q	SHIFT Q	Q
122	R	SHIFT R	R
123	S	SHIFT S	S
124	T	SHIFT T	T
125	U	SHIFT U	U
126	V	SHIFT V	V
127	W	SHIFT W	W

7-bit code (octal)	ACSII Representation	Keyboard	GT40 Printing
130	X	SHIFT X	X
131	Y	SHIFT Y	Y
132	Z	SHIFT Z	Z
133	[SHIFT [[
134		SHIFT	
135]	SHIFT]]
136	^	SHIFT V	V
137	—	SHIFT —	—
140	'	SHIFT @	'
141	a	A	a
142	b	B	b
143	c	C	c
144	d	D	d
145	e	E	e
146	f	F	f
147	g	G	g
150	h	H	h
151	i	I	i
152	j	J	j
153	k	K	k
154	l	L	l
155	m	M	m
156	n	N	n
157	o	O	o
160	p	P	p
161	q	Q	q
162	r	R	r
163	s	S	s
164	t	T	t
165	u	U	u
166	v	V	v
167	w	W	w
170	x	X	x
171	y	Y	y
172	z	Z	x
173	{	SHIFT [{
174		SHIFT	
175	}	SHIFT]	}
176	~	SHIFT V	
177	RUB OUT	R.O.	■

Function Key Codes

← 10	↑ 32	Home	35	EOS	37
→ 30	↓ 33	EOL	36		

NOTES



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