DM900/9000
TRAINING MANUAL

DM940/980
DM940R/980R
DM940CD/980CD
DM940D/980D
DM940T/980T

DM9100/9200
DM9100/9200 w Fast Sync
DM9100CD/9200CD
DM9100D/9200D
DM9100TD/9200TD

DM9300
DM9300CD
DM9300D
DM9300TD

DP900-1/900-2
"DAISY-CHAIN" OPTION

* ⇒ AC POWER shown originating in the control unit, can also be connected to separate receptacles or into rack ac power
DM900/9000 DISK SUBSYSTEM CONFIGURATIONS

SINGLE PORT

DM900/9000 DRIVES

SINGLE PORT

DM900/9000 DRIVES

DUAL PORT

DM900D/9000D DRIVES

DUAL PORT

DM900D/9000D DRIVES

DP900 DUAL PORT ADAPTORS
DM900/9000 DRIVES

DP900 DUAL PORT ADAPTORS
DM900/9000 DRIVES

Radical Configuration no longer offered
<table>
<thead>
<tr>
<th>VOLTAGE</th>
<th>CURRENT</th>
<th>REGULATION</th>
<th>MAXIMUM RIPPLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5v</td>
<td>6a</td>
<td>.02%</td>
<td>50mv</td>
</tr>
<tr>
<td>-5v</td>
<td>2.5a</td>
<td>.02%</td>
<td>50mv</td>
</tr>
<tr>
<td>+15v</td>
<td>1a</td>
<td>.01%</td>
<td>50mv</td>
</tr>
<tr>
<td>-15v</td>
<td>1a</td>
<td>.01%</td>
<td>50mv</td>
</tr>
<tr>
<td>+25v</td>
<td>250ma</td>
<td>.01%</td>
<td>50mv</td>
</tr>
<tr>
<td>+36v</td>
<td>10a</td>
<td>Unregulated</td>
<td>500mv</td>
</tr>
<tr>
<td>-36v</td>
<td>10a</td>
<td>Unregulated</td>
<td>500mv</td>
</tr>
</tbody>
</table>
INTERFACE SIGNALS

- SERVO CLOCK (9.67 MHz or 6.45 MHz)
- SELECTED
- UNIT READY (On Line)
- ON CYLINDER (Attention) [Ready or Seek Incomplete]
- SEEK END (Attention) [Ready or Seek Incomplete]
- SEEK ERROR (Seek Incomplete)
- INDEX
- SECTOR MARK
- ADDRESS MARK
- WRITE PROTECTED
- FAULT - R/W UNSAFE (Unsafe)
- SECTOR COUNT 0-6
- NINETEEN SURFACE ID
- READ DATA (NRZ or MFM)
- READ CLOCK 9.67 MHz
- WRITE DATA (NRZ or MFM)
- WRITE CLOCK
- DEVICE ENABLE (Open Cable Detector)
- DEVICE SELECT 0-3
- SELECT ENABLE (Unit Select Strobe)
- BUS OUT 0-9
- SET CYLINDER (Tag 1)
- SET HEAD ADDRESS (Tag 2)
- CONTROL SELECT (Tag 3)

* SEQUENCE PICK
  + SEQUENCE ENABLE
    - HOLD
    - SEQUENCE IN
    - SEQUENCE OUT
    - BUSY
  - PRIORITY SELECT
    - SELECTED TO OTHER PORT
    - REQUEST DESELECT
    - RECEIVE DESELECT

- signals on R/W cable, all other signals on Control cable
- # used DM9000 series only
- @ used early DM9000 series only
- $ connects between each drive
- % used later DM900 and DM3000 series only
- 1 used dual port drives only
- $ used dual port adapter (DP900) only, signal not at drives
  - Priority Select (DP900-2), replaced with Release Reservation (DP900-J)
  - Selected To Other Port (DP900-2) replaced with Reserved To Partner (DP900-J)
  - Request Deselect and Receive Deselect used DP900-2 only

CONTROL UNIT

DISK DRIVE

940
980
9100
9200
9300
<table>
<thead>
<tr>
<th>MODEL</th>
<th>CAPACITY (Megabytes)</th>
<th>DISK SPEED (RPM)</th>
<th>DATA TRANSFER RATE (MHz)</th>
<th>NUMBER OF CYLINDERS</th>
<th>NUMBER OF HEADS</th>
</tr>
</thead>
<tbody>
<tr>
<td>940</td>
<td>40</td>
<td>3600</td>
<td>9.67</td>
<td>411</td>
<td>5</td>
</tr>
<tr>
<td>980</td>
<td>80</td>
<td>3600</td>
<td>9.67</td>
<td>823</td>
<td>5</td>
</tr>
<tr>
<td>9160</td>
<td>160</td>
<td>3600</td>
<td>9.67</td>
<td>1645</td>
<td>5</td>
</tr>
<tr>
<td>9100</td>
<td>100</td>
<td>3600</td>
<td>6.45</td>
<td>404/411</td>
<td>19</td>
</tr>
<tr>
<td>9200</td>
<td>200</td>
<td>3600</td>
<td>6.45</td>
<td>808/815</td>
<td>19</td>
</tr>
<tr>
<td>9300</td>
<td>300</td>
<td>3600</td>
<td>9.67</td>
<td>808/815</td>
<td>19</td>
</tr>
</tbody>
</table>

COMPARISON OF DM900 SERIES DRIVES

DM900 SERIES READ/WRITE OPTIONS
STANDARD INTERFACE

Refer to Round Cable Assy.

CONTROL SIGNALS

READ/WRITE SIGNALS
Read Data and Clock
Write Data and Clock
Servo Clock

CABLES -
MAXIMUM LENGTH -
CONTROL ➔ 100 ft
R/W ➔ 100 ft cumulative when "Daisy-Chain"
INTERCHANGEABILITY -
DM9100, 9200, 9300 cables will interchange with
DM940, 980 cables; but not vice-versa.
The physical connector body differs

TERMINATORS are interchangeable
CABLES -

MAXIMUM LENGTH -

CONTROL  =  100 ft
100 ft cumulative when "Daisy-Chain"
R/W       =  100 ft
# COMMAND DECODE

## FUNCTION TAGS

<table>
<thead>
<tr>
<th>SET CYLINDER</th>
<th>SET HEAD</th>
<th>CONTROL SELECT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TAG 1</strong></td>
<td><strong>TAG 2</strong></td>
<td><strong>TAG 3</strong></td>
</tr>
<tr>
<td>0</td>
<td>CAR 1</td>
<td>WRITE GATE</td>
</tr>
<tr>
<td>1</td>
<td>CAR 2</td>
<td>READ GATE</td>
</tr>
<tr>
<td>2</td>
<td>CAR 4</td>
<td>OFFSET FORWARD</td>
</tr>
<tr>
<td>3</td>
<td>CAR 8</td>
<td>OFFSET REVERSE</td>
</tr>
<tr>
<td>4</td>
<td>CAR 16</td>
<td>FAULT RESET</td>
</tr>
<tr>
<td>5</td>
<td>CAR 32</td>
<td>ADDRESS MARK</td>
</tr>
<tr>
<td>6</td>
<td>CAR 64</td>
<td>REZERO</td>
</tr>
<tr>
<td>7</td>
<td>CAR 128</td>
<td>EARLY DATA STROBE</td>
</tr>
<tr>
<td>8</td>
<td>CAR 256</td>
<td>LATE DATA STROBE</td>
</tr>
<tr>
<td>9</td>
<td>CAR 512</td>
<td>RELEASE RESERVATION</td>
</tr>
</tbody>
</table>

*CONTROL SELECT present when SELECT ENABLE received on Dual Port drives causes a "PRIORITY SELECT"*

Bus line should go active min. of 200 ns before Tag line

Tag line should be minimum of 1 μSec duration
DM940/DM980/DM9300 SECTOR FORMAT

INDEX OR SECTOR

READ TO WRITE SPLICE

GAP 1
27 BYTES ZEROS
1 BYTE ONES
5 BYTES

GAP 2
1 BYTE ZERO
11 BYTES
7 BYTES
ZEROS (MIN)
1 BYTE

EOR
64 BYTES (FOR A 32 SECTOR TRACK)
7 BYTES
1 BYTE
ZEROS

EOR
GAP 3
8 BYTES
ZEROS (MIN)

HEAD SELECT

READ TIMING

HEAD SELECT

READ GATE

VALID NRZ READ DATA

READ TIMING

UPDATE WRITE TIMING

WRITE GATE

VALID DATA WRITTEN

T1 = 5 μsec, MINIMUM, 49 CLOCK COUNTS.
T2 = 6.02 μsec, 87 CLOCK COUNTS.
T3 = 100 μsec, 1 CLOCK COUNT, MINIMUM.
T4 = 9.0 μsec, 87 CLOCK COUNTS.
T5 = 0.3 μsec, 3 CLOCK COUNTS.
T6 = 0.1 μsec, 1 CLOCK COUNT.

TOTAL TRACK CAPACITY = (REQUIRED GAPS AND SYNC BYTE) - (USER DETERMINED ADDRESS, ASSOCIATED GAPS, AND SYNC BYTE) - (USER DETERMINED DATA FIELD ECC OR CRC).

FOR ABOVE EXAMPLE: DATA FIELD = 20160 / 32 = 625 - 37 = 257 = 630 - 37 - 25 - 7 = 616 BYTES / SECTOR.

EFFICIENCY = 616 × 32 / 20160 × 100 = 89%.

USAGE AND SIZE DETERMINED BY USER.
NOTE THAT THE READ GATE, FOLLOWING THE SPLICE, MUST BE RAISED SUCH THAT AT LEAST 11 BYTES REMAIN IN THE SYNC FIELD.
DM940/DM980/DM9300 VARIABLE LENGTH RECORD FORMAT

REPEATED X TIMES ON THE TRACK (WHERE X IS DEPENDENT UPON THE SIZES OF THE VARIABLE LENGTH RECORDS).

INDEX

READ TO WRITE SPICE

INDEX

<table>
<thead>
<tr>
<th>GAP1</th>
<th>AM</th>
<th>GAP2</th>
<th>SI</th>
<th>ADDR</th>
<th>ECC</th>
<th>EOB</th>
<th>GAP3</th>
<th>S2</th>
<th>DATA FIELD</th>
<th>ECC</th>
<th>EOB</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 BYTES</td>
<td>3 BYTES</td>
<td>11 BYTES</td>
<td>5 BYTES</td>
<td>7 BYTES</td>
<td>11 BYTES</td>
<td>1 BYTES</td>
<td>USER DETERMINED LENGTH</td>
<td>7 BYTES</td>
<td>1 BYTES</td>
<td>6 BYTES ZEROS (MIN)</td>
<td></td>
</tr>
<tr>
<td>ZEROS</td>
<td>NO TRANS</td>
<td>ZEROS (MIN)</td>
<td>ONE</td>
<td>ONE</td>
<td>ONE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

WRITE GATE

AM WRITE TIMING

ADDRESS MARK ENABLE

HEAD SELECT

HEAD SELECT

READ GATE

AM ENABLE

AM FOUND

VALID NRZ READ DATA

READ TIMING WITH AM

UPDATE WRITE TIMING WITH AM

HEAD SELECT

READ GATE

AM ENABLE

AM FOUND

WRITE GATE

VALID DATA WRITTEN

T1 = 16 BYTES MINIMUM, 128 CLOCK COUNTS.
T2 = 3 BYTES MINIMUM, 24 CLOCK COUNTS
T3 = 5.0 usec MINIMUM, 49 CLOCK COUNTS
T4 = 5.0 usec MINIMUM, 49 CLOCK COUNTS
T5 = 200 nsec MINIMUM OR WILL MISS THIS AM.
T6 = 0 usec MINIMUM, 0 CLOCK COUNTS.
T7 = 1.0 usec MAXIMUM, 10 CLOCK COUNTS.
T8 = 9.0 usec, 87 CLOCK COUNTS.
T9 = 9.0 usec, 87 CLOCK COUNTS.
T10 = 0.5 usec, 5 CLOCK COUNTS.
T11 = 0.1 usec, 1 CLOCK COUNT.
T12 = 100 nsec, 1 CLOCK COUNT, MINIMUM.
T13 = 6.0 ± 1.5 usec, 58 ± 15 CLOCK COUNTS.

USAGE AND SIZE DETERMINED BY USER.
NOTE THAT THE READ GATE, FOLLOWING THE SPlice, MUST BE RAISED SUCH THAT AT LEAST 11 ZERO BYTES REMAIN IN THE SYNC FIELD.
DM9100/DM9200 SECTOR FORMAT

INDEX OR SECTOR

READ TO WRITE SPlice

GAP 1

S1

ADDR

ECC

CRC

GAP 2

S2

DATA FIELD

ECC

CRC

GAP 3

SECTOR

27 BYTES ZEROS (MIN)

1 BYTES ONES

1 BYTE ZEROS

17 BYTES

ZEROS (MIN)

1 BYTE ZEROS

FOR A 32 SECTOR TRACK

5 BYTES ZEROS (MIN)

READ TIMING

VALID NRZ READ DATA

UPDATE WRITE TIMING

WRITE GATE

VALID DATA WRITTEN

T1 = 5 μsec MINIMUM, 33 CLOCK COUNTS.
T2 = 6.0 X 0.5 μsec, 33 X 4 CLOCK COUNTS.
T3 = 100 μsec, 1 CLOCK COUNT, MINIMUM.
T4 = 210 μsec, 7 3/4 CLOCK COUNTS, for FAST SYNC version.
T5 = 0.3 μsec, 2 CLOCK COUNTS.
T6 = 0.1 μsec, 1 CLOCK COUNT.

DATA FIELD LENGTH (PER SECTOR) = TOTAL TRACK CAPACITY

NUMBER OF SECTORS

FOR ABOVE EXAMPLE: DATA FIELD = 348 X 32

EFFICIENCY = 348 X 32 / 3440 X 100 = 82.9%.

NOTE:

ALL DUAL PORT OR RIBBON INTERFACE DRIVES ARE CONSTRUCTED WITH FAST SYNCH, OTHER DRIVES CAN BE MODIFIED FOR FAST SYNCH.
DM9100/DM9200 VARIABLE LENGTH RECORD FORMAT

INDEX

GAP 1            AM              GAP 2            51              ECC              ECC
10 BYTES         3 BYTES        17 (8) BYTES     ECC              DATA FIELD
ZEROS            NO TRANSMISSION ONES      (MIN)            (MIN)          ECC

REPEATED X TIMES ON THE TRACK (WHERE X IS DEPENDENT UPON THE SIZES OF THE VARIABLE LENGTH RECORDS).

READ TO WRITE SPICE

INDEX

GAP 4
5 BYTES ZEROS (MIN)

WRITE GATE

AM WRITE TIMING

ADDRESS MARK ENABLE

HEAD SELECT

READ TIMING WITH AM

HEAD SELECT

READ GATE

AM ENABLE

AM FOUND

VALID NRZ READ DATA

T13 = 10 BYTES MINIMUM, 80 CLOCK COUNTS.
T2 = 3 BYTES MINIMUM, 24 CLOCK COUNTS
T3 = 5.0 nsec MINIMUM, 33 CLOCK COUNTS.
T4 = 5.0 nsec MINIMUM, 33 CLOCK COUNTS.
T5 = 200 nsec MINIMUM OR WILL MISS THIS AM.
T6 = 0 nsec MINIMUM, 0 CLOCK COUNTS.
T7 = 1.0 nsec MAXIMUM, 7 CLOCK COUNTS.
T8 = 2.0 nsec, 136 CLOCK COUNTS (8.0 nsec, 87 CLOCK COUNTS, for FAST SYNC version).
T9 = 2.0 nsec, 136 CLOCK COUNTS (8.0 nsec, 87 CLOCK COUNTS, for FAST SYNC version).
T10 = 0.3 nsec, 2 CLOCK COUNTS.
T11 = 0.1 nsec, 1 CLOCK COUNT.
T12 = 100 nsec, 1 CLOCK COUNT, MINIMUM.
T13 = 6.0 ± 0.5 nsec, 39 ± 4 CLOCK COUNTS.

USAGE AND SIZE DETERMINED BY USER.

NOTE THAT THE READ GATE, FOLLOWING THE SPICE, MUST BE RAISED SUCH THAT AT LEAST 11 ZEROS BYTES REMAIN IN THE SYNC FIELD.

8 BYTES ZEROS (MINIMUM) FOR FAST SYNC VERSION OF THE DRIVE.

NOTE -

ALL DUAL PORT OR RIBBON INTERFACE DRIVES ARE CONSTRUCTED WITH FAST SYNC, OTHER DRIVES CAN BE MODIFIED FOR FAST SYNC.
CONTROL TIMING

- T1: 200 ns + cable delay
- T2: 1 us minimum (valid Read Data - MFM)
- T3: 1 us minimum (valid Read Data - NRZ)
- T4: 200 ns minimum (Write to Read)
- T5: 250 ns minimum (Read to Write)
- T6: 5 us minimum (Write or Read)
- T7: 1 us minimum (Write Current buildup)
- T8: 1 us maximum (valid Read Data - MFM)
- T9: 300 ns minimum (Write to Read)
- T10: 1 us maximum (Write Current buildup)
- T11: 3 ms maximum
**DRIVE SELECTION INTERFACE TIMING**

DEVICE SELECT - logical address
SELECT ENABLE
Module ID Active
SELECTED
Interface Enabled
UNIT SELECTED
ON CYLINDER
SEEK END

- Module ID Active is held "active" when the drive is selected; this prevents disruption of the drive, should the ID plug be removed during an operation.
- Selection may be dropped during Rezero or Seek operations only; when dropped, status is via Seek End.

**REZERO INTERFACE TIMING**

BUS OUT 6 - Rezero
TAG 3 - Control Select
Rezero Execution
READY
ON CYLINDER & SEEK END
Seek Incomplete time-out
SEEK INCOMPLETE
SEEK ERROR
SERVO DISABLE

- Tag 3 (Control Select) must remain "inactive" for 1 as minimum following receipt of On Cylinder or termination of previous Select operations.
- Drive Selection may be dropped during rezero execution.
SEEK INTERFACE TIMING

BUS OUT - new seek address
TAG 1 - Set Cylinder
Calculate seek distance & direction
Maximum Address Fault check
Load seek distance & direction
BUS OUT to CAR

Seek Execution - DC=0
READY
ON CYLINDER & SEEK END

Seek Execution - DC≠0
READY
ON CYLINDER & SEEK END
Seek Incomplete time-out
SEEK INCOMPLETE
SEEK ERROR
SERVO DISABLE

SEEK INCOMPLETE - max odd fault
READY
ON CYLINDER & SEEK END
SEEK ERROR
SERVO DISABLE

- Tag 1 (Set Cylinder) must remain "inactive" for 1 us minimum following receipt of On Cylinder or termination of any Control Select operation
- Drive Selection may be dropped during seek execution
READ INTERFACE TIMING

BUS OUT - head number
TAG 2 - Set Head
BUS OUT to HAR
TAG 3 - Control Select

BUS OUT 1/7,8 - Read/Data Strobe
MFM Read Data
Valid NRZ Read Data & Read Clock

BUS OUT 1/7,8 - Read/Data Strobe
BUS OUT 5 - Address Mark
MFM Read Data
ADDRESS MARK
Valid NRZ Read Data & Read Clock

BUS OUT 1/7,8 - Read/Data Strobe
BUS OUT 2,3 - Offset
Offset Execution
READY
ON CYLINDER & SEEK END
MFM Read Data
Valid NRZ Read Data & Read Clock

- 1 us minimum following a Read operation before another Control Select operation
- 3 ms minimum following an Offset Read operation before another Control Select operation
- 300 ns minimum delay between Write followed by Read
- 1 us minimum delay between Read followed by Write
- Device Selection must remain "Active" throughout entire Read operation
- Should a fault occur, the Read operation must be terminated and the Fault Reset
WRITE INTERFACE TIMING

- BUS OUT - head number
- TAG 2 - Set Head
- BUS OUT to HAR
- TAG 3 - Control Select
- BUS OUT 0 - Write
- Write Data & Write Clock
- Write Current
- Valid Write Data
- BUS OUT 0 - Write
- BUS OUT 5 - Address Mark
- Write Data & Write Clock
- Write Current
- Valid Write Data

1. 1 us minimum following a Write operation before another Control Select operation
2. 300 ns minimum delay between Write followed by Read
3. 1 us minimum delay between Read followed by Write
4. Device Selection must remain "active" throughout entire Write operation
5. Should a Fault occur, the Write operation must be terminated and the Fault Reset
CE DISK PACK LAYOUT
(DM-900 series)

APPLICATION

(Cyl. 1-3.5
Cyl. 4.5-6.5
Cyl. 10
Data Burst Timing
Outer Alignment Cylinder - Head 0, 4 only (used for radial tolerance check)
Even servo data)
Data Burst Timing

200
Data Burst Timing
242.5-244.5
245-247.5
(Even servo data)
Head Alignment Cylinder
Odd servo data

300
Data Burst Timing
317.5-319.5
320-322.5
330
(Even servo data)
Inner Alignment Cylinder - Head 0, 4 only (used for radial tolerance check)
Odd servo data
Maximum cylinder recorded on servo surface

245 is the most commonly used track for adjustments on a DM-980.

CAUTION

There are only 331 recorded servo tracks on the CE Pack. Attempting to do Sequential or Random seeks with the DMX900 tester can result in damage to both the drive and pack.
For general testing, use CDC Model 9876 or 9877 scratch pads or equivalent.

INDEX TO DATA BURST TIMING

To check Data Burst timing, sync positive on Index (AOE-TP1) while observing Read Signal (Read/Write Matrix - left end) CB.
Replace any heads not within 4 ± 2 μs, as specified, at cylinders 10, 200, and 300.

CDC Model 877-5i, or equivalent, provided with "Double Density" hub, replace hub to convert for "Single Density" to convert:
1. Very carefully lift cannister top off pack while depressing cover lock pin
2. Place pack on clean flat surface
3. Remove screws holding trim ring - remove trim ring
4. Lift out old hub - replace with new hub
5. Replace trim ring
6. Very carefully insert pack back into cannister top while depressing cover lock pin
CAUTION - PACK MUST BE SECURELY LOCKED IN CANNISTER TOP

DM 9160 uses same pack as DM 940
DM900 VOLTAGE TEST POINTS

SINGLE PORT (ORIGINAL)

SINGLE PORT (CONVERTABLE)
DUAL PORT
DM9000 TESTER CONNECTIONS

SINGLE PORT

DUAL PORT

A PORT

B PORT

*CONNECTOR USED ONLY FOR SERVO BALANCE ADJUSTMENT OR HEAD ALIGNMENT. DO NOT CONNECT FOR OTHER TESTS.
DYNAMIC BRAKE MOUNTING

DECK PLATE

DYNAMIC BRAKE MAGNETIC

SPINDLE ASSEMBLY

BRAKE DISK

FLUX PATTERN

BRAKE DISK

DYNAMIC BRAKE MAGNETIC

(Speed sensor slots present DM3100/3200/3300 only)
DISK LAYOUT
TRACK FOLLOWING

THE SERVO SYSTEM IS "TRACK FOLLOWING" WHENEVER THE HEADS ARE LOCATED IN THE CENTER OF A SPECIFIC CYLINDER. THE SERVO SYSTEM MAINTAINS ACCURATE POSITIONING AT ANY SPECIFIC CYLINDER.

SERVO TRACKS

THE SERVO SYSTEM POSITIONS THE SERVO HEAD OVER THE BORDER BETWEEN TWO ADJACENT SERVO TRACKS. THIS BORDER BETWEEN SERVO TRACKS DEFINES THE CENTER OF A CYLINDER LOCATION.

TRACK ASSIGNMENTS

CONSISTS OF 12/24 ODD SERVO TRACKS
USED TO AID IN LOCATING CYLINDER 0 DURING HEAD LOADING AND REZERO OPERATIONS

OUTER GUARD BAND

HEAD LOADING ZONE
NO INFORMATION WRITTEN IN THIS AREA (ERASED)
HEADS ARE LOADED TOWARDS DISK SURFACE IN THIS AREA

SERVO TRACK AREA
CONSISTS OF ALTERNATELY PLACED EVEN AND ODD SERVO TRACKS

INNER GUARD BAND
CONSISTS OF 18/36 EVEN SERVO TRACKS

DATA SURFACES
(5 PER DISK PACK,
2 TOP SURFACES AND
3 BOTTOM SURFACES)

DATA TRACKS

DATA TRACK 410/822

DATA TRACK 0
DISK LAYOUT
TRACK ASSIGNMENTS

DISK PACK

HEAD LOADING ZONE
NO INFORMATION WRITTEN IN THIS AREA (ERASED).
HEADS ARE LOADED TOWARDS DISK SURFACE IN THIS AREA.

SERVO SURFACE
(1 PER DISK PACK)

DATA SURFACES
(19 PER DISK PACK,
9 TOP SURFACES AND
10 BOTTOM SURFACES)

SERVO TRACK AREA
CONSISTS OF 18/19 EVEN ODD SERVO TRACKS.
USED TO AID IN LOCATING CYLINDER B DURING HEAD LOADING AND REZERO OPERATIONS.

INNER GUARD BAND
CONSISTS OF 18/19 EVEN ODD SERVO TRACKS.

OUTER GUARD BAND

SERVO HEAD (ON TRACK)

DATA TRACKS
DATA CYLINDER CENTER LINES
(DEFINED BY BORDERS BETWEEN SERVO TRACKS)

DATA TRACK 0
DATA TRACK 110/216

SERVO TRACKS
EVEN ODD EVEN ODD

DATA HEAD (ON TRACK)

OUTER GUARD BAND

SERVO TRACK

SERVO/DATA TRACK RELATIONSHIPS
SERVO READ SIGNAL

SERVO CORRECTION

A + B = 0
ON-TRACK
NO CORRECTION
HEAD REMAINS IN CENTERED POSITION OF A CYLINDER

A + B = +
OFF-TRACK
SMALL AMOUNT OF CORRECTION REMAINS, HEAD REMAINS IN DIRECTION OF

A + B (0) = +
OFF-TRACK
MAXIMUM CORRECTION, HEAD REMAINS IN DIRECTION OF

A + B = +
OFF-TRACK
POSITION CORRECTED, HEAD REMAINS IN DIRECTION OF

A + B = -
OFF-TRACK
POSITION CORRECTED, HEAD REVERSES DIRECTION TO ORIGINAL POSITION

A + B = 0
ON-TRACK
HEAD BACK ON ORIGINAL CYLINDER
**HEAD POSITIONING OPERATIONS**

**LOAD HEADS**

- The heads are loaded into "flying" position, then moved to cylinder 000 after the disks reach the proper rotational speed.
- The heads are loaded when the drive is powered up or when the drive is restarted following a disk pack change.

**TRACK FOLLOW**

- The heads are maintaining proper position ("track following") at all times when the heads are loaded and the drive is not accomplishing a seek, a rezero, or an offset operation.

**OFFSET**

- During offset, the heads maintain position a specified number of microrinches on either side of cylinder center.
- Offset is used primarily for data error recovery.

**SEEK**

- During a seek, the heads are moved directly to the new cylinder position.
- Seeks can be initiated by the system or by the control unit.

**REZERO**

- During a rezero, the heads are repositioned over cylinder 000.
- Rezero is primarily used after a seek error to reestablish a known head position.
- Rezero can be initiated by the system or by the control unit.

**RETRACT**

- During retract, the heads are unloaded off the disk surface.
- Retract occurs when the drive is powered down or when the drive is stopped to allow a disk pack change.
HE HEAD LOADING CAM ACTION

1. THE CARRIAGE MOVES THE HEADS FORWARD AFTER THE DISK IS UP TO ROTATIONAL SPEED. TENSION ON THE HEAD ARMS KEEPS THEM ON THE CAM SURFACE.

2. THE HEADS DROP TOWARD THE DISK SURFACE WHEN THE INCLINED PORTION OF THE ARM Rides OVER THE CAM.

SERVO HEAD MOVEMENT

LOAD HEADS

REZERO

4-7
TACH VELOCITY CURVE

ACCELERATE TIME —
FULL CURRENT IS APPLIED TO THE LINEAR MOTOR TO RAPIDLY ACCELERATE THE CARRIAGE TOWARDS THE DESIRED CYLINDER. CARRIAGE VELOCITY IS COMPARED WITH THE DESIRED VELOCITY. WHEN THE DESIRED VELOCITY IS REACHED, THE SERVO CIRCUITRY BEGINS TO HOLD CARRIAGE VELOCITY CONSTANT.

CONSTANT VELOCITY TIME —
THE SERVO CIRCUITRY HOLDS CARRIAGE VELOCITY NEARLY CONSTANT BY APPLYING MINIMUM DRIVE CURRENT, SUFFICIENT TO OVERCOME FRICTION LOSSES, TO THE LINEAR MOTOR. THE CARRIAGE MOVES AT THIS CONSTANT VELOCITY UNTIL NECESSARY TO DECELERATE IN PREPARATION TO STOPPING.

DECELERATE TIME —
AS THE CARRIAGE APPROACHES ITS DESTINATION, THE SERVO CIRCUITRY APPLIES BRAKING CURRENT CAUSING THE CARRIAGE TO DECELERATE. CARRIAGE DECELERATION CONTINUES UNTIL 250 MICROINCHES BEFORE DESTINATION; THE SERVO CIRCUITRY PREPARES TO STOP THE CARRIAGE AT THE DESIRED CYLINDER.

TRACK FOLLOWING —
WHEN THE CARRIAGE STOPS AT THE DESIRED CYLINDER, THE SERVO CIRCUITRY BEGINS TO “TRACK FOLLOW”.

SPEED UP

COAST

BRAKE

PARK
SERVO POSITION SIGNAL GENERATION

PHASE LOCKED MULTIPLIER

(9.67 or 6.45 MHz) SERVO CLOCK

(806 KHz) 2F SERVO CLOCK

(403 KHz) SERVO CLOCK

SERVO PULSES

DESTINATION CYLINDER (EVEN)

PHASE LOCKED LOOP

SERVO LOCK

GATING CIRCUITS

ODD CYL

POS LEVEL DETECT

NEG LEVEL DETECT

SERVO GATE EVEN

LEVEL DETECTORS

(BALANCE)

+15 <- \[ \ldots \] \[ \ldots \] <- -15

POSITION AMPLIFIER

SERVO HEAD

SERVO AMP

AMP

BUFFER AMP

POLARITY SWITCH

PEAK DETECTORS

POSITION AMP

FINE/COARSE TRACK DETECTORS

COARSE TRACK

HEADS LOADED

HEADS LOADED

PRE AMP

SERVO AMP

AGC COMPARATOR

(GAIN)
SERVO GATING

EVEN DESTINATION

SAMP-A
SERVO READ SIGNAL

SOSC-L
SERVO OSCILLATOR

S403-H
SERVO CLOCK

SGTE-H
SERVO GATE EVEN

ODD DESTINATION

SAMP-A
SERVO READ SIGNAL

SOSC-L
SERVO OSCILLATOR

S403-H
SERVO CLOCK

SGTE-H
SERVO GATE EVEN
SERVO PULSE GENERATION
EVEN DESTINATION

SAMP-A
SERVO READ SIGNAL

SOSC-L
SERVO OSCILLATOR

DETP-L
DETECT POSITIVE LEVEL

DETN-H
DETECT NEGATIVE LEVEL

SPUL-H
SERVO PULSE

ODD DESTINATION

SAMP-A
SERVO READ SIGNAL

SOSC-L
SERVO OSCILLATOR

DETP-L
DETECT POSITIVE LEVEL

DETN-H
DETECT NEGATIVE LEVEL

SPUL-H
SERVO PULSE
POSITION AMPLIFIER SIGNAL

Outer Guard Band

Odd Servo Track Recorded for 12/24 Track Widths

Even Servo Track

Odd Servo Track

Even Servo Track

Odd Servo Track

Even Servo Track

Cyl 0 1 2 3 4 5

Even Servo Track

Odd Servo Track

Even Servo Track

Odd Servo Track

Even Servo Track

PAMP-A
Position Amplifier

PAMP-A
(Even Cylinder Destination)
Position Amplifier

PAMP-A
(Odd Cylinder Destination)
Position Amplifier

4-12
CYLINDER AND COUNT PULSE GENERATION

PAMP-A
POSITION AMPLIFIER

FTKS-H
FINE TRACK

CTKS-H
COARSE TRACK

CPUL-H
CYLINDER PULSE

CDCC-L
DECREMENT DC (COUNT PULSE)
INDEX GAP SENSING

SCK0-H  
SERVO CLOCK  
(SERVO OSCILLATOR)

SPLUL-H  
SERVO PULSE

FF15

FF25

INDEX SENSING

SCK0-H  
SERVO CLOCK  
(SERVO OSCILLATOR)

SPLUL-H  
SERVO PULSE

806  
KHZ.  
76 KHz.

FF15

SR CLOCK TIME

BIT SHIFTED IN  
"0"  
"0"  
"0"  
"0"  
"0"  
"0"  
"0"  
"0"

INDEX-H  
INDEX SENSE
TACH VELOCITY CURVE

ACCELERATE TIME —
FULL CURRENT IS APPLIED TO THE LINEAR MOTOR TO RAPIDLY ACCELERATE THE CARRIAGE TOWARDS THE DESIRED CYLINDER, CARRIAGE VELOCITY IS COMPARED WITH THE DESIRED VELOCITY. WHEN THE DESIRED VELOCITY IS REACHED, THE SERVO CIRCUITRY BEGINS TO HOLD CARRIAGE VELOCITY CONSTANT.

CONSTANT VELOCITY TIME —
THE SERVO CIRCUITRY HOLDS CARRIAGE VELOCITY NEARLY CONSTANT BY APPLYING MINIMUM DRIVE CURRENT, SUFFICIENT TO OVERCOME FRICTION LOSSES, TO THE LINEAR MOTOR. THE CARRIAGE MOVES AT THIS CONSTANT VELOCITY UNTIL NECESSARY TO DECELERATE IN PREPARATION TO STOPPING.

DECELERATE TIME —
AS THE CARRIAGE APPROACHES ITS DESTINATION, THE SERVO CIRCUITRY APPLIES BRAKING CURRENT CAUSING THE CARRIAGE TO DECELERATE. CARRIAGE DECELERATION CONTINUES UNTIL 250 MICROINCHES BEFORE DESTINATION; THE SERVO CIRCUITRY PREPARES TO STOP THE CARRIAGE AT THE DESIRED CYLINDER.

TRACK FOLLOWING —
WHEN THE CARRIAGE STOPS AT THE DESIRED CYLINDER, THE SERVO CIRCUITRY BEGINS TO "TRACK FOLLOW".
*represents contamination build up on disk surfaces.

**Optimum Performance**
Recording head and disk surface are perfectly clean, and the gap between the head and the recorded data is an ideal 40 microinches.

**Retry Level**
Contamination (dust, dirt, smog, pollen, smoke, etc.) has started to build up on recording head and disk surface, forcing head away from the recorded data, causing a problem recovering data. After several retries, data is recovered, and the job proceeds.

**Data Check Level**
Contamination build up has forced the head so high it cannot recover data. Corrective cleaning action is mandatory at this time.

**Head Crash Level**
Contamination builds up unevenly, resulting in erratic head flying pattern, and eventual contact between the head and disk surface.

**Chronology of Contamination**
(9.67 MHz)

CELL TIME - 103.3 nsec

50 nsec

DM940, DM 980, DM 9300

(6.45 MHz)

CELL TIME - 155 nsec

55 nsec

DM 9100, DM 9200
HEAD SCANNING

HEAD OUTPUT
WRITE
READ

Write Clock
(from servo clock)

NRZ Write Data

Precompensated MFM Write Data

Write Current Flux Changes

WRITE

READ

Read Signal at Head

Read Signal
(amplified and time corrected)

MFM Read Data

NRZ Read Data

Read Clock
(from MFM Read Data)
DISK SURFACES

(Viewed from motor)

DM940, DM980

DISK SURFACES

(Viewed from motor)

DM9100, DM9200, DM9300
DATA STROBE TIMING

DATA STROBE TIMING IS DETERMINED BY WHEN THE STROBE VOLTAGE Passes THROUGH THE REFERENCE VOLTAGE.
(LESS NEGATIVE IS EARLY)
DATA STROBE TIMING CAN BE SHIFTED 3 MS EARLY OR 3 MS LATE.
WRITE PRE-COMPENSATION TIMING

Timing is determined by when the ramp voltage passes through the reference voltage. (Less negative is early.)

WRITE PRE-COMPENSATION TIMING CAN BE SHIFTED A MINIMUM OF 3 ns EARLY OR 3 ns LATE.

6-14
<table>
<thead>
<tr>
<th>Mode</th>
<th>Mode</th>
<th>Mode</th>
<th>Mode</th>
<th>Mode</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 REZERD</td>
<td>2 SEEK</td>
<td>4 HEAD LOAD</td>
<td>6 READ</td>
<td>7 WRITE</td>
<td></td>
</tr>
<tr>
<td><strong>State 1</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse Latch</td>
<td>Velocity Enable AND NOT State 2</td>
<td>Launch Velocity AND NOT Heads Extended</td>
<td>Squelch</td>
<td>Write Select</td>
<td></td>
</tr>
<tr>
<td><strong>State 2</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rezero Velocity AND State 1</td>
<td>Drive Current Sense AND State 1</td>
<td>Launch Velocity AND Heads Extended</td>
<td>Read Select AND State 1</td>
<td>Write Current Sense AND State 1</td>
<td></td>
</tr>
<tr>
<td><strong>State 3</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NOT Heads Loaded AND State 2</td>
<td>NOT Coarse Track AND State 2</td>
<td>NOT Heads Loaded AND State 2</td>
<td>NOT Squelch AND State 2</td>
<td>(AC Safe OR Write AM) AND State 2</td>
<td></td>
</tr>
<tr>
<td><strong>State 4</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Launch Velocity AND Forward AND State 3</td>
<td>Fine Track AND State 3</td>
<td>Launch AND Forward AND State 3</td>
<td>Squelch AND State 3</td>
<td>State 2 AND State 3</td>
<td></td>
</tr>
<tr>
<td><strong>State 5</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NOT Heads Loaded AND Allow Guard Band AND State 4</td>
<td>Difference Count Equal Zero AND State 2</td>
<td>NOT Heads Loaded AND Allow Guard Band AND State 4</td>
<td>Multiple Write Current</td>
<td>Multiple Write Current</td>
<td></td>
</tr>
<tr>
<td><strong>State 6</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slow Forward AND State 5</td>
<td>Lock-On Latch AND State 2</td>
<td>Slow Forward AND State 5</td>
<td>Multiple Head Select</td>
<td>Multiple Head Select</td>
<td></td>
</tr>
<tr>
<td><strong>State 7</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Heads Loaded AND Allow Guard Band AND State 4 AND State 6</td>
<td>NOT Drive Current Sense AND Lock-On Delayed AND State 6</td>
<td>Heads Loaded AND Allow Guard Band AND State 4 AND State 6</td>
<td>NOT (On-Line AND Ready) AND (Read Select OR Write) AND NOT Fine Track</td>
<td>Write AND (Fine Track OR Read Select AND NOT Ready AND On-Line)</td>
<td></td>
</tr>
<tr>
<td><strong>State 8</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lock-On Latch AND State 7</td>
<td>Seek Latch Delayed AND NOT Coarse Track AND Fine Track</td>
<td>Lock-On Latch AND State 7</td>
<td>Write Current AND State 4</td>
<td>Index Error</td>
<td></td>
</tr>
<tr>
<td><strong>Clear MODE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>State 8 AND Lock-On Delayed</td>
<td>State 8 AND Lock-On Delayed</td>
<td>NOT Read Select AND State 4</td>
<td>State 4 AND NOT Write Gate</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
RIBBON INTERFACE

1. GENERAL DESCRIPTION

The ribbon-cable version of the DM940 and DM980 drive differs from the round-cable version only in the physical interface to the control unit. This interface consists of a connector panel assembly located on the right rear section of the drive, two cable harnesses (H1 and H2) which provide internal signal connections between the connector panel assembly and the logic chassis mother board, two flat ribbon-type input/output cables, and a line terminator plug. In addition, the Read Data Latch/Operator Control Panel PC board, DLOCP in logic chassis location A08, is replaced by a new DLOCP board, P/N 3306203-01. The read/write cable line transmitters and receivers located on this board have 68-ohm terminating resistors rather than the 82-ohm resistors that were used for the standard round-cable interface.

2. CONNECTOR AND CABLE REQUIREMENTS

Connectors (headers) for the flat ribbon-type input/output cables are mounted on the connector panel assembly located on the right rear area of the drive chassis (see figure 1). For single-port operation (i.e., interface with only one control unit), only the A port connectors are provided. Table 1 lists these connectors and defines their cabling requirements.

<table>
<thead>
<tr>
<th>TABLE 1. CONNECTOR AND CABLE REQUIREMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NAME</strong></td>
</tr>
<tr>
<td>Control Cable</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Read/Write Cable</td>
</tr>
</tbody>
</table>

* A control terminator assembly, P/N 3306223-01, must be installed in connector J1 if the drive is the only drive (radial configuration) or is the last drive in a daisy-chain configuration.

The cable connectors on both the control and read/write cables are standard insulation displacement-type connectors designed for use with ribbon cable. The input/output cable assemblies, together with their parts lists and wire lists, are included in the applicable drawings section of this supplement.

3. SYSTEM CABLING CONFIGURATION

The control, read/write, and AC power cables are connected to a system of drives in daisy-chain. The drives may also be attached to the control unit in radial fashion; however, this requires a separate control cable (from the control unit) and a line terminator for each drive.
FIGURE 1. CONNECTOR PANEL ASSEMBLY AND SYSTEM CABLES
QUIET ENCLOSURE

SECTION I

GENERAL INFORMATION

1-1. GENERAL

The Ampex DM900 Quiet Enclosure is designed to house all models of the DM900-series disk storage drive. This configuration permits operation of the drive in an office, or similar environment, without noticeable increase in noise level.

1-2. EQUIPMENT DESCRIPTION

The quiet enclosure is constructed of a durable tubular steel frame with removable top, front, rear, and side panels. Each panel contains heavy layers of sound-deadening foam-type materials that are flame-retardant and provide natural sound isolation to noises generated within the disk drive.

The enclosure measures 39-3/8 inches high, 36 inches deep, and 21 inches wide, and requires only slightly more floor space than the standard drive console.

Operating controls and indicators are mounted on the front panel and are easily accessible to the operator. During normal operation, the operator does not require access to the drive unless installing or removing a disk pack. When maintenance is required, all panels can be rapidly removed to provide access to internal components.

The design of the enclosure permits unrestricted airflow. Room air enters through a removable pre-filter located on the bottom front of the cabinet frame. A vertical bulkhead, separating the front and rear areas of the enclosure frame, directs the airflow upwards and then from the front to the rear of the drive. The air is expelled downwards through a cutout on the bottom rear section of the enclosure frame. A neoprene curtain, across the bottom of the drive, prevents the warm expelled air from re-entering the enclosure.

1-3. EQUIPMENT CONFIGURATIONS

The DM900 Quiet Enclosure is normally available from the factory as a complete unit including the specified DM900-series disk storage drive. If desired, the enclosure may be ordered without the drive, thus permitting an existing standard drive to be removed from its console and field-installed into the quiet enclosure.
SECTION II
INSTALLATION INSTRUCTIONS

2.1. GENERAL

This section provides instructions for removing the quiet enclosure panels to provide access to the disk drive. All other procedures for unpacking, installing, and checking out the disk drive are contained in section II of the applicable operation and maintenance manual provided with the DM900-series disk drive.

2.2. REMOVAL OF QUIET ENCLOSURE PANELS

The rear, front, side, and top panels of the quiet enclosure may be removed by referring to figure 2-1 and performing the following procedure.

a. To remove rear panel ⊙, depress latches ◊, and lift panel up and slightly away from the frame. Disconnect ground wire from panel.

NOTE

A separate ground wire provides an electrical connection from each panel to the enclosure frame. If a panel is to be completely removed, the ground wire must first be disconnected from its jack on the inside of the panel.

b. To open the front panel ⊙, turn latch handle ◊, located at machine rear, from the 3 o’clock (CLOSE) position to the 12 o’clock (OPEN) position. Swing front panel open; it will remain at near vertical position due to an attaching cable. (To completely remove the front panel, disconnect the attaching cable, the ground wire, and the control panel harness connector.)

c. To remove the side panel ⊙, first remove the top rear panel ⊙ by exerting pressure and lifting up. (The top panel is secured to the side panels by means of ball studs.) Use fingers, screwdriver, or coin to loosen two screws ◊, disconnect ground wire, then lift side panel ⊙ up and away from frame.
FIGURE 2-1. REMOVAL OF QUIET ENCLOSURE PANELS
### Read/Write Head Identification

<table>
<thead>
<tr>
<th>Drive</th>
<th>Qty</th>
<th>Location</th>
<th>Part Number</th>
<th>Connector Color</th>
<th>Head Identification</th>
</tr>
</thead>
<tbody>
<tr>
<td>DM312</td>
<td>5</td>
<td>LU</td>
<td>3300576-01</td>
<td>White</td>
<td></td>
</tr>
<tr>
<td>DM313</td>
<td>5</td>
<td>LD</td>
<td>3300577-01</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>RU</td>
<td>3300578-01</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>RD</td>
<td>3300579-01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM322</td>
<td>5</td>
<td>LU</td>
<td>3300576-02</td>
<td>Blue</td>
<td></td>
</tr>
<tr>
<td>DM323</td>
<td>5</td>
<td>LD</td>
<td>3300577-02</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>RU</td>
<td>3300578-02</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>RD</td>
<td>3300579-02</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM330&lt;sup&gt;1&lt;/sup&gt;</td>
<td>5</td>
<td>LU</td>
<td>3302527-01</td>
<td>Orange(Green)</td>
<td></td>
</tr>
<tr>
<td>DM9100</td>
<td>5</td>
<td>LD</td>
<td>3302528-01</td>
<td>Red(Red)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>RU</td>
<td>3302525-01</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>RD</td>
<td>3302526-01</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Servo</td>
<td>3302535-01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM331</td>
<td>5</td>
<td>LU</td>
<td>028-017</td>
<td>Red</td>
<td></td>
</tr>
<tr>
<td>DM9200</td>
<td>4</td>
<td>LD</td>
<td>028-019</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>RU</td>
<td>028-016</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>RD</td>
<td>028-018</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Servo</td>
<td>028-020</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM9300</td>
<td>5</td>
<td>LU</td>
<td>3308047-01</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>LD</td>
<td>3308046-01</td>
<td>Pink</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>RU</td>
<td>3308045-01</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>RD</td>
<td>3308039-01</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Servo</td>
<td>028-020</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM940&lt;sup&gt;2&lt;/sup&gt;</td>
<td>3</td>
<td>LU</td>
<td>3307945-02</td>
<td>Blue</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>RD</td>
<td>3307945-01</td>
<td>Red</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Servo</td>
<td>3307945-03</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM980&lt;sup&gt;2&lt;/sup&gt;</td>
<td>3</td>
<td>LU</td>
<td>3307967-02</td>
<td>Orange</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>RD</td>
<td>3307967-01</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Servo</td>
<td>3307967-03</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM440&lt;sup&gt;3&lt;/sup&gt;</td>
<td>3</td>
<td>AU</td>
<td>HDA000095P5</td>
<td>Various</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>AD</td>
<td>HDA000095P1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>HDA000095P2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM445</td>
<td>2</td>
<td>AU</td>
<td>HDA000095P5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>AD</td>
<td>HDA000095P1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM441&lt;sup&gt;3&lt;/sup&gt;</td>
<td>1</td>
<td>AU</td>
<td>HDA000095P7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>AD</td>
<td>HDA000095P8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM447</td>
<td>1</td>
<td>AU</td>
<td>HDA000095P7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>AD</td>
<td>HDA000095P8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM443&lt;sup&gt;3&lt;/sup&gt;</td>
<td>2</td>
<td>AU</td>
<td>HDA000095P7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>AD</td>
<td>HDA000095P8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM448</td>
<td>2</td>
<td>AU</td>
<td>HDA000095P7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>AD</td>
<td>HDA000095P8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. DM330/DM9100 heads are marked two ways; by engraving connector plug, or by attaching decal to connector plug. When decal is attached to connector, plug color as indicated by numerals.

2. DM940/DM980 carriage redesigned. New heads used on original design carriage, screws must also be changed.

3. DM440 Series available 1500 or 2400 RPM. 1500 RPM heads identified by numerals.

---

8-1
DM900 CARRIAGE AND HEADS

A new carriage assembly is being used on DM900 drives which provides improved radial positioning of heads. The new carriage can be recognized by the prominent casting number visible on the casting when viewed from the logic gate side of the drive. New heads and screws are also used.

![Carriage Assembly Diagram]

The new part numbers are:

- 3307945-01  940 RD Head
- 3307945-02  940 LU Head
- 3307945-03  940 Servo Head
- 3307967-01  980 RD Head
- 3307967-02  980 LU Head
- 3307967-03  980 Servo Head
- 3307937-01  Head Mounting Screw

The new heads are usable on the old carriage assembly, provided new head mounting screws are also used.

NOTE: Old heads will not fit the new carriage assembly.

The head mounting tool used with the old heads can cause overflexing of the arm on the new heads during installation. This overflexing can cause the head to crash.

The head mounting tool can be modified to work with new heads by machining off surface "X" of "TAB" indicated; tab thickness must be reduced from .050" to .035".

![Head Mounting Tool Diagram]

If unable to have necessary machining done locally, request return authorization for Ampex to correct head mounting tool.

8-2
HEAD ALIGNMENT TIPS

1. The CE pack should be in the same room environment as the drive for 2 hours before mounting on the drive. The drive should then run a minimum of 45 minutes to temperature-stabilize the pack and drive before head alignment is checked or performed. If the pack has not been in the same temperature environment as the drive for 2 hours before installing, it should be run 1-1/2 hours before alignment. Temperature stabilization is critical.

2. Do servo gain and balance prior to head alignment.

3. Should servo head be moved or replaced, heads must be adjusted.
   
   NOTE: Correct position of servo head is back against positioning pin fitted into carriage assembly.

4. Heads must be aligned "off-line" using the DDH900.

5. Set initial head torque to just finger-tight; make final torque to 5.5 in/lbs.
   
   CAUTION: DO NOT MOVE SERVO HEAD. DO NOT OVER TORQUE; THE TORQUE WRENCH IS NON-RATCHETING.

6. Always make final adjustment moving head forward onto alignment track.

7. Try to hold head alignment to within ±25 μin; once heads have been aligned, do not realign unless they are out more than ±150 μin.

8. The heads are perfectly aligned when the alignment meter is nulled. Alignment meter null point is where no further change in meter reading is observed as the sign switch is toggled. Once the null point is found, align all heads to this reading.

   NOTE: Oscilloscope connected to align signal test point on tester front panel will display a balanced "DI-BIT" pattern at alignment track.
9. The alignment error is the difference between the reading in the + sign switch position and the meter null reading or the alignment error can be calculated by using the following equation:

\[
\text{ALIGNMENT ERROR} = \frac{(\text{POSITIVE READING}) - (\text{NEGATIVE READING})}{2}
\]

Positive Reading – Meter reading with Sign Switch in Positive position
Negative Reading – Meter reading with Sign Switch in Negative position

10. The alignment meter is calibrated for single density drives and the reading must be compensated when aligning double density drives. This difference in meter readings between single and double density drives is due to track spacing and the alignment signal employed.

![Diagram showing alignment error for single and double density drives]

11. To compensate the meter reading for double density,

1) Divide the reading on the meter by 2 for double density or
2) Set the meter range switch to 125 for single density and 250 for double density, always read the 125 scale.

**NOTE:** If the heads are forward of the alignment track, the meter will read + from the null when the sign switch is in the + position.
SUGGESTED PREVENTIVE MAINTENANCE ON
DM 900/9000 SERIES DISK DRIVES

The frequency of preventive maintenance required to ensure proper operation of the DM900/9000 series drives is dependent upon several factors including the number of hours used, cleanliness of the environment in which installed, number of pack changes made, length of time the pack shroud area is left with the pack door open, etc. Because of these variables, Ampex recommends the following as starting preventive maintenance intervals at any given site. If, at a specific site, it is found that no significant problems are identified when using the recommended starting intervals, it is suggested that the maintenance intervals be gradually lengthened. (In no case should the minimum interval be longer than 3 months, however). Conversely, if a number of problems are identified, the maintenance intervals should be shortened.

1. Operator Provided PM -- Performed as the Drive is Used

   This PM performed by an operator should be limited to a general visual inspection as follows:
   
   - Check front operator panel for broken lenses or switches or failing indicators
   - Inspect shroud area for dirt
   - Check pack door latch for proper operation

   If any problems are suspected, the operator should be advised to notify his customer engineer.

2. Monthly Preventive Maintenance:

   - Visual check including:
     
     Cable connections
     Front operator panel
     Pack door operation
     Shroud area for dirt

   - Heads should be inspected and cleaned only if necessary
   - Front bezel prefilter should be checked and replaced if necessary

3. Quarterly Preventive Maintenance:

   - Power supply checks
   - Servo adjustment check
   - Head alignment check

4. Semiannually Preventive Maintenance:

   - Check of the absolute filter
   - Carriage inspection and cleaning
   - Inspection of pack drive belt and pulleys

   - The following optional checks may also be performed:
     
     Power On/Off sequence
     Rezero operation check
     Write operation check
     Write Protect check
     Read operation check
PM PROCEDURE FOR ABSOLUTE FILTER

The absolute filter should be checked a minimum of twice a year. The following procedure will be based on use of Ampex pressure gauge part number 330937-01.

**DM9000:**

A. Remove the rear panel by pulling the top edge out, then lifting the panel off the machine, swing the logic chassis out.

B. Remove the rubber plug from the hole in the rear of the absolute filter.

C. Insert the gauge tube in the hole provided, start a pack spinning with select plug inserted in the drive to allow heads to load.

D. If the gauge shows less than .1 inches of water positive pressure, the absolute filter must be changed.

**DM900:**

A. Remove the front bezel assembly by removing the four #10 allen head socket screws from the front and pulling the bezel out.

B. Loosen the left deck plate hold down screw sufficiently to allow insertion of the air restrictor between absolute filter output and deck plate. (Template for restrictor included, may be cut from cardboard or any suitable material).

C. Remove the rubber plug from the hole in the front of the absolute filter.

D. Insert the gauge tube in the hole provided, start a pack spinning with select plug inserted in the drive to allow heads to load.

E. If the gauge shows less than .1 inches of water positive pressure, the absolute filter must be changed.

F. Be sure to remove air restrictor before returning drive to service.
POWER UP PROBLEM

Failure of DM900 drives to start pack rotation upon application of AC power can be corrected by the replacement of Signetic’s 9602 IC chip at location 5A on PCISX PCBA (A02) with a 9602 from another vendor.
Table 1-1. DM900-Series Special Tools and Accessories

<table>
<thead>
<tr>
<th>NOMENCLATURE</th>
<th>PART NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Head Alignment Tool</td>
<td>3306147-01</td>
</tr>
<tr>
<td>Head Mounting Tool</td>
<td>3306149-01</td>
</tr>
<tr>
<td>Torque-Limiting Screwdriver (Handle)</td>
<td>3302777-01</td>
</tr>
<tr>
<td>Head Torque Wrench Adapter (Bit)</td>
<td>3306148-01</td>
</tr>
<tr>
<td>Data Separator PCBA*</td>
<td>3305593-01</td>
</tr>
<tr>
<td>Card Extender</td>
<td>3300937-01</td>
</tr>
<tr>
<td>Filter Pressure Gage</td>
<td>3307203-01</td>
</tr>
<tr>
<td>Dual Port Tester Adaptor PCBA **</td>
<td>3308359-01</td>
</tr>
<tr>
<td>20 Pin Ribbon Cable **</td>
<td></td>
</tr>
</tbody>
</table>

* Required if drive does not have NRZ Read/Write capability.

** Required for testing of Dual Port drives.

Table 1-2. DM9000-Series Special Tools and Accessories

<table>
<thead>
<tr>
<th>NOMENCLATURE</th>
<th>PART NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial Head Positioning Tool</td>
<td>3302377-01</td>
</tr>
<tr>
<td>Torque-Limiting (6 in./lbs.)Screwdriver Assembly</td>
<td>3302778-01</td>
</tr>
<tr>
<td>Handle</td>
<td>3302777-01</td>
</tr>
<tr>
<td>Bit</td>
<td>360-416</td>
</tr>
<tr>
<td>Head Mounting Tool</td>
<td>3302379-01</td>
</tr>
<tr>
<td>Head Alignment</td>
<td>3302378-01</td>
</tr>
<tr>
<td>Paddleboard (PDDL1)</td>
<td>3301883-01</td>
</tr>
<tr>
<td>Data Separator PCBA *</td>
<td></td>
</tr>
<tr>
<td>Write Compensation PCBA **</td>
<td></td>
</tr>
<tr>
<td>Card Extender</td>
<td>3302153-01</td>
</tr>
<tr>
<td>Filter Pressure Gage</td>
<td>3300937-01</td>
</tr>
</tbody>
</table>

* Required for drives without NRZ Read capability.

** Required for drives without NRZ Write capability.
Test Point & Card Locations shown are for the Single-Port 2M-900 Series.

SERVO DI-BITS

SERVO POSITION SIGNALS
Even Cylinder

SERVO POSITION SIGNALS
Odd Cylinder
PEAK DETECTOR GATING
Even Cylinder

POSITION AMPLIFIER GENERATION
SERVO PULSE GENERATION

INDEX DETECTION
SERVO OPERATION
8 Track Seek
MFM ENCODING
Cylinder 364 - Head 3

MFM WRITE DATA
Cylinder 410 - Head 3

WRITE COMPENSATION
Cylinder 410 - Head 3
WRITE COMPENSATION CHECKS
TESTER READ TIMING
16 Track Seek

TESTER READ TIMING
16 Track Seek with Offset

TESTER READ TIMING
256 Track Seek with Offset
DM 940/980 LOAD

**SEQUENCE FLOW CHARTS**

**START**
- PIN 29-H
- AB2
- (SEQO)

**DOOR CLOSED**
- PIN 74-H
- AB2
- (DCSW)

**RUN & UPSPEED**
- PIN 32-H
- AB2
- (RUPS)

**UPSEED**
- PIN 32-H
- AB2
- (UPDO)

**HEADS RETRACTED**
- PIN 37-L
- AB2
- (HDEX)

**HOLD**
- PIN 41-L
- AB2
- (HOLD)

**SEQUENCE IN**
- PIN 40-H
- AB2
- (SQIN)

**NOTE**
- Used with RPQ-43

**BRUSH MOTOR RUN**
- PIN 23-L
- AB2
- (BRMR)

**BRUSH MOTOR STARTS**

**BRUSHES RETRACTED?**
- PIN 32-H
- AB2
- (SEQO)

**NO**
- BREX

**YES**
- BMRR

**BRUSH CYCLE REQUIRES APPROXIMATELY 15 SECONDS**

**RUN & UPSPEED**
- PIN 32-H
- AB2
- (RUPS)

**NO**
- BMRR

**YES**
- SEQO

**DROP SEQUENCE OUT**
- PIN 29-H
- AB2
- (SEQO)

**START PACK MOTOR LATCH**
- AB2

**PACK MOTOR RUN**
- PIN 25-L
- AB2
- (PMRN)

**ENERGIZE PACK MOTOR START & RUN WINDINGS**
- Pins 5-9-L
- AB2
- (PMSR, PMSR)

**PACK MOTOR STARTS**

**NO**
- A62

**YES**
- 5 MC

**PACK ON CHECK DELAY**

**75 RPM!**

**NO**
- A62

**YES**
- A62

**2500 RPM!**

**NO**
- A62

**YES**
- A62

**DROP PACK MOTOR RUN**
- PIN 25-H
- AB2
- (PMRN)

**DEENERGIZE PACK MOTOR START WINDING**
- PIN 5-9-H
- AB2
- (PMSR)

**NO**
- A62

**YES**
- A62

**DROP BRUSH MOTOR RUN**
- PIN 23-H
- AB2
- (BMRR)

**BRUSH MOTOR STARTS**

**NO**
- BMRR

**YES**
- SEQO

**STOP**

**BRUSH MOTOR STOPS**

**DYNAMIC BRAKE**
- PIN 21-L
- AB2
- (DBK)

**BRUSH MOTOR STOPS**

**DEENERGIZE PACK MOTOR START & RUN WINDINGS**
- Pins 5-9-H
- AB2
- (PMSR, PMSR)

**SHROUD AIR-PURGE DELAY**

**RESET START PACK MOTOR LATCH**
- AB2

**START PACK MOTOR LATCH**
- AB2

**MODULE ID PLUG IN**
- AB2

**RUN HOLD LATCH**
- AB2

**MAINTAIN PACK MOTOR RUN**
- PIN 25-L
- AB2
- (PMRN)

**SEQUENCE OUT**
- PIN 32-L
- AB2
- (SEQO)

**INITIAL LOAD**
- PIN 18-L
- AB2
- (INLD)

**INITIAL LOAD ENABLE LATCH**
- AB2

**INITIAL LOAD**
- PIN 32-L
- AB2
- (SEQO)
SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION

The Ampex DP900-1 and DP900-2 Dual-Port Adaptors (figure 1-1) are self-contained units which connect two controllers to one Ampex DM900 or DM9000-series disk drive, thus permitting access to the drive by either of the two controllers. In providing this access, the dual-port adaptor functions as a dynamic (or static) switch that routes the necessary control and data signals between the drive and the correct control unit. Once the appropriate connection has been made by either control unit, the dual-port adaptor is essentially transparent (e.g., the control unit can see right through the adaptor to the drive). The DP900-1 and DP900-2 are physically identical. The basic differences between the two units are in the control logic functions for selecting, reserving, and releasing the disk drive. These differences are described in detail in section III.

1-2. CHARACTERISTICS AND REQUIREMENTS

The characteristics and requirements of the DP900 Dual-Port Adaptors are listed in table 1-1.

![Dual-Port Adaptor Image](image-url)

FIGURE 1-1. DUAL-PORT ADAPTOR
TABLE 1-1. CHARACTERISTICS AND REQUIREMENTS

<table>
<thead>
<tr>
<th>PHYSICAL SIZE</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Length</td>
<td>19.445 inches (49.38 cm), plus length of connector</td>
</tr>
<tr>
<td>Width</td>
<td>13.875 inches (35.24 cm)</td>
</tr>
<tr>
<td>Height</td>
<td>5.0625 inches (12.76 cm)</td>
</tr>
<tr>
<td>WEIGHT</td>
<td>Approximately 23 lbs.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>POWER REQUIREMENTS</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Power</td>
<td>115 V ± 10%, 50 or 60 Hz, single phase or</td>
</tr>
<tr>
<td></td>
<td>230 V ± 10%, 50 or 60 Hz, single phase</td>
</tr>
<tr>
<td>DC Power</td>
<td>±5 VDC (±5%), internally supplied</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SPACE REQUIREMENTS</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Rack Mounting</td>
<td>5-1/4 inches (13.14 cm) of vertical space</td>
</tr>
<tr>
<td></td>
<td>24 inches (61 cm) deep</td>
</tr>
<tr>
<td></td>
<td>19 inches (48.26 cm) wide</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ENVIRONMENTAL CHARACTERISTICS</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Relative Humidity</td>
<td>20% to 80% operating</td>
</tr>
<tr>
<td></td>
<td>8% to 80% nonoperating</td>
</tr>
<tr>
<td></td>
<td>5% to 95% shipping (with no condensation)</td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>0°F (32°C) to 110°F (43.4°C) operating</td>
</tr>
<tr>
<td></td>
<td>-30°F (34.4°C) to 140°F (60°C) shipping</td>
</tr>
</tbody>
</table>

1-3. GENERAL DESCRIPTION

The dual-port adaptor includes three printed circuit board assemblies, a self-contained power supply, a cooling fan, a control panel, and appropriate input/output connectors.

1-4. PRINTED CIRCUIT BOARD ASSEMBLIES

All electronic components are contained on three printed circuit board (PCB) assemblies. These boards are stacked horizontally, one above the other, and each is hinged so that all three boards may be raised vertically (in three different directions) for easy servicing (see figure 1-2).

Signals are transferred between the three PCB assemblies and the I/O connectors via ribbon cable harness assemblies which attach to headers (connectors) on the boards. The three PCB assemblies are identified from top to bottom as follows:

- BOARD 1: DUAL-PORT CONTROL LOGIC (DPCTL)
- BOARD 2: DUAL-PORT RECEIVER/TRANSMITTER 2 (DPRX2)
- BOARD 3: DUAL-PORT RECEIVER/TRANSMITTER 1 (DPRX1)
Different versions of the DPCTL board are required for the DP900-1 and DP900-2 models of the dual-port adaptor. Also, different versions of the DPRX1 and DPRX2 receiver/transmitter boards are required for radial and daisy-chain configurations. Refer to section V, maintenance diagrams, for appropriate part numbers.

FIGURE 1-2. DUAL-PORT ADAPTOR PCB ASSEMBLIES
1-5. **POWER REQUIREMENTS**

The dual-port adaptor has the following AC and DC power requirements.

a. **AC Power**

   The adaptor is wired in the factory to operate from either a 115 VAC or a 230 VAC, 50 or 60 Hz, single-phase power source as specified by the customer. Units equipped for 115 VAC operation may be field-modified to operate from 230 VAC as follows:

   (1) Replace 1-ampere fuse with 0.5-ampere fuse.
   
   (2) Alter power transformer wiring in DC power supply as follows:
   
      (a) Remove connections between terminals 1 and 3, and terminals 2 and 4.
      
      (b) Connect jumper between terminals 2 and 3.

   Reverse the above procedure to convert from 230 VAC to 115 VAC.

b. **DC Power**

   A self-contained DC power supply provides ±5 VDC operating power for the dual-port adaptor. The power supply is located at the left rear of the adaptor chassis (see figure 1-3).

c. **Fusing**

   The power circuits of the adaptor are protected by a fuse (1 amp for 115 VAC input or 0.5 amp for 230 VAC input) that is located immediately beneath the power on/off switch on the back panel of the adaptor.

1-6. **INPUT/OUTPUT CONNECTORS**

   All input/output connectors are located on the rear panel of the dual-port adaptor. These connectors and their cable requirements are defined in paragraph 2-8.

1-7. **COOLING**

   A muffin fan mounted on the rear of the chassis, directly behind the power supply, expels warm air from the adaptor thus providing necessary cooling for the electronic components and the power supply (see figure 1-3).

1-8. **LOCATION OF OPERATING SWITCHES AND INDICATORS**

   All switches and indicators, except the power on/off switch, are located on the front panel (see figure 1-1). The power on/off switch is on the rear panel above the fuse. The functions of the switches and indicators are described in section II, paragraph 2-13.

1-9. **OPTIONS**

   The DP900 Dual-Port Adaptor can be purchased with any of the following options, or can be field-modified to include these options.
1-10. **DAISY-CHAIN OPTION**

The standard (radial) configuration is normally used for single installations of the dual-port adaptor and attached disk drive. In this configuration, the adaptor requires two complete sets of interface cables (one Control cable and one Read/Write cable from each controller), and all terminations are made internally in the adaptor and drive.

The daisy-chain option permits a series of adaptor/drive combinations to be chained together on the same control lines by installing Control cables from adaptor to adaptor, and terminating the control-out connectors on the last adaptor in the string with appropriate terminator plugs. Either configuration requires separate Read/Write cables from the controllers to the adaptor.

1-11. **MOUNTING OPTIONS**

The adaptor is supplied as a standalone unit, and may be installed on a table top or appropriate flat surface. As an option, the adaptor may be installed in a standard 19-inch rack cabinet, a disk drive console, or a disk drive quiet enclosure. Drawer slides are required for mounting in both the rack and disk drive consoles.
SECTION II
INSTALLATION AND OPERATION

2-1. UNPACKING AND INSPECTION

Following is the recommended procedure for unpacking and inspecting the dual-port adaptor.

a. Open the protective shipping carton at the top.
b. Remove the DP900 from the shipping carton.
c. Remove the protective plastic cover from the unit.
d. Inspect the unit for damage, and if any is found, notify the appropriate personnel.

After the dual-port adaptor has been unpacked and inspected, refer to table 2-1 and verify that all cables required for system installation are available.

2-2. MOUNTING INSTRUCTIONS

Prior to installing the dual-port adaptor in the system, the appropriate mounting option must be completed.

2-3. INITIAL CHECKOUT

The following checkout procedure should be performed prior to installing the dual-port adaptor in the system.

a. Remove the ten phillips head screws from the top cover and lift the cover from the chassis.
b. Remove the two holldown screws from each PCB assembly and carefully raise the board assemblies to the vertical (maintenance) positions. (*Do not remove the pivot screws.*)
c. Check each PCB assembly for proper seating of all ribbon cable connectors and integrated circuits.
d. Inspect the interior of the chassis for any broken components and tighten any loose screws and hardware.
e. Verify that the DP900 is configured for the appropriate AC power source (refer to paragraph 1-5a).
f. After verifying the power configuration, connect the captive AC power cord to the appropriate AC power source.
g. Turn power switch on DP900 on.
h. Verify that the POWER ON indicator lights. This lamp indicates that ±5 VDC power is available within the unit. If the indicator fails to light, check the ±5 volt (red wire) and ±5 volt (orange wire) terminals on the power supply regulator board for correct operating voltages.
i. Verify that the muffin fan is operating.
j. Turn power switch to off.

k. Return PCB assemblies to horizontal (operating) position and install top cover. The adaptor is now ready for installation and checkout in the using system.

2.4. SYSTEM INSTALLATION

The DP900 Dual-Port Adaptor communicates with two control units through two identical interfaces designated Port A and Port B. The physical interface to each control unit consists of two cables: Control and Read/Write.

The DP900 communicates with its attached disk drive through a single interface consisting of a standard Control cable and a standard Read/Write cable.

A diagram of the system interconnection cabling is shown in figure 2-1.

2.5. CONNECTOR AND CABLE REQUIREMENTS

All input/output connectors are located on the rear panel (figure 2-2) of the dual-port adaptor. Table 2-1 lists these connectors and defines their cable requirements. Following is a description of each interface cable.

<table>
<thead>
<tr>
<th>TABLE 2-1. SYSTEM CABLES AND CONNECTOR INFORMATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Cables, P/N 3305669-XX (DM900 Series) or P/N 3301735 (DM9000 Series)</td>
</tr>
<tr>
<td>FROM</td>
</tr>
<tr>
<td>---</td>
</tr>
<tr>
<td>Controller A</td>
</tr>
<tr>
<td>Controller B</td>
</tr>
<tr>
<td>J1*</td>
</tr>
<tr>
<td>J4*</td>
</tr>
<tr>
<td>J7</td>
</tr>
</tbody>
</table>

* Control terminators, P/N 3305667-01, must be installed in connectors J1 and J4 if the adaptor is the last unit in a daisy-chain configuration.

If the DP900 is ordered for a radial configuration, connectors J1 and J4 are not installed, and termination is accomplished internally on the receiver/transmitter PCB assemblies.

<table>
<thead>
<tr>
<th>Read/Write Cables, P/N 3305668-XX</th>
</tr>
</thead>
<tbody>
<tr>
<td>FROM</td>
</tr>
<tr>
<td>---</td>
</tr>
<tr>
<td>Controller A</td>
</tr>
<tr>
<td>Controller B</td>
</tr>
<tr>
<td>J8</td>
</tr>
</tbody>
</table>
FIGURE 2-1. SYSTEM INTERCONNECTING CABLELING

2-6. CONTROL CABLE

Two control cables (one for each port) connect the two control units to the dual-port adaptor, and a third control cable connects the adaptor to the disk drive. In the daisy-chain configuration, two addi-
tional control cables (one from each port) are required to connect the adaptor to the next adaptor in the string. If the adaptor is the last one in a daisy-chain string, control terminators (P/N 3305667-01) must be installed in connectors J1 and J4. However, if the adaptor is designed for a radial configuration, connector J1 and J4 are not installed, and the terminations are accomplished internally on the receiver/transmitter PCB assemblies.

The control cable is identical to and carries the same signals as the standard control cable for the respective DM900 and DM9000-series disk drives. The XX following the cable part number indicates the cable length in feet (i.e., 3305669-20 indicates a control cable 20 feet long).

Table 2-2 lists the control cable pin assignments and signal functions, and defines the mating connectors and associated hardware. The cable connector shown is for a DM900-series drive. The control cable connector for a DM9000-series drive requires a 180° shield (P/N 166-552) rather than the 90° shield (P/N 167-299) shown in the diagram; all other connector hardware is identical. Because of this connector difference, the control cables for the DM900 and DM9000-series of drives also have different part numbers (see table 2-1 and figure 2-1).

2-7. READ/WRITE CABLE

Each dual-port adaptor requires three Read/Write cables. Two of these cables (one for each port) are used to transfer read/write data between the control units and the adaptor. The third Read/Write cable routes read/write data between the adaptor and its attached disk drive.

The Read/Write cable is identical to the standard Read/Write cable used for the respective DM900 and DM9000-series disk drives. However, previously unused pins are now assigned signal functions which are unique to dual-port operation.

Table 2-3 lists the Read/Write cable pin assignments and signal functions, and defines the mating connectors and associated hardware. The signals which are unique to the DP900-1 are identified by an asterisk (*) and those signals unique to the DP900-2 are identified by a double asterisk (**) .

The Read/Write cable part number is 3305668-XX. The XX indicates the cable length in feet (i.e., 3305668-20 indicates a Read/Write cable 20 feet long).
### TABLE 2-2. CONTROL CABLE DEFINITIONS

<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>PIN POLARITY (ACTIVE)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>–</td>
</tr>
<tr>
<td>Device Select 0</td>
<td>1</td>
</tr>
<tr>
<td>Device Select 1</td>
<td>2</td>
</tr>
<tr>
<td>Device Select 2</td>
<td>3</td>
</tr>
<tr>
<td>Device Select 3</td>
<td>8</td>
</tr>
<tr>
<td>Select Enable</td>
<td>22</td>
</tr>
<tr>
<td>Set Cylinder (Tag 1)</td>
<td>46</td>
</tr>
<tr>
<td>Set Head Address (Tag 2)</td>
<td>48</td>
</tr>
<tr>
<td>Control Select (Tag 3)</td>
<td>52</td>
</tr>
<tr>
<td>Bus Out 0</td>
<td>23</td>
</tr>
<tr>
<td>Bus Out 1</td>
<td>24</td>
</tr>
<tr>
<td>Bus Out 2</td>
<td>28</td>
</tr>
<tr>
<td>Bus Out 3</td>
<td>29</td>
</tr>
<tr>
<td>Bus Out 4</td>
<td>30</td>
</tr>
<tr>
<td>Bus Out 5</td>
<td>34</td>
</tr>
<tr>
<td>Bus Out 6</td>
<td>35</td>
</tr>
<tr>
<td>Bus Out 7</td>
<td>36</td>
</tr>
<tr>
<td>Bus Out 8</td>
<td>40</td>
</tr>
<tr>
<td>Bus Out 9</td>
<td>41</td>
</tr>
<tr>
<td>Device Enable (Open Cable Detect)</td>
<td>16</td>
</tr>
<tr>
<td>Index</td>
<td>10</td>
</tr>
<tr>
<td>Sector Mark</td>
<td>74</td>
</tr>
<tr>
<td>Fault (R/W Unsafe)</td>
<td>11</td>
</tr>
<tr>
<td>Seek Error</td>
<td>75</td>
</tr>
<tr>
<td>On Cylinder</td>
<td>15</td>
</tr>
</tbody>
</table>
TABLE 2-2. CONTROL CABLE DEFINITIONS (Continued)

<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>PIN POLARITY (ACTIVE)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>–</td>
</tr>
<tr>
<td>Unit Ready</td>
<td>17</td>
</tr>
<tr>
<td>Write Protected</td>
<td>53</td>
</tr>
<tr>
<td>Address Mark</td>
<td>42</td>
</tr>
<tr>
<td>Sector Count 0 (Optional)</td>
<td>54</td>
</tr>
<tr>
<td>Sector Count 1 (Optional)</td>
<td>58</td>
</tr>
<tr>
<td>Sector Count 2 (Optional)</td>
<td>59</td>
</tr>
<tr>
<td>Sector Count 3 (Optional)</td>
<td>60</td>
</tr>
<tr>
<td>Sector Count 4 (Optional)</td>
<td>65</td>
</tr>
<tr>
<td>Sector Count 5 (Optional)</td>
<td>66</td>
</tr>
<tr>
<td>Sector Count 6 (Optional)</td>
<td>67</td>
</tr>
<tr>
<td>Sequence Pick</td>
<td>73</td>
</tr>
<tr>
<td>Sequence Enable</td>
<td>76</td>
</tr>
<tr>
<td>Spare</td>
<td>47</td>
</tr>
<tr>
<td>DC Ground</td>
<td>80</td>
</tr>
<tr>
<td>Cable Shield</td>
<td>82</td>
</tr>
</tbody>
</table>

2.8. AC POWER CABLE

Main AC power is supplied to the DP900 via a captive cable with the following type o connector.

120 V, 15 Amp, 60 Hz, 1 Phase, 2-Pole, 3-Wire, Male Connector  NEMA #5-15P

or

230 V, 15 Amp, 50 Hz, 1 Phase, 2-Pole, 3-Wire, Male Connector  NEMA #7-15P

Power to the attached disk drive may be supplied from either control unit or directly from the main AC power source depending on system design.

2.9. TERMINATORS (DAISY-CHAIN OPTION)

The daisy-chain configuration of the DP900 allows daisy-chain connection of the Control cables from the control unit (or previous drive) to the two ports. As shown in figure 2-1, the Control cable must be terminated at the last adaptor in the chain, on both ports, with 3305667 terminators. If it is desired to install a daisy-chain-configured DP900 in a radial fashion (i.e., one Control cable from the control unit for each DP900 to which it connects), a 3305667 terminator must be used on both ports of each DP900 in the system.

The DP900 connects to only one disk drive and termination is included in the unit for this connection. However, if the drive connected to the DP900 is configured with the daisy-chain option, it must have a 3305667 terminator installed on its Control cable output connector.

The radial-configured DP900 incorporates all line termination within the unit and requires no external termination.
### TABLE 2-3. READ/WRITE CABLE DEFINITIONS

**GUIDE PIN, 166-889**
(AMP P/N 200833-4)

**MATING CONNECTOR, 167-310**
(AMP P/N 201357-1)

**FIXED FEMALE JACKSCREW**
169-457, (AMP P/N 200875-2)

**GUIDE SOCKET, 166-890**
(AMP P/N 200835-4)

**CONNECTOR BLOCK**
166-572
(AMP P/N 200838-2)

**MALE JACKSCREW, 169-459**
(AMP P/N 200871-2)

**SHIELD, 166-169**
(AMP P/N 200857-2)

**PIN CONTACT**
3301207-02, (AMP P/N 66103-1),
22 PLACES,
3301207-05, (AMP P/N 66429-1),
10 PLACES.

**GUIDE PIN, 166-889**
(AMP P/N 200833-4)

---

<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>PIN POLARITY (ACTIVE)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-</td>
</tr>
<tr>
<td>Write Data</td>
<td>A</td>
</tr>
<tr>
<td>Servo Clock</td>
<td>M</td>
</tr>
<tr>
<td>Read Data</td>
<td>U</td>
</tr>
<tr>
<td>Read Clock</td>
<td>W</td>
</tr>
<tr>
<td>Write Clock</td>
<td>H</td>
</tr>
<tr>
<td>Selected</td>
<td>BB</td>
</tr>
<tr>
<td>Seek End</td>
<td>AA</td>
</tr>
<tr>
<td>Nineteen-Surface 1D (DM9000-Series Only)</td>
<td>JJ</td>
</tr>
<tr>
<td>Reserved to Partner*</td>
<td>L</td>
</tr>
<tr>
<td>Selected to Other Port**</td>
<td>LL</td>
</tr>
<tr>
<td>Release Reservation*</td>
<td>HH</td>
</tr>
<tr>
<td>Priority Select**</td>
<td>P</td>
</tr>
<tr>
<td>Request De-Select**</td>
<td></td>
</tr>
<tr>
<td>Receive De-Select**</td>
<td></td>
</tr>
</tbody>
</table>

* Unique signal to DP900-1
** Unique signal to DP900-2
2-10. INTERCONNECTING HARNESS ASSEMBLIES

The dual-port adaptor contains eleven ribbon cable harness assemblies. Eight of these harnesses (H1 through H8) transfer signals between the logic boards and the I/O connectors. Three harnesses (H9 through H11) are used to interchange signals between the three logic boards and between logic board 1 and the control panel. The connector designations for each harness assembly are shown in table 2-4. Corresponding connectors (headers) on each logic board are listed below.

| Board 1 | P27, P28, P29, P30, P31 |
| Board 2 | P20, P21, P22, P23, P24, P25, P26 |
| Board 3 | P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19 |

**TABLE 2-4. INTERCONNECTING HARNESS ASSEMBLIES**

<table>
<thead>
<tr>
<th>HARNESS</th>
<th>FROM</th>
<th>TO</th>
</tr>
</thead>
<tbody>
<tr>
<td>H1</td>
<td>J1, A Control Out</td>
<td>Bd. 2 — J20, Bd. 3 — J9, J13</td>
</tr>
<tr>
<td>H2</td>
<td>J2, A Control In</td>
<td>Bd. 2 — J21, Bd. 3 — J10, J14</td>
</tr>
<tr>
<td>H3</td>
<td>J4, B Control Out</td>
<td>Bd. 2 — J22, Bd. 3 — J11, J15</td>
</tr>
<tr>
<td>H4</td>
<td>J5, B Control In</td>
<td>Bd. 2 — J23, Bd. 3 — J12, J16</td>
</tr>
<tr>
<td>H5</td>
<td>J7, A Read/Write to Drive</td>
<td>Bd. 2 — J24, Bd. 3 — J17, J18</td>
</tr>
<tr>
<td>H6</td>
<td>J3, A Read/Write from Controller</td>
<td>Bd. 1 — J29</td>
</tr>
<tr>
<td>H7</td>
<td>J6, B Read/Write from Controller</td>
<td>Bd. 1 — J30</td>
</tr>
<tr>
<td>H8</td>
<td>J8, B Read/Write to Drive</td>
<td>Bd. 1 — J31</td>
</tr>
<tr>
<td>H9</td>
<td>J28 — Bd. 1</td>
<td>Control Panel</td>
</tr>
<tr>
<td>H10</td>
<td>J19 — Bd. 3</td>
<td>J25 — Bd. 2</td>
</tr>
<tr>
<td>H11</td>
<td>J26 — Bd. 2</td>
<td>J27 — Bd. 1</td>
</tr>
</tbody>
</table>

2-11. OPERATING SWITCHES AND INDICATORS

Operation of the dual-port adaptor is essentially automatic (controlled by using control unit) and, except for power application and maintenance activities, no operator intervention is required. The only front panel switch (RESERVE A/AUTO/RESERVE B) allows the operator to override the reservation logic by manually forcing the reservation of the drive to the desired controller. This switch is normally in the AUTO position. The functions of the switches and indicators are listed in table 2-5.
### FIGURE 2-3. FRONT PANEL SWITCHES AND INDICATORS

### TABLE 2-5. SWITCHES AND INDICATORS

<table>
<thead>
<tr>
<th>NAME</th>
<th>TYPE</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Force Reservation</td>
<td>3-position rocker switch</td>
<td>Used to override the device reservation logic.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>When in this position, reserves the drive to control unit on Port A.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>When in this position, enables the device reservation logic permitting the drive to be automatically reserved by the selecting control unit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>When in this position, reserves the drive to control unit on Port B.</td>
</tr>
<tr>
<td>Reserve A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Auto</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserve B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Device Reservation/Selection</td>
<td>Yellow LED indicators</td>
<td>These are four LED's located on the front panel.</td>
</tr>
<tr>
<td>A Reserve</td>
<td></td>
<td>This indicator lights if controller A initiates selection and the drive is not already reserved by controller B.</td>
</tr>
<tr>
<td>B Reserve</td>
<td></td>
<td>This indicator lights if controller B initiates selection and the drive is not already reserved by controller A.</td>
</tr>
<tr>
<td>A Select</td>
<td></td>
<td>This indicator lights whenever the control unit on Port A communicates with the drive.</td>
</tr>
<tr>
<td>B Select</td>
<td></td>
<td>This indicator lights whenever the control unit on Port B communicates with the drive.</td>
</tr>
<tr>
<td>Power</td>
<td>Toggle switch</td>
<td>This toggle switch (located on the rear panel) applies power to the DP900.</td>
</tr>
<tr>
<td>Power On</td>
<td>Red LED indicator</td>
<td>This indicator lights to indicate that ±5 VDC power is available.</td>
</tr>
</tbody>
</table>
SECTION III
THEORY OF OPERATION

3-1. BASIC OPERATION

The DP900-1 and DP900-2 Dual-Port Adaptors permit access to a disk drive by either of two controllers. To accomplish this, the adaptor functions as a dynamic (or static) switch that transfers control and data signals between the drive and the using controller.

Included on the front panel of the DP900-1 and DP900-2 Dual-Port Adaptors is a manual three-position switch which allows the operator to statically assign reservation of the drive to one of the two attached control units. If the operator sets the manual switch to either the RESERVE A or RESERVE B positions, the drive and dual-port become statically reserved to the controller on the designated port, and all reservation or release signals from either of the two control units are ignored.

In addition to the manual reservation switch, the adaptor incorporates a logical three-position switch that permits the drive to be dynamically selected and reserved by either of the two control units. The logical switch is enabled only when the manual switch is in the AUTO position. When neither of the two controllers has the drive reserved, the logical switch is, in effect, in the neutral position and the drive may be selected from either port. The logical switch is automatically latched to the first port to successfully complete a selection of the drive.

The dual-port adaptor incorporates tie-breaking logic to solve the problem of simultaneous or overlapping selection attempts from both control units. In these situations, the select attempt from the nonwinning control unit is held until the select attempt from the winning control unit is completed. This is explained in more detail in paragraph 3-15, entitled Select Timing.

Except for basic differences in the method of selection, reservation, and release, the DP900-1 and DP900-2 Dual-Port Adaptors operate in essentially the same manner. These basic differences are listed in table 3-1 and described in the following paragraphs.

3-2. SELECTION AND RESERVATION (DP900-1)

Drive selection is accomplished as follows. The controller activates the appropriate device select number lines to the dual-port adaptor, and after a minimum delay of 200 nanoseconds, raises the Select Enable line. This action reserves the appropriate port to the controller and allows the DP900-1 to transfer the device select number lines and the Select Enable signal to the attached drive, where an address comparison is made with the Select Plug inserted in the drive. If the addresses compare, the drive indicates its selected condition by sending a Selected signal to the dual-port adaptor. If the addresses do not compare, the reservation will be cleared.

Upon receipt of the Selected signal, the dual-port adaptor does the following:

a. Consumes the logical switching of the dual port to the selecting control unit and, thereby, relays the Selected signal to that control unit.

b. Saves the successful device select number in a select plug register for comparison with device select numbers sent during select attempts by the other (nonselected) controller.

c. Automatically reserves the drive to the controller on the selecting port. The drive remains reserved, even though the selection may be dropped, until the control unit activates a Release reservation signal (see paragraph 3-3).
## TABLE 3-1. BASIC DIFFERENCES BETWEEN DUAL-PORT ADAPTORS

<table>
<thead>
<tr>
<th>DP900-1</th>
<th>DP900-2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Automatically reserves the dual-port adaptor following a successful drive selection, and retains the reservation even if the selecting controller drops the Select Enable signal.</td>
<td>Automatically reserves the dual-port adaptor following a successful drive selection, but releases the reservation if the selecting controller drops the Select Enable signal.</td>
</tr>
<tr>
<td>Must issue a release before the partner control unit can use the drive.</td>
<td>The partner control unit may use the drive as soon as it is deselected by the user control unit.</td>
</tr>
<tr>
<td>Does not require constant attention of the controller to maintain the reserve. The dual-port adaptor stays reserved until the release command is issued.</td>
<td>The controller may cause a reserve by activating the Priority Select command and holding it active until the control unit is finished with its sequence.</td>
</tr>
<tr>
<td>Can force partner’s release of the drive by issuing a force release command while partner has the dual-port reserved.</td>
<td>Can force partner’s release of the drive by issuing a Priority Selection command while partner is using the drive, unless partner has its Priority Selection active.</td>
</tr>
<tr>
<td>Provides a communication link between partner controllers allowing the requesting of a partner to release its reservation; these signals are the Request De-Select and the Receive De-Select.</td>
<td></td>
</tr>
</tbody>
</table>

If the drive is reserved by a control unit on one of the ports (for discussion, assume Port A), and the control unit on the partner port (Port B) attempts selection, a comparison of the device select number lines with the select plug register is made. A successful comparison causes the adaptor to activate the Reserved to Partner status signal to the Port B control unit. A control unit must therefore monitor two lines in the Read/Write cable during a select attempt. These lines are Selected and Reserved to Partner.

a. **Selected**

The active state of this line indicates that the select attempt was successful, the drive is selected, and the dual-port adaptor is reserved to the selecting controller.

b. **Reserved to Partner**

The active state of this line indicates that the port was successfully selected, but the partner control unit has the drive reserved and, therefore, it is unavailable to the control unit attempting selection.

If neither the Selected nor the Reserved to Partner lines are activated within the allotted time (see paragraph 3-14 for operational timing requirements), it indicates that the select attempt was unsuccessful (i.e., the drive select plug did not match the transmitted device select number).

### 3-3. RELEASE RESERVATION (DP900-1)

The dual-port reservation can be released normally by the reserving control unit or can be forcibly released by the partner control unit. In either case, the control unit initiates the action by activating a Release signal.
3.4. **DP900-1 NORMAL RELEASE**

Normally, a control unit releases its reservation of the drive and dual-port adaptor by raising the Release command. This occurs following the receipt of the Selected signal as the result of a successful selection attempt, or following a sequence of operations on the selected drive.

**NOTE**

_The Release signal must be a pulse of 1.0 µsec minimum duration. The actual release occurs on the trailing edge of the signal._

The Select Enable signal from the controller must drop within 500 µsec after the Release signal drops to ensure that the drive and dual port are not re-reserved by the same control unit.

3.5. **DP900-1 FORCED RELEASE**

Following a selection of the dual-port adaptor by the nonreserving control unit, the dual-port adaptor is responsive to only one command from that control unit and that is Release. If the Release signal is activated in this situation, the reservation by partner is force released. This action causes the drive to cease any read or write operation currently in progress and return to the unselected mode. The dual-port adaptor drops the Reserved to Partner signal to indicate that the force release has been consummated. If the nonreserving control unit maintains its device select number and Select Enable lines active after dropping the Release (force release) signal, it will select and reserve the drive.

An example of the implementation of the force release capability is to have the nonreserving control unit monitor the Reserved to Partner status for a predetermined length of time. If, during this length of time, the partner has not used the drive, the assumption is made that the partner control unit is hung up, or dead and, therefore, a forced release is in order. This permits the system to automatically recover access to a drive that would otherwise be unavailable because of a system failure elsewhere.

**NOTE**

_The forced release function must be used with discretion since it causes an immediate cessation of all activities, including write operations, and could result in incomplete files, records, or sectors on the disk._

When the dual port executes a forced release, it sets a force released memory latch for the port being released. This latch prohibits subsequent port selection until that port’s control unit drops and then reraises its Select Enable line, indicating that it is not in a hung up condition with Select Enable active. In this way, once a port has been forced released away from a hung up control unit, it does not get reselected to that control unit until it is restarted by manual or other intervention.

3.6. **SEEK END HANDLING (DP900-1)**

Special handling must be made of the Seek End signal. Seek End normally indicates the completion of any carriage motion operation including a seek incomplete condition. Since a Rezero operation occurs following initial startup of a new pack or insertion of a new plug, Seek End also indicates completion of a pack change or address change. The Seek End signal is cleared by any of the following:
a. The initialization of another carriage motion operation
b. The removal of the select plug (if the drive is not selected)
c. The stopping of the pack motor

The following changes have been incorporated into the dual-port adaptor in regards to the Seek End signal.

a. If the logical port reservation switch is in the neutral position, the state of the Seek End signal is passed to both of the attached control units.

b. When the drive is reserved by one of the control unit, the dynamic Seek End signal is forwarded only to the reserving control unit. The state of the Seek End signal at the time of reservation is locked to the partner (nonreserving) control unit.

c. While the drive is reserved by one control unit, the dual port will remember any selection attempts by the partner control unit. Then, when the reserving control unit drops its reservation, the port will lower the Seek End signal for 1.5 ms, then raise it again to the control unit that did not have the reservation. This provides a low-to-high transition of the Seek End signal, alerting that control unit of the drive's availability.

d. If, while the drive is reserved to one control unit, the Seek End signal from the drive drops low for a period of one second or more, the dual port causes a lowering and raising of the Seek End signal to the partner control unit upon reservation release as described in the previous paragraph. This Seek End is generated to alert the nonreserving control unit that the select plug or disk pack may have been changed during the partner's reservation period.

3-7. SELECTION (DP900-2)

Either of the attached controllers may initiate selection of the drive by activating appropriate device select number lines to the dual-port adaptor, and raising the Select Enable signal a minimum of 200 nanoseconds later. This temporarily reserves the appropriate port and permits the DP900-2 to transfer the device select number lines and the Select Enable signal to the attached disk drive. The disk drive compares the device select number with the Select Plug inserted in the drive, and if they compare, the drive sends a Selected signal to the DP900-2 to indicate that a successful selection has been made. The temporary reservation of the dual port is cleared if the addresses do not compare.

Upon receipt of the Selected signal, the DP900-2 does the following:

a. Consummates the logical switching of the dual port to the selecting control unit and, thereby, relays the Selected signal to that control unit.

b. Saves the successful device select number in the select plug register for comparison with device select numbers sent during select attempts by the other (nonselected) controller.

c. Automatically reserves the drive to the controller on the selecting port, and retains this reservation as long as the controller holds the Select Enable signal active, or until the partner (nonselecting) control unit activates a Priority Select signal to cause a forced release of the reservation. (See paragraph 3-11 for an explanation of forced release.)

In attempting to select the drive, a controller must monitor two lines in the Read/Write cable. These lines are Selected and Selected to Other Port.
a. **Selected**

The active state of this line indicates that the drive has been successfully selected, and the dual port will remain reserved to the selecting controller as long as the controller holds Select Enable active, or until the partner forces release by activating a Priority Select.

b. **Selected to Other Port**

The active state of this line indicates that the control unit on one port (assume Port B) has made a successful port selection (device select number compares with select plug register) but the drive is already selected by the control unit on Port A and, therefore, is unavailable to Port B.

If neither the Selected nor the Selected to Other Port signals are activated within the allotted time (see paragraph 3-14 for operational timing requirements), it indicates that the select attempt is unsuccessful (i.e., the drive select plug did not match the transmitted device select number).

3.8. **NORMAL RELEASE (DP900-2)**

During normal operation, a controller releases its selection of the drive by simply deactivating the Select Enable line to the DP900-2. This causes the logical switch to return to the neutral position. However, if either controller uses its Priority Select signal to exclusively reserve or force release the dual port, the normal release function has no effect. Use of the Priority Select signal is described in the following paragraphs.

3.9. **EXCLUSIVE RESERVATION AND FORCED RELEASE (DP900-2)**

The Read/Write cable includes a special signal, Priority Select, which is unique to the operation of the DP900-2 and provides several functions, depending upon the conditions of the dual port when it is used.

3.10. **DP900-2 EXCLUSIVE RESERVATION**

When the Priority Select line is raised by the control unit currently holding a successful drive selection, it reserves the dual port and prohibits the partner control unit from forcing a release reservation by the use of its Priority Select line. If Priority Select is maintained in the active state by the control unit, even though it has dropped selection of the drive, the partner control unit is prohibited from selecting the drive as well as force-releasing the reservation to the first control unit. In this way, Priority Select provides a method whereby a control unit may keep the drive reserved while the control unit is selecting and working with other drives in a daisy-chain string.

In order for the Priority Select signal to be recognized by the DP900-2, a successful port selection must have occurred first (i.e., the sending of the select number lines and the raising of the Select Enable line, along with the subsequent successful comparison of the number on the device select number lines with the select plug, must have occurred).

3.11. **DP900-2 FORCED RELEASE**

When the Priority Select line is raised by a control unit holding only a dual port selection (partner control unit has the drive selected), it causes the immediate termination of the partner's selection and use of the drive (unless the partner control unit had previously raised its Priority Select line). In this way, the nonselecting control unit can force a release of the dual-port unit and drive, if it has urgent work to do, or if it suspects that the partner control unit may be in a hung-up condition.
NOTE

This function must be used with discretion since it causes an immediate cessation of all activities, including write operations, and could result in incomplete files, records, or sectors on the disk.

If the Priority Select line is held active after it has been raised (along with the select number lines and the Select Enable line), the dual port, following a 500-μsec delay (to permit drive functions to cease), will send the select number lines and the Select Enable signal to the drive to permit drive selection. In this way, drive selection can be obtained following a forced release.

When the dual port executes a forced release as the result of a Priority Select, it sets a force released memory latch for the port being released. This latch prohibits subsequent selection of the DP900-2 until that port’s control unit drops and then reraises its Select Enable line, indicating that it is not in a hung-up condition with Select Enable active. In this way, once a port has been force-released away from a hung-up control unit, it does not get reselected to that control unit until it is restarted by manual or other intervention.

3.12. INTERCONTROL UNIT RELEASE REQUESTING (DP900-2)

Included in the Read/Write cable are two unique signals, Request De-Select and Receive De-Select, which the DP900-2 uses to provide a communication link between the two attached control units. Through this communication link, the nonusing controller can gracefully request the partner to release the drive, rather than just forcing a release with the Priority Select signal.

Either control unit, upon consummating a successful selection of either the drive or the dual port (if the partner control unit has the drive selected), may raise its Request De-Select line. This line is considered by the DP900-2 and, if the following conditions are met, causes the Receive De-Select line to be activated to the partner control unit:

a. The requesting control unit has drive select or port select.

b. Partner does not have Priority Select active.

c. Partner does not have Request De-Select (and consequently Receive De-Select) active

Receive De-Select will be held active to the partner’s control unit until:

a. This port drops Select Enable.

b. This port drops Request De-Select.

c. Partner raises Priority Select.

3-13. SEEK END HANDLING (DP900-2)

Seek End normally indicates the completion of any carriage motion operation, including a seek incomplete condition. Since a Rezero operation occurs following initial startup of a new pack and following insertion of a new select plug, Seek End also indicates completion of a pack change or address change. The Seek End condition is cleared by initialization of a seek operation, removal of the select plug, if the drive is not selected, or the stopping of the pack motor.

The DP900-2 does not require any special handling of the Seek End signal, as it passes the signal from the drive to both control units at all times regardless of the position of the logical or manual
reservation switches. It is the control unit's responsibility to monitor this signal to determine whether the select plug or pack may have been changed during the partner's selection of the drive.

3.14. OPERATIONAL TIMING REQUIREMENTS

Because the dual-port adaptor is a device with several special functions, and because it can be located up to 40 cable feet away from the drive, several unique timing restrictions must be imposed. However, a control unit designed to accommodate the timing requirements of the adaptor will also function with no modification with the DM900-series or DM9000-series drives not working through a dual-port adaptor.

3.15. SELECT TIMING

Of prime concern to the function of the controller is the total amount of time required from when the select number lines are raised by the controller to when the Selected signal returns from the dual-port adaptor, indicating successful selection of the drive. The worst-case situation exists when one control unit attempts to select a drive just moments after the partner control unit has issued a select to the drive string (in a daisy-chain configuration). In this case, the second control unit's select attempt must be held up at the dual port until the select attempt of the drive by the first control unit is complete. No comparison can be made with the select plug register, in this case, because it is not loaded with a valid device select number until one of the control units has successfully selected (reserved) the drive. Consequently, the contents of the select plug register cannot be trusted whenever the logical reservation switch is in neutral.

Figure 3-1 illustrates the worst-case timing situation for a selection attempt on both the DP900-1 and DP900-2 Dual-Port Adaptors. This figure shows the various timing events that occur from the issuance of the device select number by a control unit to the receipt of the Selected signal at the control unit. From the figure it can be seen that:

\[
\text{Maximum Select Cycle Time} = 200 \text{ ns} + 1000 \text{ ns} + 200 \text{ ns} + 120 \text{ ns} + 200 \text{ ns} + 120 \text{ ns} + 100 \text{ ns} + PT = 1940 \text{ ns} + PT
\]

Assuming the maximum cable length from control to drive is 100 ft.:

\[
PT = 3 \times 100 \text{ ns} = 300 \text{ ns}
\]

\[
\text{Maximum Select Cycle Time} = 1940 + 2 \times 300 = 1940 + 600 = 2540 \text{ ns}
\]

It is recommended, therefore, that the control unit wait at least 3.0 \(\mu\text{sec}\) following the beginning of a select attempt before declaring the attempt unsuccessful (if Selected has not been returned by the drive). This allows ample time for the drive to respond to select attempts from both control units at essentially the same time.

Referring to figure 3-1 again, it should be noted that if the partner had already successfully selected the drive, the dual-port adaptor would not have attempted to select the drive for the second control unit. Instead, the status signals, Reserved to Partner (DP900-1) or Selected to Other Port (DP900-2), would have been returned to the second control unit at the completion of the first control unit's select cycle.
Select No. Lines Xmitted from C.U.
Select No. Lines Recv'd at Dual Port
SELECT ENABLE Xmitted from C.U.
SELECT ENABLE Recv'd at Dual Port
Partner's Dual Port-to-Drive Select Cycle
Select No. Lines Xmitted from DP to Drive
Select No. Lines Recv'd at Drive
SELECT ENABLE Xmitted from DP to Drive
SELECT ENABLE Recv'd at Drive
SELECTED Xmitted from Drive to DP
SELECTED Recv'd at DP
SELECTED Xmitted from DP to C.U.
SELECTED Recv'd at C.U.
Select Attempt Cycle Window

PT — Cable Propagation Time
C.U. to DP
≈3.0 ns per foot max.
PT max. @ 100 ft. ≈300 ns

**FIGURE 3-1. WORST CASE SELECTION TIMING**
3-16. RELEASE TIMING

Release timing restrictions for the DP900-1 and DP900-2 are described in the following paragraphs.

a. DP900-1 Release Timing Restrictions

The DP900-1 remains reserved to a control unit until either that control unit or the partner control unit issues a Release command. In the case of the release being generated by the partner control unit, it is with the intent of gaining access (selection and reservation) to the drive by forcing a release of the reserved control unit. The dual-port adaptor includes the capability of allowing a selection attempt and subsequent reservation to the control unit issuing the release providing it holds its Select Enable signal active. This capability imposes some timing restrictions on the use of the Release command. The timing restrictions for the DP900-1 are illustrated in figure 3-2.

b. DP900-2 Release Timing Restrictions

Generally, the controller that does not hold selection of the drive can gain access to the drive by raising a Priority Select signal and thus force a release of the partner control unit. The controller issuing the Priority Select can then select the drive providing that controller holds its Select Enable signal active. This capability imposes some timing restrictions on the use of the Priority Select command. The timing restrictions for the DP900-2 are shown in figure 3-3.
SELECT NO. LINES

SELECT ENABLE

RELEASE

- Causes a release to both ports. If partner was reserved, it forces his release.
- To avoid "re-reserving", SELECT ENABLE must be dropped no later than 500 ns after RELEASE drops.
- Actual release occurs at trailing edge of RELEASE pulse.

RELEASE TIMING WITH NO FOLLOWING RESERVATION

SELECT NO. LINES

SELECT ENABLE

RELEASE

- Causes a release to both ports and reservation to sending port.
- SELECT ENABLE must be held active for a minimum of 2.0 µsec after RELEASE drops to ensure reservation.
- Usually used only in a "forced" RELEASE situation.

RELEASE TIMING WITH FOLLOWING RESERVATION

FIGURE 3-2. DP900-1 RELEASE TIMING
SELECT NO. LINES

SELECT ENABLE

PRIORITY SELECT

- If partner was selected, it forces his release.
- To avoid re-reserving, Select Enable must be dropped no later than 500 ns after Priority Select drops.
- Actual release occurs at leading edge of Priority Select pulse.

RELEASE TIMING WITH NO FOLLOWING SELECTION

SELECT NO. LINES

SELECT ENABLE

PRIORITY SELECT

- Causes a release to partner port and selection to sending port.
- Select Enable must be held active for a minimum of 2.0 μsec after Priority Select drops to ensure selection.
- Usually used only in a forced release situation.
- Priority Select may remain active to prohibit partner's selection of drive.

RELEASE TIMING WITH FOLLOWING SELECTION

FIGURE 3-3. DP900-2 RELEASE TIMING
SECTION IV

SIMPLIFIED LOGIC DIAGRAMS

FIGURE 4.1. DEVICE ENABLE, SIMPLIFIED LOGIC DIAGRAM

FIGURE 4.2. SELECT LOGIC, SIMPLIFIED LOGIC DIAGRAM
FIGURE 4-3. SELECTION DECODE AND COMPARISON LOGIC
SERVO CORRECTION

SERVO READ SIGNAL
NOTE - Only logic for one 'Port' shown
SECTION V
MAINTENANCE DIAGRAMS

5-1. GENERAL

This section provides maintenance personnel with maintenance diagrams for the Ampex DP900-2 Dual-Port Adaptor.

5-2. LOGIC SYMBOLOGY

The logic symbols used on the schematic diagrams are specified in MIL-STD-806B. Standard definitions are used and active signal levels are listed on all input and output lines.

5-3. LIST OF DRAWINGS

SCHEMATIC DIAGRAMS

<table>
<thead>
<tr>
<th>Title</th>
<th>Location</th>
<th>Drawing No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual-Port Control Logic (DPCTL)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP900-1</td>
<td>Bd. 1</td>
<td>3305790-01</td>
</tr>
<tr>
<td>DP900-2</td>
<td>Bd. 1</td>
<td>3307010-01</td>
</tr>
<tr>
<td>Dual-Port Receiver/Transmitter 2 (DPRX2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Radial Configuration</td>
<td>Bd. 2</td>
<td>3305810-01</td>
</tr>
<tr>
<td>Daisy-Chain Configuration</td>
<td>Bd. 2</td>
<td>3307060-01</td>
</tr>
<tr>
<td>Dual-Port Receiver/Transmitter 1 (DPRX1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Radial Configuration</td>
<td>Bd. 3</td>
<td>3305800-01</td>
</tr>
<tr>
<td>Daisy-Chain Configuration</td>
<td>Bd. 3</td>
<td>3307020-01</td>
</tr>
<tr>
<td>Power Supply Schematic and Parts List</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Dual-Port Receiver/Transmitter 2 (DPRX2) with RPQ Power Sequencing Options</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Radial Configuration (RPQ50)</td>
<td>Bd. 2</td>
<td>3306180-01</td>
</tr>
<tr>
<td>Daisy-Chain Configuration (RPQ51)</td>
<td>Bd. 2</td>
<td>3306190-01</td>
</tr>
</tbody>
</table>

ASSEMBLY DRAWINGS AND PARTS LISTS

<table>
<thead>
<tr>
<th>Title</th>
<th>Drawing No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual-Port Control Logic (DPCTL)</td>
<td></td>
</tr>
<tr>
<td>DP900-1</td>
<td>3305793-01</td>
</tr>
<tr>
<td>DP900-2</td>
<td>3307013-01</td>
</tr>
</tbody>
</table>
## ASSEMBLY DRAWINGS AND PARTS LISTS (Continued)

<table>
<thead>
<tr>
<th>Title</th>
<th>Drawing No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual-Port Receiver/Transmitter 2 (DPRX2)</td>
<td></td>
</tr>
<tr>
<td>Radial</td>
<td>3305813-01</td>
</tr>
<tr>
<td>Daisy-Chain</td>
<td>3307063-01</td>
</tr>
<tr>
<td>Dual-Port Receiver/Transmitter 2 (DPRX2) with RPQ Power Sequencing Options</td>
<td></td>
</tr>
<tr>
<td>Radial (RPQ50)</td>
<td>3306183-01</td>
</tr>
<tr>
<td>Daisy-Chain (RPQ51)</td>
<td>3306193-01</td>
</tr>
<tr>
<td>Dual-Port Receiver/Transmitter 1 (DPRX1)</td>
<td></td>
</tr>
<tr>
<td>Radial</td>
<td>3305803-01</td>
</tr>
<tr>
<td>Daisy-Chain</td>
<td>3307023-01</td>
</tr>
<tr>
<td>Dual-Port Adaptor Assembly</td>
<td>3307906-XX</td>
</tr>
</tbody>
</table>

## HARNESS ASSEMBLY WIRE LISTS

<table>
<thead>
<tr>
<th>Title</th>
<th>Drawing No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1 to Logic</td>
<td>(H1) 3301776-01</td>
</tr>
<tr>
<td>J2 to Logic</td>
<td>(H2) 3301777-01</td>
</tr>
<tr>
<td>J4 to Logic</td>
<td>(H3) 3301778-01</td>
</tr>
<tr>
<td>J5 to Logic</td>
<td>(H4) 3301779-01</td>
</tr>
<tr>
<td>J7 to Logic</td>
<td>(H5) 3301785-01</td>
</tr>
<tr>
<td>J3 to J29</td>
<td>(H6) 3301786-01</td>
</tr>
<tr>
<td>J6 to J30</td>
<td>(H7) 3301787-01</td>
</tr>
<tr>
<td>J8 to J31</td>
<td>(H8) 3301788-01</td>
</tr>
<tr>
<td>Control Panel Assembly</td>
<td>(H9) 3301789-01</td>
</tr>
<tr>
<td>J19 to J25</td>
<td>(H10) 3301807-01</td>
</tr>
<tr>
<td>J26 to J27</td>
<td>(H11) 3301808-01</td>
</tr>
<tr>
<td>DC Power Wiring</td>
<td>3301837-01</td>
</tr>
<tr>
<td>REF DES</td>
<td>VALUE/DESCRIPTION</td>
</tr>
<tr>
<td>---------</td>
<td>-------------------</td>
</tr>
<tr>
<td>C1,2</td>
<td>9000/15 CAPACITOR ALUM ELECTROLYTIC</td>
</tr>
<tr>
<td>C6</td>
<td>100/35</td>
</tr>
<tr>
<td>C8,5</td>
<td>220/16 ALUM ELECTROLYTIC</td>
</tr>
<tr>
<td>C4,7</td>
<td>.01/100 CAPACITOR MYLAR</td>
</tr>
<tr>
<td>CR5,9,10</td>
<td>AE 1C DIODE, 1A, 200V</td>
</tr>
<tr>
<td>CR1,2,5,7,3</td>
<td>AE 33B DIODE, 3A, 100V</td>
</tr>
<tr>
<td>CR4,8</td>
<td>IN 752A DIODE, ZENER, 400mV</td>
</tr>
<tr>
<td>SCR1,2</td>
<td>50303L53 SCR 1A</td>
</tr>
<tr>
<td>Q1,3</td>
<td>2N 6492 TRANSISTOR, POWER DARLINGTON, NPN</td>
</tr>
<tr>
<td>Q2</td>
<td>2N 2905 TRANSISTOR</td>
</tr>
<tr>
<td>R1,2,3,8,13,14</td>
<td>270 OHM RESISTOR, 1/2W CARBON</td>
</tr>
<tr>
<td>R11</td>
<td>1K</td>
</tr>
<tr>
<td>R4,4,10</td>
<td>2.2K</td>
</tr>
<tr>
<td>R18</td>
<td>240 OHM</td>
</tr>
<tr>
<td>R7,12</td>
<td>47K</td>
</tr>
<tr>
<td>R19,17</td>
<td>.12M RESISTOR 2W, WW, BHW</td>
</tr>
<tr>
<td>R6,R16</td>
<td>1.5K POTENTIOMETER 2W WW</td>
</tr>
<tr>
<td>R1B</td>
<td>2.2K RESISTOR 1/2W CARBON</td>
</tr>
<tr>
<td>U1,U2</td>
<td>JA 723 IC VOLTAGE REGULATOR</td>
</tr>
<tr>
<td>TI</td>
<td>12115 TRANSFORMER</td>
</tr>
<tr>
<td>PCB</td>
<td>12089 PRINTED CIRCUIT BOARD</td>
</tr>
<tr>
<td>CHASSIS</td>
<td>11101 ALUMINUM, ALODINE COATED</td>
</tr>
</tbody>
</table>

[Diagram of circuit with components labeled]
Differential and Operational Amplifiers

INTRODUCTION

As originally conceived, the differential amplifier was a direct-coupled (d-c) amplifier. A d-c amplifier is one that is connected to the following stage without the use of a coupling capacitor or transformer. Thus, it is not possible to separate the signal currents from those of the biasing network. Such circuits are still widely used in applications requiring the amplification of direct-current or low-frequency signals where it is impossible or impractical to use coupling capacitors.

The principal applications of d-c amplifiers are in the instrumentation field, especially where it is necessary to separate and amplify low-level difference-mode (DM) signals from much larger common-mode (CM) signals. A typical application is that of detecting unbalance in a strain-gauge bridge network.

The advent of monolithic integrated circuits has substantially changed and widened the use of the differential amplifier. It is a building block for almost every linear (not digital) integrated circuit presently being fabricated. It is used as a balanced or unbalanced amplifier, as an oscillator, as a mixer or converter, and as a cascade amplifier. Its applications span the spectrum from low to high frequencies in video, wide-band, and narrow-band applications. And it is the basic building block for the operational amplifier.

The operational amplifier is typically a cascaded series of differential amplifiers followed by an appropriate output stage. Thus, there is a design relationship between the differential and operational amplifier. The operational amplifier is composed of a number of differential amplifiers.

The differential amplifier finds wide application when used by itself or as the differential input to an operational amplifier. When used by itself, the differential amplifier requires relatively few components, none of which is critical as long as corresponding components of each amplifier half are matched. Thus, absolute component tolerances may be very loose as long as component matching is maintained.

This characteristic is especially important in integrated-circuit fabrication where absolute tolerances cannot be held to much better than about 20 percent, but ratios can be held to better than 3 percent, and parameters for transistors on the same die can be matched even closer. It is evident that these considerations had an important impact on the selection of the differential amplifier as the basic building block for linear integrated circuits.

The operational amplifier is widely used in a variety of electronic applications, including those utilizing the silicon integrated circuit technology. In addition to its versatility, the operational amplifier has several important advantages. Its operation is determined by discrete feedback components; and circuit operation can be completely determined and specified by considering only these components and the input-output and transfer characteristics of the circuit. Because the user of this circuit need not be concerned with those parameters internal to the operational amplifier, he can analyze the circuit very simply. Furthermore, when this circuit is integrated, circuit operation can be specified only by the external discrete components.

DIFFERENTIAL AMPLIFIERS

The most widely used direct-coupled amplifier is known as the difference amplifier. This circuit has two inputs, and the output is equal to the difference in voltage between the two inputs multiplied by the gain of the amplifier. This interesting property makes it possible to measure small potential differences in the presence of large amounts of noise. If the noise signal on each input of the amplifier is the same (as would be the case, for example, with 60-Hz a-c pickup from two unshielded wires), the difference between the two noise signals is zero, and therefore the noise is not amplified at all. Signals which appear in phase and with the same amplitude at both inputs are known as common-mode (CM) signals. Those which are
not the same are known as difference-mode (DM) signals.

It can be seen that the output load, $R_O$, is across the collector outputs of $Q_1$ and $Q_2$, and that therefore the voltage, $V_O$, across $R_O$ represents a difference. $V_O$ is the difference between the amplified input to $Q_1$ and the amplified input to $Q_2$. Since $Q_1$ and $Q_2$ are closely matched for operating characteristics, the amplification provided by each should be nearly equal. Therefore, if equal voltage signals are applied to the two inputs, nearly equal amplification is given to each, and the difference across $R_O$ would be zero. This is how common-mode (CM) signals are rejected. If different voltages are applied to the inputs, each is amplified by the same factor, and the amplified difference appears across $R_O$. Thus, difference-mode (DM) signals are amplified.

$Q_3$: $R_{E_1}$ and $R_{E_2}$ form a constant current source for more constant operation over the full range of operating points and temperature.

**FUNDAMENTALS OF THE OPERATIONAL AMPLIFIER**

An operational amplifier is simply a cascaded series of differential amplifiers, sometimes with a single-ended power-output stage (Figure 3). As it is supplied, however, it is virtually useless. A typical operational amplifier will have a voltage gain of 100,000 or more. Noise on the input will therefore simply saturate the output. By adding different negative feedback features such as frequency-selective networks or nonlinear elements, the behavior of the amplifier can be changed. If the gain of the amplifier is sufficiently high, and it usually is, the operation of the circuit is determined solely by the feedback.

Figure 4 shows a simple circuit using an operational amplifier. This circuit is simply an amplifier with a voltage gain of one; it is called a follower. The follower has a very high input impedance and very low output impedance, and therefore has high power gain.

Because this amplifier has a differential input and high gain, the two input voltages must be equal to within a few microvolts in order for the output to remain within the operating range of the circuit (usually ±5 or ±10 volts). If there were no feedback, this would not be possible. In the follower, the output is connected directly to the inverting input. If the plus input of the amplifier is raised...
output must also follow, and so it has the same voltage as the input.

What is the output impedance of this circuit? Normally, the output impedance of a circuit comes from the series resistance between the power supply and the output transistors. This is true inside the operational amplifier too, but voltage gain has been traded for output impedance. If some current is drawn from the output of the amplifier, any internal voltage drop in the output stage will show up on the output. This drop will be fed back to the input and will show a net input voltage difference. This difference, in turn, will cause the amplifier to increase the output drive to compensate for the voltage drop and the input voltages will again be the same. In fact, the output voltage will not change regardless of load until the maximum current output capabilities of the amplifier are reached. The circuit therefore appears to have a very low output impedance, on the order of a few milliohms.

Without feedback, the operational amplifier might have a typical output impedance of 5000 ohms. The output impedance is simply $Z_{in}$ for the first stage of the amplifier and can therefore be quite high. If field-effect transistors are used, input impedance as high as 10<sup>12</sup> ohms are possible.

**TYPICAL LINEAR SUMMING**

Figure 5 shows an operational amplifier connected as an inverting amplifier. The gain $A$ equals -1. This circuit is a basic circuit for computation and for many instrumentation applications.

The plus input of the amplifier is connected to ground; therefore, the minus input must be within a few microvolts of ground or the output of the
amplifier will be off-scale. The amplifier will draw current through $R_f$ to try to keep this minus input at ground. This point, known as the summing mode, is therefore a virtual ground. The output of the amplifier is forcing it to ground. This concept is very useful. For example, it is very easy to see that the input impedance of this configuration is equal to $R_i$.

![Figure 5](image)  
Figure 5. – Circuit to show the operational amplifier as a unity-gain converter.

Suppose now that $V_{in}$ is 2 volts and $R_i = R_f = 10,000$ ohms. The input current in the summing mode is 0.2 mA. In order to satisfy Kirchhoff's law at the summing mode and keep the voltage there at ground (assuming a very high input impedance to the amplifier itself), the output must draw 0.2 mA through $R_f$. If $R_f$ is equal to 10,000 ohms, the output must go to -2 volts. Now, if $R_f$ is made 50,000 ohms, the output must still draw 0.2 mA to satisfy Kirchhoff’s law. In this case, the output must go to -10 volts to draw that current. In general, for the inverting amplifier with the positive input grounded,

$$A = \frac{R_f}{R_i} \quad (1)$$

Equation (1) assumes that the gain of the amplifier itself is infinite. Also, the input impedance is given by

$$Z_{in} = R_i \quad (2)$$

and the output impedance is very low, like the follower, and for the same reason.

Figure 6 shows another inverting amplifier, this time with many inputs. Because the summing mode is a virtual ground, the currents into it simply add, and no current from one signal source (represented here by $e_1$, $e_2$, $e_3$, and $e_4$) can get past this summing point to another source. The signals being mixed are therefore isolated. Current produced by the output through $R_f$ must equal the sum of the individual currents in order to ensure that the summing point stays at ground. The output voltage is therefore given by

$$e_{out} = -R_f \left( \frac{e_1}{R_1} + \frac{e_2}{R_2} + \frac{e_3}{R_3} + \frac{e_4}{R_4} \right) \quad (3)$$

It is not necessary for all input signals to be given the same gain before mixing. Each one is given its own weighting resistor (an analog computer term). Signals of widely differing natures may be amplified and combined in one circuit. Figure 7 is another example from real life. It is desired to digitize a waveform coming from a telemetry

![Figure 6](image)  
Figure 6. – Diagram of the weighted summing amplifier.

![Figure 7](image)  
Figure 7. – Circuit of weighted adding amplifier with gain and baseline controls.
system. This signal may have an undesired d-c component and may also be of the wrong gain. An engineering technician with an oscilloscope is required to "set up" the signal by giving it the correct gain and baseline. The circuit of Figure 7 is simply a weighted adding amplifier as just discussed. The two signals being added are the telemetry output and a d-c voltage. The gain of the telemetry signal is varied by adjusting \( R_1 \), and the offset is varied by adjusting the d-c voltage tapped off the divider formed by \( R_2, R_3, \) and \( R_4 \). Capacitor \( C_f \) serves to bypass any noise from the operation of \( R_4 \).

**NOTES.** — In order to protect the amplifier from saturation, overload, or destruction, a few tricks are commonly used. Figure 8 shows two diodes which protect the amplifier from an excessively large difference-mode input. If the difference-mode input voltage is only a few millivolts, both diodes are reverse-biased because of their forward voltage offset. If the difference exceeds a few tenths of a volt in either direction, one of the diodes turns on and shorts out the offending signal.

**Exercise Problem:**

1. Draw a circuit whose gain can be switch-selected as either -10, -1, or -0.1.

**Answer to Exercise Problem:**

1. 

![Diagram of the circuit showing diode connection to operational amplifier to prevent negative outputs.](image)

**Figure 9.** — Illustration to show diode connection to operational amplifier to prevent negative outputs.

![Diagram of the circuit showing Zener diode connected to prevent the output from going negative or into saturation.](image)

**Figure 10.** — Circuit diagram which shows Zener diode connected to prevent the output from going negative or into saturation.
Figure 10 shows a Zener diode being used as a two-way bound. Not only will the diode conduct in the forward direction and prevent the amplifier output from going negative, but it will also turn on in the reverse direction when the amplifier output passes 10 volts and prevent the amplifier from saturating.

Figure 11 shows two back-to-back Zener diodes in the feedback circuit. These diodes prevent saturation in both directions, positive and negative.

Figure 11. — Illustration to show diode connection to operational amplifier to prevent negative and positive saturation.
BASIC LOGIC FLIP-FLOPS

NAND GATE FLIP-FLOPS (RS FLIP-FLOP)

A basic Reset-Set flip-flop can be constructed by connecting two NAND gates as shown below.

The operation of an RS flip-flop is quite simple and should become clear after examination of the truth table shown below.

<table>
<thead>
<tr>
<th>INITIAL INPUTS</th>
<th>CONDITIONS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>S R Q Q Q Q Q</td>
<td>S R Q Q Q</td>
<td>S R Q Q</td>
</tr>
<tr>
<td>L H L H H L H</td>
<td>L H L H H</td>
<td>L H L H</td>
</tr>
<tr>
<td>H L H L L H H</td>
<td>H L H L L</td>
<td>H L H L</td>
</tr>
<tr>
<td>H H H H H H H</td>
<td>H H H H H</td>
<td>H H H H</td>
</tr>
<tr>
<td>L H L H H L H</td>
<td>L H L H H</td>
<td>L H L H</td>
</tr>
<tr>
<td>L L H H H L H</td>
<td>L L H H H</td>
<td>L L H H</td>
</tr>
<tr>
<td>L L H H H L H</td>
<td>L L H H H</td>
<td>L L H H</td>
</tr>
</tbody>
</table>

* AMBIGUOUS STATE

An ambiguous state results when both inputs are low at the same time; in practice the input that stays low longest will assume control.

CLOCKED NAND GATE FLIP-FLOPS (CLOCKED RS FLIP-FLOP)

The Reset-Set flip-flop can be clock-synchronized by the addition of a two-input NAND gate to both the set and the reset inputs (shown below). One of the inputs of each NAND is tied to a common clock or trigger line.

A change of state is inhibited until a positive clock pulse is applied. An ambiguous state will result if both the set and reset inputs are high when the clock pulse occurs. Refer to the truth table shown above.

Two types of general-purpose flip-flops are available which have built-in protection against the ambiguous state characteristic of NAND gate flip-flops.

D FLIP-FLOP

The first of these is the D flip-flop shown below.

The D flip-flop is a true leading (positive going voltage) edge triggered flip-flop and the D input is locked out until the clock input returns to low.

A single-ended data input (D) is connected directly to the set input. An inverter is provided between the input line (D) and the reset input. This ensures that the set and reset levels cannot be high at the same time.

The flip-flop proper employs three-input NAND gates to provide for DC set and reset inputs.

D flip-flops are especially suited to buffer register, shift register and binary ripple counter applications.

A characteristic of the D flip-flop which is not illustrated in the NAND gate equivalent circuit is the fact that the D input is locked out after the clock input threshold voltage on the leading (positive-going voltage) edge of the clock has been passed. The D input is not unlocked until the clock input threshold voltage of the trailing (negative-going voltage) edge has been passed.

MASTER-SLAVE J-K FLIP-FLOP

The second of these is the master-slave J-K flip-flop shown on page 2.
The master-slave J-K flip-flops transfer the information present at the J and K inputs just prior to and during the clock pulse to the master flip-flop when the threshold is passed on the leading (positive-going voltage) edge of the clock pulse. The information stored in the master flip-flop is transferred to the slave flip-flop, and consequently to the outputs, when the threshold is passed on the trailing (negative-going voltage) edge of the clock pulse.

The two unique features of a J-K flip-flop are: A) a clock pulse will not cause any transition in the flip-flop if neither the J nor the K inputs are enabled during the clock pulse, and B) if both the J and K inputs are enabled during the clock pulse, the flip-flop will complement (change states). There is no ambiguous state in the operation of a J-K flip-flop.

A word of caution is in order concerning the clock input. The J and K inputs must not be allowed to change states when the clock line is high, the output will complement on the negative-going voltage transition of the clock. It is for this reason that the clock line must be kept low until it is desired to transfer information into the flip-flop and no change in the states of the J and K inputs should be allowed when the clock line is high.

If the J input is enabled and the K input is disabled prior to and during the clock pulse, the flip-flop will go to the "1" condition when the trailing edge of the clock occurs. If the K input is enabled and the J input is disabled prior to and during the clock pulse, the flip-flop will go to the "0" condition when the trailing edge of the clock pulse occurs. If both the J and K inputs are enabled prior to and during the clock pulse, the flip-flop will complement when the trailing edge of the clock pulse occurs. If both the J and K inputs are disabled prior to and during the clock pulse, the flip-flop will remain in whatever condition existed prior to the clock pulse when the trailing edge of the clock pulse occurs.

Referring to the NAND gate equivalent circuit shown: Gates C and D are the master flip-flop and gates G and H are the slave flip-flop. Gates A and B are the steering network of the master flip-flop and the steering network for the slave flip-flop is comprised of gates E, F, and I.

The operation of the J-K flip-flop will be studied by examining the "1" to "0" transition of the flip-flops, with both the J and the K inputs enabled with a HI level before the clock pulse. When the leading edge of a HI clock pulse occurs, gate B will be enabled with three HI inputs. This will provide a RESET signal for the master flip-flop which will then go to the "0" condition. The slave flip-flop remains in the "1" condition while the clock pulse is HI because gate I is providing a LO signal to both gates E and F, thereby blocking inputs to the slave flip-flop. When the trailing edge of the clock pulse occurs, gate F will be enabled with a HI level at both its inputs and a RESET signal will be provided to the slave flip-flop, which will then go to the "0" condition. The other input signal conditions operate in a similar manner.

**FLIP-FLOP PROPAGATION DELAYS**

Propagation delays in any flip-flop is measured as the time between applying the required input until the flip-flop output changes; this is typically 30-35 ns. In the R-S flip-flop a low going set input will cause the "Q" output to go high. Typical timing is shown below.

<table>
<thead>
<tr>
<th>INITIAL INPUTS</th>
<th>CONDITIONS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>J  K Q Q</td>
<td>L L L L</td>
<td>H L</td>
</tr>
<tr>
<td>L L L L</td>
<td>H H L H</td>
<td>NO CHANGE</td>
</tr>
<tr>
<td>H H L H</td>
<td>L H L H</td>
<td>NO CHANGE</td>
</tr>
<tr>
<td>L L L L</td>
<td>H L L H</td>
<td>NO CHANGE</td>
</tr>
<tr>
<td>H H L H</td>
<td>* H L * H</td>
<td></td>
</tr>
</tbody>
</table>

* OUTPUTS COMPLEMENTED
Clocked RS flip-flop and D flip-flop propagation delays are measured from the leading or rising edge of a positive clock pulse. Data on the S and R or D inputs must be settled at least 20 ns prior to the clock transition. The advantage of leading edge triggering is that the flip-flop output will change while the clock pulse is still high. Typical timing is shown below.

When resetting ripple type counters (where the output of one flip-flop is used as the trigger input to the next stage) the reset pulse must be longer than the maximum propagation delay of a single stage. This will ensure that a slow flip-flop does not introduce a false transition, which could ripple through and result in an erroneous count.

J-K flip-flops are, in effect, trailing edge triggering devices. The only restriction on the J and K inputs is that they must be settled by the time that the rising edge occurs. Typical timing is shown below.

When using the DC set or reset inputs of D or J-K flip-flops: propagation delay is measured from the low going transition applied. Timing would be as shown for RS flip-flops.
HIGH SPEED LOGICS

For the purpose of this discussion, high speed logic has either or both of two characteristics: a) toggle rates over 50 MHz b) gate propagation delays under 6 ns. Only two types of standard high speed logic integrated circuits are commonly available in the marketplace; Schottky-clamped TTL logic (TTL-S), and non-saturating emitter-coupled logic (ECL).

Schottky-clamped TTL logic is similar to conventional TTL logic in its circuit configuration and operating characteristics. Conventional TTL is a saturated form of logic; that is, during turn-on, both the emitter-base and collector-base junctions of a transistor are forward biased, causing an accumulation of charged carriers in the base regions. Then, when the transistor is turned off, this charge must discharge through the collector. The finite time required for this charge to dissipate causes a delay in turning the transistor off. This "storage time" delay is an integral part of all saturated logic forms. Schottky-clamped TTL logic reduces storage time by means of Schottky-diodes between base-collector junctions. These diodes tend to keep the transistor out of saturation, but they also tend to increase the input capacitance of the Schottky-clamped transistor. Thus, while the speed of TTL-S is greater than that of TTL, due to a reduction in storage time, it is limited by the RC time constant of the transistor input.

Emitter-Coupled Logic, being non-saturating by design, completely avoids transistor storage time and its attendant speed limitation without the tradeoffs inherent in TTL-S. Gate delays of less than one nanosecond and operating frequencies approaching one gigahertz are currently feasible, and even these are not ultimate limits.

The term MECL identifies Motorola's emitter-coupled logic. Emitter-coupled logic is a non-saturating form of digital logic which eliminates transistor storage time as a speed limiting characteristic, permitting very high speed operation. "Emitter-Coupled" refers to the manner in which the emitters of a differential amplifier within the integrated circuit are connected. The differential amplifier provides high impedance inputs and voltage gain within the circuit. Emitter follower outputs restore the logic levels and provide low output impedance for good line driving and high fanout capability.

HISTORY OF MECL

Motorola offers MECL circuits in four logic families: MECL I, MECL II, MECL III, and MECL 10,000.

The MECL I family was the first digital monolithic integrated circuit line produced by Motorola. Introduced in 1962, MECL I was considerably beyond the state-of-the-art at that time. Several years passed before any other form of logic could equal the 8ns gate propagation delays and 30 MHz toggle rates of MECL I. As a result of its reliability and performance, MECL I was designed into many advanced systems.

In 1966 Motorola introduced the more advanced MECL II. The basic gate featured 4ns propagation delays and toggle rates over 70 MHz. MECL II immediately set a new standard for performance that has been equaled by non-ECL logic only with the introduction of Schottky TTL in 1970.
Motorola continued with the development of MECL II and flip-flop speeds were increased first to 120 MHz, and then to 180 MHz. To drive these high speed flip-flops, high speed line drivers were introduced with 2ns propagation delays and 2ns rise and fall times. With 2ns edges, transmission lines could be used to preserve the waveforms and limit overshoot and ringing on longer lines. Consequently, gates were designed to drive 50 ohm lines. Because of the significant speed increase of the line drivers and high speed flip-flops over the basic MECL II gates, these circuits are commonly called MECL II-1/2, although they are part of the MECL II family.

Complex functions became available in MECL II when trends shifted toward more complicated circuits. The family now has adders, data selectors, decoders, multiplexers, and decoder/drivers just to name a few. MECL II is a growing line, with new devices currently being designed and introduced.

Motorola's continuing development of ECL made possible an even faster logic family. As a result, MECL III was introduced in 1968. Its ins gate propagation delays and greater than 500 MHz flip-flop toggle rates remain the industry leaders. The ins rise and fall times require a transmission line environment for all but the smallest systems. For this reason, all circuit outputs are designed to drive transmission lines and all output logic levels are specified when driving 50 ohm loads. Because of MECL III's fast edge speeds, multi-layer boards are recommended above 200 MHz. For the first time with MECL, internal pulldown resistors are included with the circuits to eliminate the need to tie unused inputs to VEE. The Hi-Z 50K ohm input resistors are used with transmission lines for most applications. Optional Low-Z 2K ohm input resistors can be used in place of pulldown resistors when the chips are used in a hybrid circuit or when line lengths are very short.

Trends in large high speed systems have shown the need for an easy to use logic family with 2ns propagation delays. To fill this requirement, Motorola introduced the MECL 10,000 series in 1971. In order to make the circuits comparatively easy to use, edge speed was slowed to 3.5ns while the important propagation delay was held to 2.0ns. The slow edge speed permits use of wire wrap and standard printed circuit lines. However, the circuits are specified to drive transmission lines for optimum performance.

MECL 10,000 is provided with logic levels that are completely compatible with MECL III to facilitate using both families in the same system. A second important feature of MECL 10,000 is the significant power reduction. MECL 10,000 gates use less than one-half the power of MECL III or high speed MECL II gates. Finally, the low gate power and advanced circuit design techniques have permitted a new level of MECL complex circuits.

The basic MECL 10,000 series has recently been expanded by a subset of devices with even greater speed. This additional series provides a selection of toggle rates over 200 MHz. The MECL 10,200 series is meant for use in critical timing chains, and for clock distribution circuits. MECL 10,200 gates are otherwise identical to their MECL 10,000 series counterparts (subtract 100 from the MECL 10,200 type number to obtain the equivalent standard MECL 10,000 gate number).

**MECL FAMILY COMPARISONS**

Although the basic design of all MECL families is the same, there are differences other than the speed and power capabilities. Comparisons of the key characteristics of each family are given in Table 1.
Table 1 - MECL FAMILY COMPARISONS

<table>
<thead>
<tr>
<th>Feature</th>
<th>MECL I</th>
<th>MECL II</th>
<th>MECL 10,000</th>
<th>MECL III</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Propagation Delay</td>
<td>8 ns</td>
<td>4 ns</td>
<td>2 ns</td>
<td>1.5 ns</td>
</tr>
<tr>
<td>Gate Edge Speed</td>
<td>8.5 ns</td>
<td>4 ns</td>
<td>3.5 ns</td>
<td>2.5 ns</td>
</tr>
<tr>
<td>Flip-Flop Toggle Speed (min)</td>
<td>30 MHz</td>
<td>70 MHz</td>
<td>125 MHz</td>
<td>200 MHz</td>
</tr>
<tr>
<td>Transmission Line Capability</td>
<td>No</td>
<td>On Some Devices</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Output Pulldown Resistors</td>
<td>Yes</td>
<td>Optional</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Input Pulldown Resistors</td>
<td>No</td>
<td>No</td>
<td>50K ohms</td>
<td>50K ohms</td>
</tr>
<tr>
<td>Separate Vcc Inputs</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Bias Driver Source</td>
<td>External</td>
<td>Internal</td>
<td>Internal</td>
<td>Internal</td>
</tr>
</tbody>
</table>

WHY USE MECL?

Circuit speed is, of course, an obvious reason for using MECL. MECL III is significantly faster than any other digital logic family. MECL 10,000 offers shorter propagation delays and higher toggle rates than any non-ECL type of logic. Equally important to the circuit speed are the characteristics of MECL circuits which permit entire systems of operate at high speeds.

The ability of the faster MECL families to drive transmission lines becomes increasingly important in larger and faster systems. Unlike non-ECL forms of logic, MECL circuits have constant power supply requirements, independent of operating frequency.

In addition to faster operation, the line driving features of MECL circuits can be used to improve system performance. For one, the parts specified to drive transmission lines will drive coaxial cables over distances limited only by the bandwidth of the cable. In addition, the shielding in coaxial cable gives good isolation from external noise. More economical than using coaxial cable, is the ability of MECL circuits to differentially drive and receive signals on twisted pair lines.

The complementary outputs and Wired-OR capabilities of MECL circuits result in faster system operation with fewer chips and less power used. The complementary outputs are inherent in the circuit design and both outputs have equal propagation delay. This eliminates the timing problems associated with using an inverter to get a complement signal. The Wired-OR function is obtained by wiring circuit outputs together. The propagation delay of the Wired-OR connection is much less than a gate function.

Another advantage with MECL is the low noise generated by the circuits. Unlike totem-pole outputs, the emitter follower does not generate a large current spike when switching logic states, so the power lines stay comparatively noise free. The low current-switching in signal paths, relatively small voltage swing (typically 800 mv), and low output impedances, cut down crosstalk and noise.

Generated noise is also reduced by MECL’s relatively slow rise and fall times. For each MECL family the edge speed is equal to or greater than the propagation delay. The low noise associated with MECL is especially important when the logic circuits are to be used in a system which contains low level analog or communications signals.

The flexibility of the MECL line receivers and Schmitt Triggers to act as linear amplifiers leads to many functions that may be performed with standard MECL
circuits. For example, in addition to amplifying low level signals to MECL levels, these MECL circuits can be used as crystal oscillators, zero crossing detectors, power buffers, Schmitt triggers, RF and Video amplifiers, one-shot multivibrators, etc.

THE ADVANTAGES OF MECL

1. Highest speed IC logic available
2. Low output impedance
3. High fanout capability
4. Constant supply current as a function of frequency or logic state
5. Very low noise generation
6. Complementary logic outputs
7. Low crosstalk between signal leads
8. All outputs are buffered
9. Outputs can be tied together giving the Implied-OR function
10. Common mode rejection of noise and supply variations is 1 v or greater for differential line receiving
11. Bias supplies are internal, allowing MECL use with a single power supply
12. Easy data transmission over long distances by using balanced twisted pair
13. All positive logic functions available

THE BASIC MECL GATE

An understanding of the basic circuits used in the construction of a logic family is important in order to successfully trouble-shoot a system which uses the family.
The typical MECL gate circuit, Figure 1, consists of a differential amplifier input circuit, a temperature and voltage compensated bias network, and emitter follower outputs to restore DC levels and provide buffering for transmission line driving. High fanout operation is possible because of the high input impedance of the differential amplifier input and the low output impedance of the emitter follower outputs. Power supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function.

Any of the power supply levels, \( V_{BB} \), \( V_{CC} \), or \( V_{EE} \) may be used as ground; however, the use of the \( V_{CC} \) node as ground results in best noise immunity. In such a case: \( V_{CC} = 0 \), \( V_{BB} = -1.15 \) to \(-1.3 \) V (depending on the specific MECL family), and \( V_{EE} = -5.2 \) V.

The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, Figure 2, varies from a "low" state of \(-1.75 \) V to a "high" state of \(-0.9 \) V with respect to ground. (These logic levels are valid for the MECL 10,000 and MECL III families. MECL I and MECL II logic levels differ slightly.) Positive logic is used when reference is made to logical "0's" or "1's"; thus typically "0" = \(-1.75 \) V or "low" and "1" = \(-0.9 \) V or "high".

![Figure 2 - GATE TRANSFER CURVES](image-url)

Circuit operation can be explained by beginning with all logic inputs "low" (\(-1.75 \) V); assume that Q1 through Q4 are cut-off because their P-N base-emitter junctions are not conducting, and the forward-biased Q5 is conducting. Under these conditions, with the base of Q5 held at \(-1.29 \) V by the \( V_{BB} \) network, its emitter will be one diode drop (0.8 V) more negative than its base, or \(-2.09 \) V. (The 0.8 V differential is a characteristic of this P-N junction.) The base-to-emitter differential across Q1 through Q4 is then the difference between the common emitter voltage (-2.09 V) and the "low" logic level (\(-1.75 \) V) or 0.34 V. This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut-off.

When any one of the logic inputs are shifted upward from the \(-1.75 \) V "low" state to the \(-0.9 \) V "high" state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the
Figure 3 - MECL FAMILY COMPARISONS
voltage at the common emitter point rises from -2.09 v to -1.7 v (one diode drop below the -0.9 v base voltage of the input transistor), and since the base voltage of the fixed bias transistor (Q5) is held at -1.29 v, the base-emitter voltage of Q5 cannot sustain conduction. Hence, this transistor is cut-off.

This action is reversible, so that when the input signal(s) return to the "low" state, Q1 through Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1 through Q5 are transferred through the output emitter-followers to the output terminals. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

The bias voltage applied to the bias input is normally obtained from circuitry on each individual chip, except in the MECL I series for which separate bias drivers are available. The temperature characteristics of the bias driver compensate for any variations in circuit operating point over the temperature range or supply voltage changes, to insure that the threshold point is always in the center of the transfer characteristic curves. The separate bias driver of MECL I can be used to drive up to 25 logic elements and should be employed for all elements except those with built-in bias networks.

VARIATIONS AMONG MECL FAMILIES

The basic gate circuits of the four MECL families are illustrated in Figure 3. From these diagrams, it is evident that some variations were employed as technology advanced. The first of these is that the bias driver for the MECL I gates is not included on the chip, whereas all subsequent series have this as an internal feature.

Second, most corresponding resistor values differ among all MECL families. This difference is necessary to achieve the varying speed and power improvements of the different families. Of course, speed is not determined by resistor values alone. Transistor geometries, while not represented on a schematic, are a major determinant. The transistor geometries in conjunction with the resistor values provide the speed and power characteristics of the different families.

Third, it will be noted that MECL III and MECL 10,000 gates are supplied with base pull-down resistors in each of the input transistors while the other two families are not. These resistors provide a path for base leakage current to unused input bases, causing them to be well turned off. Where these resistors are not used, any unused inputs must be externally tied to a suitable negative potential, e.g. VEE.

A final significant difference between the families is in the output circuits. MECL I circuits normally are supplied with output pull-down resistors on the chip. MECL II circuits can be obtained with or without output resistors. MECL III and MECL 10,000 circuits normally have open outputs.

The use of on-chip output resistors has both advantages and limitations. On the plus side is the obvious advantage that you require fewer external components. On the minus side is the fact that wire-Oring capability with on-chip pull-down resistors is limited. Moreover, with open outputs the designer can choose both the value and location of his terminating resistance to meet system requirements. And finally, the use of external resistors reduces on-chip heating and power dissipation, allowing more complex LSI and increasing chip life and reliability.
MECL CIRCUIT TYPES

It is possible to connect the basic MECL differential amplifiers together within a circuit to increase logic flexibility, speed, and power efficiency. Two techniques, series gating and collector dotting, add the AND and NAND logic functions to the basic OR and NOR operation of the MECL gate with very little increase in propagation delay. A third technique, Wired-OR, gives the logic OR function by tying together two or more emitter-follower transistors. This is used internally in complex functions to save speed and power and, unlike collector dotting, may also be used externally by connecting logic outputs together.

Series gating is accomplished by connecting MECL differential amplifiers in a current-switch tree, building up from a current source, Q1 as shown in Figure 4. The A input controls the switch, Q2/Q3 through the level shifter Q8 and the associated resistor diode network. The bias network is modified to provide the proper voltage level at Q3, a level which is lower than that on Q5 and Q7. The two upper differential amplifiers are controlled by inputs B and C. The overall circuit generates the four logic functions as indicated. MECL circuits use up to three levels of series gating, permitting up to eight logic functions with one current source.

Figure 4 - SERIES GATING
The propagation delay from an input, to a top current switch is approximately one gate delay. The propagation delay from an input to a lower level current switch is slightly longer because of the input level shifter Q6. Typically, the latter takes about 1.5 gate delays.

Because of the bias network design, some of the MECL II series gated circuits require unused inputs be connected to "low" potential instead of to the normal VEE.

Series gating is an advantage in MECL logic since it provides the AND and NAND logic functions. Together with the OR and NOR function of the basic gate, MECL has the four basic logic functions needed for efficient logic design. Series gating is used internally in most MECL complex functions and flip-flops.

Collector dotting is a second logic technique which is used in the MECL 10,000 series. With it, the AND function can be generated by interconnecting one collector node of separate differential amplifiers as shown in Figure 5. When connected this way, the two 2 input OR gates give the AND logic function as indicated.

Only one collector resistor (Rc) is used for the two transistors Q1 and Q2. The interconnection requires that at least one input to each gate be at a logic 1 level for the output to be at a the logic 1 level. Since it is possible to have both Q1 and Q2 conducting at the same time (all inputs "low"), a clamp is used to limit the current in Rc and maintain the output 0 logic level. This clamp consists of Q3 and R1. They insure that the Q1/Q2 collector node never goes too far negative. Propagation delays for all inputs to collector dotted circuits are equal and are typically about 20% greater than the basic gate delay.

The collector dot (OR-AND) logic function, series gating, and the wired-OR characteristics of MECL combine to provide the means for designing very efficient and fast complex logic functions.

Figure 5 - COLLECTOR DOTTING
MECL FLIP-FLOPS

In addition to the basic gate, the flip-flops in a logic line provide a necessary building block. MECL employs two types of flip-flop circuits; the ac coupled JK flip-flops found in MECL I and MECL II, and the direct coupled master-slave flip-flops used in MECL II, MECL III, and MECL 10,000.

The MECL II ac coupled flip-flops are characterized by small capacitors (25 to 30 pf) coupling the J and K inputs to the storage section of the circuit. Because of this capacitive coupling, the circuit is somewhat sensitive to input rise time. However, the circuits will trigger on signals of MECL amplitude with edges up to 100 ns long - much longer than any MECL edge.

A limitation on these flip-flop circuits is their susceptibility to some types of noise on the input line. For example, a positive going input with a large overshoot on a J input will override a 1 level on another J input intended to inhibit that positive going input. The overshoot will couple through the capacitor and will look like a J input. A similar condition exists on the K inputs. Fortunately the problem is not a serious one and its solution requires only that the input signals do not have excessive ringing.

The MECL II type D, and all MECL III and MECL 10,000 flip-flops, use a direct coupled master-slave circuit. In each direct coupled circuit the master is updated while the clock is "low", and data is transferred to the slave on the positive excursion of the clock. This type of circuit offers better noise protection than the ac coupled circuit and is not susceptible to overshoot on the inputs. Also, the master-slave flip-flops do not have the rise time limitations of the ac coupled circuits.

INTERFACING MECL TO SLOWER LOGIC TYPES

MECL circuits are interfactable with most other logic forms. For MECL/MTTL/MDTL interface, when MECL is operated at the recommended -5.2 volts and TTL/DTL at +5 volts, currently available translator circuits may be used. For systems where a dual supply (-5.2 v and +5 v) is not practical, a discrete component translator can be designed.

MECL also interfaces readily with MOS. With CMOS operating at +5 volts, any of the MECL to TTL translators works very well. On the other hand, CMOS will drive MECL directly when using a common -5.2 volt supply. P-channel MOS, operating with a negative supply, requires simple translators to equalize the differing logic levels.

Complex MECL 10,000 functions are presently under development for use to interface MECL 10,000 with MOS logic, MOS memories, TTL tri-state circuits, and IBM bus logic levels.
The 3305593-01 Extender Board used on the DM-940/980 drives is not compatible with the DM-9160. The 3305593 board has Pins 55 and 56 tied together and 81 and 82 tied together. These pins were reserved for +15V and -15V. However due to the need for extra I/O pins on the DM-9160, these pins must now be separated.

The part number for a DM-9160 Extender Board is 3307873-01. The DM-9160 board is downward compatible to the DM-940/980.

Alternatively the 3305593-01 board can be modified to work in DM-9160 and maintain compatibility to DM-940/980 by installing FCO #232.
The following procedures are used to factory select values for the following adjustments:

I. PLO Adjustment (U24)
   1. With heads retracted, hang frequency meter on pin 53.
   2. Looking for $403 \pm \frac{0}{3}$ kHz tolerance (range from 400-403 kHz).
   3. Combination of C39, C48 is used to select frequency. Possibly need to select C47 if it cannot be done with combination of C39 and C48. Silver-mica capacitors must be used.

II. Heads Loaded Adjustment (U23)
   1. With heads retracted, hang frequency meter on U23, pin 5.
   2. Looking for $403 \pm \frac{0}{3}$ kHz tolerance (range from 400-403 kHz).
   3. Select R83 for above frequency range. May need to select different metal film resistor R82 if tolerance cannot be reached.

III. 9.67 MHz Clock Phase Adjustment (U3)
   1. Scope sync. Chan 1, pin 51 (806 kHz).
   2. Scope Chan 2, pin 2B (9.67 MHz).
   3. Look at TP2 and adjust R171 to +4V or as positive as it will go and insure that two signals are in phase with each other. Typically, this in phase condition occurs at 2.5 to 3.0 but still adjust to as positive as it will go.
The DM900/9000 Series Drives have been U.L. approved. One of the requirements for U.L. approval was to tie the deck plate (DC ground) to frame ground (AC ground).

On DM9000 drives this braided wire is located on the rear left corner of the deck plate.

On recent shipments of DM900 drives the wire is located between the AC ground lug and the DC ground lug on the rear pan of the drive. This green wire is on the inside of the pan.

If there is no wire present, the AC and DC are tied together on the ground lug located in front of T81. Raise the deck plate and remove the 3 green wires on this lug. Ohm between the deck plate and each of these 3 wires. Find the wire that has continuity to the deck plate, insulate the lug and tie back in the harness to avoid contact with the pulley or belt on the deck plate.

For systems that tie AC and DC ground together at one central point either controller or CPU these grounds in the drive, in effect put additional ground loops into the system which may cause intermittent problems on the drives, i.e., select locks, read or seek errors.

For systems that do tie AC and DC ground together removal of the internal drive AC to DC ground wire may be necessary.

To insure that the system does in fact tie the two together, do the following:

1. Remove the AC to DC ground wire in the drive.

2. With all cables removed from drive, ohm between AC ground (frame) and the deck plate (DC ground), must read open. If not, another AC to DC ground short of some kind may be present in the drive. This will have to be found and isolated.

3. Reattach cables from system to drive and verify that AC to DC ground is shorted together.

4. Only if this condition has been met should the grounds be removed in the disk drives.
HEAD INSPECTION

All heads should be inspected a minimum of once a month and possibly more frequently, (reference FEB 135,034, suggested PM on DM-900/9000 Series Disk Drives) or anytime operating personnel report suspected head-to-disk interference (HDI).

1) Ensure drive primary power switch is off.
2) Remove disk pack.
3) Move the carriage to a point just before the cam follower allows the heads to load. Exceeding this point will allow heads to slap together causing possible head damage.
4) Using a dental mirror and light, inspect each head for signs of contamination. Normal dirt build-up will appear as a black build-up on the head shoe trailing edges.

![Diagram showing head shoe trailing edge and gimbal spring]

Brown or black build-up appearing on the shoe surface would indicate excessive length of time between PM intervals. Red or heavy black oxide streaks would indicate possible HDI. In both cases disk packs should be inspected and cleaned. Inspection and cleaning should be done by the appropriate pack vendor or a pack inspection service company with the proper equipment.

5) Head attitude should be looked at. Heads will appear as follows looking from the front. Will be difficult to see on DM900 drives due to pack shroud.

Correct View

Exaggerated View

Incorrect View
Incorrect attitude will cause HDI immediately or excessive oxide build-up usually on the leading edges over several load unload cycles. Heads must be replaced.

6) The gimbal spring that the head shoe is mounted on should be looked at for any abnormal bends. This acts as a pivot to allow the head to fly at the correct distance from the disk surface. Any sharp bends or kinks may result in HDI. These heads must be replaced.

NOTE: After replacing R/W heads or the servo head, Items 5 and 6 should be checked prior to head load as well as inspection/cleaning of new heads if necessary.

HEAD CLEANING
When contamination is found, head cleaning is necessary.

1) Using a head cleaning paddle, dampen (not soak) a lint-free material with 91% isopropyl alcohol and with a right to left motion gently wipe the shoe with flat, even pressure. Ensure that the paddle with tissue is less in width than the space between the heads. Do not use excessive force to clean the head shoe as the gimbal spring may be deformed.

2) Wrap a dry lint-free material on the head cleaning paddle and repeat the right to left motion cleaning off the alcohol residue.

3) After cleaning if oxide or black contamination is present and cannot be removed with moderate pressure, then that head(s) must be replaced.

NOTE: Ensure pack(s) are inspected and cleaned if the above case is found on head(s). Inspection and cleaning should be done by the appropriate pack vendor or a pack inspection service company with the proper equipment.

If head(s) are excessively dirty but clean up, make a note of that head. If it is found excessively dirty on the next succeeding PM, then that head or pack(s) may need to be replaced. Ensure pre-filters and absolute filter are clean (reference Absolute Filter Check, FEB 135,036).

4) Reposition the carriage in the retracted position.

5) Apply primary power to disk drive.

LIST OF DON'Ts

INSPECTION
1) Do not pry heads apart for a better look at shoe while inspecting heads.
2) Do not position mirror so that you can easily scratch shoe.
CLEANING

1) Do not soak lint-free material with alcohol.

2) Do not use Q-tips or any non-lint-free substance, as they leave particles which will cause HDI.

3) Do not use any cleaning agent other than 91% isopropyl alcohol. Drug store alcohol is usually not acceptable.
A new Read/Write Cable is now available for the DM-940/980 Round Cable interface drives. This cable, P/N 3310317-XX has replaced P/N 3305668-XX, and is pin for pin compatible. The new cable incorporates a right angle entry of the cable to the hood, and improved strain relief. All new DM-940/980 disk drives will ship with the new cable. If your application requires a cable with the right angle entry, contact sales to order the new style on an exchange basis.
GOOD MORNING - WELCOME TO AMPEX

We want your training session to be as profitable and as comfortable as possible, so while you're attending this class in Redwood City, here are some "Helpful Hints" to make your stay an enjoyable one.

1. **CLASS HOURS:** Our classroom hours are 8:30 - 12:00 and 1:00 - 4:30, with coffee breaks at approximately 10:30 and 2:30.

2. **MEALS:** The Ampex Cafeteria, located east of here near the Corporate Headquarters Building, serves an excellent variety of moderately priced meals. It is open 7:00 - 8:00 a.m. for breakfast and is open for lunch as well. A coffee truck also stops in front of Bldg. 2 at about 8:25 a.m. At the corner of Broadway and Woodside Road about three blocks away, is Denny's open 24 hours. At the corner of Woodside Road and Bay Road, in the Shopping Center, there is a delicatessen and a pizza and sandwich shop which you might like to try for lunch. For evening dining, El Camino Real (State Highway 82), where your motel is probably located, is also "restaurant row" for most of the small cities on the San Francisco peninsula. A little exploration between San Carlos on the north and Mountain View on the south, about twenty miles or less, should produce many good meals for you. San Francisco itself is noted for its fine restaurants and varied cuisines.

3. **MESSAGES & MAIL:** These will be posted on the Message Board located in the hall outside each classroom. It is your responsibility to check the board for messages since none will be delivered personally to you in class unless they are of an emergency nature.

4. **CASHING CHECKS:** The nearest bank is a branch of Wells Fargo at the corner of Broadway and Main in Redwood City, about six blocks west of Bldg. 2. Please check with Training Department office for bank identification.

5. **AIRLINE RESERVATIONS & CONFIRMATIONS:** The Training Department office staff will be happy to assist with these.

6. **OUTGOING TELEPHONE CALLS:** It is the policy of Ampex that outgoing calls must be made on a collect or credit card basis and applies to both Ampex personnel and customers. There are four telephones, three Ampex lines and one coin, in the Training Office for use. Since the Training Department office staff control these phones from their desks, all calls must be placed by them, except those from the pay phone. Please remember that there is usually a large number of people waiting to use these phones and try to limit your conversation accordingly.

---

James C. Lawson  
Manager, Training Department
AMPEX TECHNICAL SUPPORT SERVICES

AUDIO/VIDEO PRODUCTS

AMPEX CORPORATION
401 Broadway
Redwood City, CA 94063

Attention: AVSD Technical Support
Mail Stop 3-46

Telephone: (415) 367-3014
(415) 365-0661

8:00AM - 5:00PM
AFTER HOURS, WEEKENDS, HOLIDAYS

INSTRUMENTATION PRODUCTS

AMPEX CORPORATION
401 Broadway
Redwood City, CA 94063

Attention: DSD Technical Support
Mail Stop 10-16

Telephone: (415) 367-3006,
3007, 3008

8:00AM - 5:00PM

DISK PRODUCTS

AMPEX CORPORATION
1024 Kifer Road
Sunnyvale, CA 94086

Attention: Disk Technical Support
Mail Stop 900-10

Telephone: (408) 738-4910

8:00AM - 5:00PM

When ordering emergency parts, please be as specific as possible regarding part and equipment identification, shipping instructions and purchase order information when applicable.
MANUAL SHIPPING INFO

Ampex will ship your training manuals to your home or business establishment as follows:

1. You may ship via surface, COLLECT ONLY.

2. UPS BLUE LABEL - PREPAID - (Air shipped by United Parcel Service). If you are uncertain if your area has this particular service, ask Staff as some areas do not. We will give you approximate cost and receipt for your prepayment if you choose this manner of shipment.

3. UPS REGULAR (Surface) - PREPAID - Same as #2.

4. The U.S. Post Office is on Broadway, approximately three blocks from here. We will box your books for you if you wish to take them to the post office for shipment.

5. CANADIAN SHIPMENTS - Surface or Air Freight, COLLECT. On Canadian shipments via AIR, please note airport nearest your business and add your telephone number for notification of arrival.

If you wish Ampex to ship for you, please PRINT CLEARLY your name and address (no P.O. Boxes), method of shipment - surface, air freight, COLLECT, or UPS PREPAID - and leave with your books on your table in your classroom.
Ampex Corp.
Memory Products Division
200 North Nash Street
P.O. Box 999
El Segundo, CA. 90245
Mail Stop 900-02
Ph. (213) 640-0150

Connie Gates
The following people are attending courses in Redwood City:

<table>
<thead>
<tr>
<th>NAME</th>
<th>COMPANY</th>
<th>COURSE &amp; INSTRUCTOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Robert J. Ainsworth</td>
<td>Cray Research, Chippewa Falls, WI</td>
<td>DM-960/9160</td>
</tr>
<tr>
<td>Reg Lustenhouwer</td>
<td>TCG Systems Automation, Sydney, Australia</td>
<td>Sept 10-14, 1979</td>
</tr>
<tr>
<td>Michael Csteen</td>
<td>KALBRO, La Mesa, Ca.</td>
<td>Jack Cox</td>
</tr>
<tr>
<td>Edward Coran</td>
<td>General Electric, Oakbrook, Il.</td>
<td></td>
</tr>
<tr>
<td>Ken Jennings</td>
<td>University of New Mexico, Armidale, N.S.W., Australia</td>
<td></td>
</tr>
</tbody>
</table>