TA11 cassette system
maintenance manual

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CHAPTER 1
INTRODUCTION

INTRODUCTION
This manual describes the operation and maintenance of the TA11 Cassette System Interface. The TA11 is a dual cassette magnetic tape system for use with PDP-11 family computers. Its two drives run nonsimultaneously using Philips-type cassettes. The TA11 system comprises three elements: one TU60 Dual Cassette Transport, one M7892 Control module, and two BC08-S interconnection cables. This manual contains details of the TA11 system and the TA11 control module. The TU60 transport is described in a separate manual (Paragraph 1.4).

1.1 PHYSICAL DESCRIPTION
The TA11 is available in two configurations depending on input voltage requirements. The TU60 transport requires 5-1/4 in. of vertical space in a standard 19-in. rack. The M7892 Control module is quad sized and is designated as a small peripheral controller (SPC) that mounts in any SPC slot, such as in the DD11-A, DD11-B, and in most PDP-11 family processors. The TU60 transport connects to the M7892 Control module through the two BC08-S interconnecting cables. Communication between the M7892 Control module and the rest of the system is through the Unibus, and power for the M7892 Control module is derived from the power supply of the box it is mounted in. Figure 1-1 is a simplified block diagram of the interconnections between the TU60 transport, the M7892 Control module, and the Unibus.

![Figure 1-1 TA11 Simplified Block Diagram](image)

1.1.1 Specifications
TA11 specifications are given in Table 1-1.

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<th><strong>Table 1-1</strong></th>
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<td><strong>Recording Medium</strong></td>
<td>0.150 in. wide, 1 mil thick by 150 ft long magnetic tape; proprietary DEC “Philips-type” cassette</td>
</tr>
<tr>
<td><strong>Recording type</strong></td>
<td>Phase encoded, blocked</td>
</tr>
<tr>
<td><strong>Capacity</strong></td>
<td>Full tape 93,000 bytes minimum; with 256 byte blocks, 87,000 bytes minimum. Subtract 300 bytes for each file gap.</td>
</tr>
<tr>
<td><strong>Transfer rate</strong></td>
<td>560 bytes/sec (peak); with 256 byte block, 487 bytes/sec (average)</td>
</tr>
<tr>
<td><strong>Data format</strong></td>
<td>Variable block length, 1 byte minimum, no maximum hardware-formatted with length software-controlled</td>
</tr>
<tr>
<td><strong>Recording density</strong></td>
<td>350-700 bits/in.</td>
</tr>
<tr>
<td><strong>Drive method</strong></td>
<td>Direct reel-to-reel</td>
</tr>
<tr>
<td><strong>Read/Write speed</strong></td>
<td>9.6 in./sec average</td>
</tr>
<tr>
<td><strong>Space file fwd/rev speed</strong></td>
<td>22 in./sec average</td>
</tr>
<tr>
<td><strong>Rewind speed</strong></td>
<td>100 to 150 in./sec</td>
</tr>
<tr>
<td><strong>Data transfer rate</strong></td>
<td>562 bytes/sec maximum</td>
</tr>
<tr>
<td><strong>Latency (TRANSFER REQUEST)</strong></td>
<td>1.8 ms</td>
</tr>
<tr>
<td><strong>Latency (READY)</strong></td>
<td>None; asynchronous</td>
</tr>
</tbody>
</table>
| **Register addresses** | TACS – 777500  
TADB – 777502 |
| **Vector address** | 260 |
| **Priority level** | 6 |
| **Error rates** | 1 in 10⁷ bits soft error  
1 in 10⁸ bits hard error (3 retries on soft errors) |
| **Power requirements** | TU60 transport: 90 to 132V 48–63 Hz or 180 to 256V 48–63 Hz  
120W maximum  
M7892 Control module: 5 Vdc ± 5%, 1.5A |
| **Physical dimensions** | TU60 transport: 5-1/4 in. H x 19 in. W x 18-1/4 in. D  
M7892 Control module: quad-sized DEC Flip Chip |
1.1.2 Equipment Supplied
The equipment supplied comprising the TA11 is as follows:

- TU60 Cassette Tape Transport
- M7892 Control Module
- BC08-S-15 Interconnecting Cables (2)
- DEC-150 Cassette Tapes (2) PN 36-11226
- LIBKIT 11-TA11 (on cassette)
- Maintenance Manual DEC-00-TU60-DA
- TA11 Engineering Drawings Manual B-DD-TA11

1.2 RECORDING METHODS AND DATA FORMATS
In the TA11 Cassette System, data is recorded on tape in a single bit-serial track of data. Since there is no prerecorded timing or format track (such as in DECTape), data must be sequentially recorded and retrieved as in conventional mag-tape systems. A sample tape format is shown in Figure 1-2.

![Figure 1-2 Sample Tape Format](image)

The cassette medium is an oxide-coated tape with sections of clear leader (no oxide) appended to both ends. Data cannot be recorded in these clear leader sections, but they identify BOT (beginning of tape) and EOT (end of tape). Placement of data onto the recordable region of the cassette tape is organized into units called files. Adjacent files are separated by file gaps, which are generated under software control. Each file consists of one or more blocks separated by automatically generated block gaps. Each block consists of one or more bytes of data and two cyclic redundancy check (CRC) bytes. Under program control, the CRC bytes are appended when a block is written and checked when a block is read. Each byte consists of eight bits (no parity).

The initial gap on tape between clear leader and the first block of data is termed load point gap. It is essentially an extended file gap that is invisible to most tape operations, but has some special significance.
The number of files, blocks per file, and bytes per block is unrestricted except for the tape capacity. Because of the requirements for generation of the block and file gaps, the preamble, and the CRC bytes, the tape capacity, read rate, and write rates are a function of the block length. Figure 1-3 shows this relationship.

![Graph showing TA11 Capacity and Data Rate vs Block Length](image)

**Figure 1-3** TA11 Capacity and Data Rate vs Block Length

### 1.3 CYCLIC REDUNDANCY CHARACTER (CRC)

The CRC bytes are read and written under program control. Two CRC bytes are computed by the TU60 hardware during a write operation. These bytes comprise a 16-bit word and are written onto the tape at the end of each block of data. The CRC word is read at the end of each read cycle and compared with the CRC word just computed during the cycle to determine if data bits were picked up or lost. If an error is detected, a CRC ERROR signal is generated by the TU60 and sent to the control module. A complete description of CRC generation and error checking operations is contained in the *TU60 Cassette Tape Transport Maintenance Manual*.

### 1.4 COMPANION DOCUMENTS

The following documents are required to operate and maintain the TA11:

- PDP-11/* Processor Handbook
- PDP-11 Peripherals and Interfacing Handbook
- TU60 Cassette Tape Transport Maintenance Manual, DEC-00-TU60-DA
- Tech tip “PDP-11 Systems”

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*Appropriate Processor Handbook for the particular processor used with the system.*
CHAPTER 2
INSTALLATION AND ACCEPTANCE TESTS

This chapter contains the installation and check-out procedures for the TA11. The TA11 is installed on-site by DEC Field Service personnel; no attempt to unpack, install, check-out or service the equipment should be made by customer personnel.

2.1 SITE PREPARATION
Unpack and inspect the equipment for damage that may have occurred in transit. Report any damage to the carrier and to Digital Equipment Corporation. Ensure that all items listed in Paragraph 1.1.2 are included.

Prior to commencing installation, check the following items:

1. Ensure that a vacant SPC slot exists in the processor or data interface unit. The selection of this slot is dependent on cable length (25 ft max), power requirement (1.5A @ 5V), and latency (1.8 ms max last device on BR6).

2. Ensure that sufficient rack space is available to mount the TU60 Cassette Tape Transport. Installation of the transport is restricted only by the lengths of the interconnecting cables. Since the TA11 is usually an alternative for a high-speed reader, the space normally allocated for that device may be used, if available.

3. Ensure that the two BC08-S interconnecting cables are sufficiently long to reach between the controller and the transport.

4. Ensure that the vent fan inlet on the transport is not obstructed when the transport is pushed all the way into the rack.

5. Check the power supply fuses in the transport for correct rating. There are three fuses, as follows:

   +5V      5A
   +15V     3A
  −15V     3A

2.2 INSTALLATION PROCEDURE
Install the TA11 as follows:

1. Ensure that the system power is off.

2. Ensure that the correct device code address jumpers are installed on the control module. Factory shipments are made with a device code address of 777500 wired in. For multiple controller installations, refer to “PDP-11 Systems” tech tip for address selection.
3. Ensure that the correct vector address code jumpers are installed on the control module. Factory shipments are made with a vector address code of 260 wired in. For multiple controller installations, refer to "PDP-11 Systems" tech tip for vector address selection.

4. Ensure that the correct jumper plug is installed for the desired BR priority. Factory shipments are made with a BR6 jumper plug installed.

5. Connect the two BC08-S cable assemblies between the control module and the transport according to Figure 2-1.

6. Plug the control module into its designated location in the processor interface unit.

7. Install the TU60 Cassette Tape Transport according to the procedure contained in Chapter 2 of the *TU60 Cassette Tape Transport Maintenance Manual*, DEC-00-TU60-DA.

![Figure 2-1 TA11 Interconnection Diagram](image-url)
2.3 CHECK-OUT

Energize the system and load the LIBKIT-TA11 cassette. Refer to MAINDEC-11-DZTAF for tape loading instructions. The procedure involves the use of the BM792-YH Bootstrap Loader or a toggle-in loader to load the diagnostics from the cassette.

The LIBKIT-TA11 cassette contains five diagnostic programs, which test the following functions:

MAINDEC-11-DZTAA Basic Test – Part 1. This diagnostic test checks the basic controller functions. It also contains three toggle-in routines that can be used to troubleshoot a dead cassette if circumstances prevent loading of the diagnostics from cassette.

MAINDEC-11-DZTAB Basic Test – Part 2. This diagnostic test checks basic transport motion.

MAINDEC-11-DZTAC Manual Intervention Test. This diagnostic test checks WRITE LOCK, POWER FAIL, and other functions requiring operator intervention.

MAINDEC-11-DZTAD Motion Test. This diagnostic test checks data integrity during complex motion sequences.

MAINDEC-11-DZTAE Data Test. This diagnostic test checks the TU60 Cassette Tape Transport to data reliability specifications.

Successful completion of these diagnostic tests indicates satisfactory operation of the TA11. A duplicate of the Teletype printout made during the running of these five tests is contained in Appendix A of this manual.

2.4 INTERFACE

The TU60 Cassette Tape Transport is unique in that the transport does not require a separate controller. All the logic necessary for data formatting, error checking, and cassette housekeeping are contained on two logic modules within the transport chassis. The M7892 Control module (Figure 2-2) contains logic that converts the processor codes into commands and transmits them to the TU60. In addition, the M7892 Control module is capable of interpreting status flags received from the TU60, as well as providing temporary storage of input/output data.

There are several interface signals that must be present at the TU60 during an entire operation. These signals are SELECT ENABLE L, DRIVE B L, BACK BLOCK GAP L, BACK FILE GAP L, and R/W FILE GAP. The REWIND L, R/W CLR L, TRANSFER L, and WRITE MODE L signals, however, are transmitted and then stored in the TU60. All interface signals are at ground (low) for a logical 1 and +3V (high) for a logical 0. Figure 2-3 shows the interface signal paths between the TU60 and the control module. The signals are described in the following paragraphs.

2.4.1 Control Module Output Interface Signals

2.4.1.1 Select Enable L – This signal, at a logical 1, enables the TU60 input/output transmitters and receivers.

2.4.1.2 Drive B L – This signal selects one of the dual tape drives. A logical 1 selects drive B or a logical 0 selects drive A.

2.4.1.3 Start L – This signal, at a logical 1, is used in conjunction with a specific command to initiate command execution. If a command is to be performed, the drive must be in the ready state (READY L present) and the command present and stable one microsecond prior to START L. If this is the case, when START L is received, the TU60 electronics removes the READY L signal and initiates command execution. When READY L is removed, the interface then removes START L, and while the command is being executed, any additional START L signals are ignored by the drive.

2-3
2.4.1.4 **Rewind L** — This motion command signal, at a logical 1, is clocked by the START L signal to trigger the REWIND one-shot and thus cause a high-speed (100-150 ips) tape rewind on the selected drive, to the beginning of the tape.

2.4.1.5 **Back Block Gap L** — This motion command signal, at a logical 1, is clocked by the START L signal to cause reverse tape motion at read/write speed across a data block to the preceding pre gap.

2.4.1.6 **Back File Gap L** — This motion command signal, at a logical 1, is clocked by the START L signal to cause reverse tape motion at search speed across a data file, stopping at two-thirds of the preceding file gap.
2.4.1.7 **R/W File Gap L** – This signal, at a logical 1, is used in conjunction with the WRITE MODE L signal to initiate either forward tape motion or a WRITE FILE GAP operation. If WRITE MODE L is a logical 1 when this signal is clocked by the START L signal, 535 ms of tape is erased. If WRITE MODE L is a logical 0 when this signal is clocked, tape on the selected drive moves forward, stopping at the beginning of the next file gap.

2.4.1.8 **Write Mode L** – This signal selects either the read or write logic. For a WRITE or WRITE FILE GAP operation, this signal, at a logical 1, is clocked by the START L signal to set the WRITE flip-flop.

For a READ operation, this signal, at a logical 0, allows the START L signal to reset the WRITE flip-flop. Once the specific operation is initiated, the WRITE flip-flop remains either set or reset until the next operation is started.

2.4.1.9 **Transfer L** – During a WRITE operation, this signal, at a logical 1, is transmitted to the TU60 in response to a TRANSFER REQ L signal. If this is the case, TRANSFER L sets the TRANS REQ flip-flop and the 8-bit byte is loaded into the TU60 data buffer.

During a READ operation, this signal, at a logical 1, is transmitted to the TU60 in response to a TRANSFER REQ L signal. If this is the case, TRANSFER L sets the TRANS REQ flip-flop to indicate that the 8-bit byte has been loaded into the interface buffer.

2.4.1.10 **R/W CRC L** – During a WRITE operation, this signal, at a logical 1, causes the accumulated CRC character to be recorded on the tape. R/W CRC L is transmitted to the TU60 while the final data byte is being recorded. When this occurs, the next TRANSFER REQ L signal is inhibited and the CRC character is recorded after the final data bit is written.
During a READ operation, this signal, at a logical 1, tests the CRC register for an error. At the start of a read operation, the CRC ERR flip-flop is set and remains set while the data block is being read. After the first 8 CRC bits have been read, the interface transmits R/W CRC L. When the final TRANSFER REQ L signal is generated, the CRC register is checked for 0. If the register is not 0 (data read incorrectly), the CRC ERR flip-flop remains set and, when READY L is generated, a CRC ERROR L signal is also generated. If the data has been read correctly, the CRC ERR flip-flop resets and a CRC ERROR L signal is not generated.

2.4.1.11 Initialize L – This signal, at a logical 1, removes all flags (except EOT), generates READY L and, except for a REWIND operation, stops tape motion regardless of the tape position.

2.4.2 Control Module Input Interface Signals

2.4.2.1 Off Line L – This signal, at a logical 1, indicates that the appropriate tape cassette is not properly loaded on the selected drive or that the clear leader sensing lamp has failed.

2.4.2.2 Ready L – This signal, at a logical 1, indicates that the appropriate tape cassette has been properly loaded and tape motion is not occurring on the selected drive. In general, READY L is generated when all command functions have been completed and the drive is ready for the next operation or when a clear leader is encountered.

2.4.2.3 End File L – This signal, at a logical 1, indicates that a file gap has been detected or the ensuing tape is blank.

2.4.2.4 EOT/BOT L (End Tape) – This signal, at a logical 1, indicates that the drive has reached the end-of-tape or beginning-of-tape (clear leader photosensor uncovered). When this occurs, tape motion stops and the READY L and EOT/BOT L signals are generated. EOT/BOT L is suppressed during a REWIND operation or if the drive is not in the ready state.

2.4.2.5 Rewind L – This signal, at a logical 1, indicates that the selected drive is performing a rewind operation.

2.4.2.6 Write Protect L – This signal, at a logical 1, indicates that a write-protected cassette is loaded on the selected drive or that the drive is empty. If the cassette is write protected, the selected drive will not perform any WRITE operations.

2.4.2.7 Write Status L – This signal, at a logical 1, indicates that a WRITE or WRITE FILE GAP operation is being performed on the selected drive.

2.4.2.8 Transfer Request L – During a WRITE operation, this signal, at a logical 1, indicates that the drive is ready to receive an 8-bit byte from the interface buffer. The TRANSFER REQ L signal is generated one bit time before a byte is needed and this signal is removed when the interface responds with a TRANSFER L signal.

During a READ operation, this signal, at a logical 1, indicates that a byte from the drive is ready to be transferred to the interface buffer. The interface must then respond with a TRANSFER L signal within one bit time (≈ 220 μs) after the TRANSFER REQ L signal is generated or a time error occurs.

2.4.2.9 Time Error L – This signal, at a logical 1, indicates that the interface has not responded to a TRANSFER REQ L signal within the allotted time (≈ 220 μs).

2.4.2.10 CRC Error L – This signal, at a logical 1, indicates that a CRC error has occurred during a READ operation. At the start of the READ operation, the CRC ERR flip-flop is set. When the final CRC character is read, the CRC register is then checked for 0. If the register is not 0, the CRC ERR flip-flop remains set and, when READY L is generated, a CRC ERROR L signal is also generated.

2.4.2.11 PWR OK L – This signal, at a logical 1, indicates that the +5V power supply is operating normally.

2.4.2.12 Bits 1–8 (Bidirectional) – These eight lines transmit to and from the TU60 data buffer.
CHAPTER 3
OPERATION AND PROGRAMMING

This chapter describes the device registers in the TA11, register and vector address assignments, and programming examples.

3.1 DEVICE REGISTERS

All software control of the TA11 is performed by means of two device registers. These registers have been assigned bus addresses, and can be read or loaded, with certain exceptions, using any instruction referring to their addresses. These registers are the Tape Control and Status register (TACS) and the Tape Data Buffer register (TADB). They are described in the following paragraphs.

3.1.1 Control and Status Register

The TACS enables the program to control the TA11 functions. This register has an assigned bus address, and can be read or loaded, with the exceptions noted, using any instruction referring to its address. The TACS bit assignments are shown below:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>ERROR</td>
<td>Indicates an error condition determined by the current status indicators 14:09 and the current function 03:01. Paragraph 3.4 indicates which status bits under a particular function result in ERROR set. ERROR is valid only when READY is set. Read only.</td>
</tr>
<tr>
<td>Bit</td>
<td>Name</td>
<td>Meaning</td>
</tr>
<tr>
<td>-----</td>
<td>----------------</td>
<td>-------------------------------------------------------------------------</td>
</tr>
<tr>
<td>14</td>
<td>BLOCK CHECK</td>
<td>Indicates a CRC error for READ and SFB. During a READ function, BLOCK CHECK sets ERROR. Cleared when the next function is successfully initiated. Read only.</td>
</tr>
<tr>
<td>13</td>
<td>CLEAR LEADER</td>
<td>Indicates that the currently selected cassette is at end of tape (EOT) or beginning of tape (BOT). Sets ERROR for all functions exceptREWIND. Read only.</td>
</tr>
<tr>
<td>12</td>
<td>WRITE LOCK</td>
<td>Indicates that the currently selected cassette is write protected if and only if the current function bits are set for WRITE or WFG. Sets ERROR. This status indicator is derived from a microswitch and is not filtered from switch bounce. Read only.</td>
</tr>
<tr>
<td>11</td>
<td>FILE GAP</td>
<td>Indicates a file gap has been entered during a READ, SFB, SRF, or SFF function. Sets ERROR only on READ and SFB. Cleared when the next function is successfully initiated. Read only.</td>
</tr>
<tr>
<td>10</td>
<td>TIMING ERROR</td>
<td>Indicates that the program's response to TRANSFER REQUEST was not quick enough and signifies loss of data during READ or WRITE function. Sets ERROR. Cleared when the next function is successfully initiated. Read only.</td>
</tr>
<tr>
<td>09</td>
<td>OFF-LINE</td>
<td>Indicates that the currently selected cassette is not present or that there is no power in the cassette transport. Sets ERROR on all functions. This status indicator is derived from a microswitch and is not filtered from switch bounce. Read only.</td>
</tr>
<tr>
<td>08</td>
<td>UNIT SELECT</td>
<td>Specifies which transport is under program control. 0 for left (unit 0); 1 for right (unit 1). Read/Write. Cleared by initialize.</td>
</tr>
<tr>
<td>07</td>
<td>TRANSFER REQUEST</td>
<td>Indicates data available in TADB during READ, or request for data during WRITE. Cleared when TADB is addressed and by initialize. Held clear by ILBS. Inhibits READY from setting and must be serviced prior to READY. Read only.</td>
</tr>
<tr>
<td>06</td>
<td>INTERRUPT ENABLE</td>
<td>Enables READY or TRANSFER REQUEST to interrupt. Read/Write. Cleared by initialize.</td>
</tr>
<tr>
<td>05</td>
<td>READY</td>
<td>Indicates that the TA11/TU60 is ready to accept and execute a command. Cleared when function is initiated and set when function is completed as long as TRANSFER REQUEST is cleared. Set by initialize. Read only.</td>
</tr>
<tr>
<td>04</td>
<td>ILBS</td>
<td>Initiate Last Byte Sequence. Used to terminate WRITE function by causing the transport to write the CRC bytes, and to terminate READ function by causing the transport to read and check the next two bytes on tape as CRC characters. For an n byte block, ILBS is set in response to the n+1 TRANSFER REQUEST. Holds TRANSFER REQUEST clear. Cleared by initialize. Read/Write.</td>
</tr>
</tbody>
</table>
### 3.1.2 Tape Data Buffer Register (TADB)

The TADB register serves a dual function and actually comprises two separate registers in the control module. One register is loaded with data from the TU60 during the READ function and this data can be retrieved by reading TADB. The other register is loaded from the Unibus and presented to the TU60 during the WRITE function. Because of the dual nature of the TADB, deposited data cannot be examined by performing a read immediately after a write.

#### 3.2 REGISTER AND VECTOR ADDRESS ASSIGNMENTS

Up to eight TA11s can be used in a system. The address assignments for the first system are 777500 and 777502 for the TACS and TADB, respectively, and a vector address of 260. For multiple controller installations, a "floating" address scheme is used. The tech tip "PDP-11 Systems" contains the latest information regarding address selection for such installations.

Register and vector addresses are hardwired by means of jumpers on the control module.

#### 3.3 FUNCTION DESCRIPTION

A function is initiated by loading bits 03:01 in the TACS and setting the GO bit. The function will be executed on the drive specified by the UNIT SELECT bit. Only one drive at a time can be under program control. From the point in time when the GO bit is set until the READY indicator becomes true again, UNIT SELECT, GO, and the three function bits should not be altered.
There is one exception to the above rule: a REWIND function can be initiated on one drive and then be deselected, while operations are performed on the other drive. When the original drive is reselected, READY can be examined to determine if the previously initiated REWIND is complete; however, there is no guarantee that an interrupt will occur when the original drive is reselected unless INTERRUPT ENABLE is cleared prior to reselecting and set after reselecting.

Normal and abnormal operating sequences for the TA11 functions are described in the following paragraphs.

3.3.1 Write File Gap (WFG)

WFG writes a length of blank tape that is used to separate files. These gaps are detected by some of the other functions and are used by the program to position the tape.

Normally, 535 ms of blank tape is written; however, if WFG is issued when the tape is at BOT, then 1.4 seconds of blank tape is written to create the load point gap.

A normal WFG sequence is as follows:

1. Program issues WFG and GO.
2. Controller removes READY and initiates tape motion.
3. After writing the required blank tape, READY is set.

Abnormal WFG sequences are:

a. WFG on a write-protected cassette
   1. Program issues WFG and GO.
   2. Controller removes READY.
   3. Controller senses write-locked condition and sets READY with ERROR and WRITE LOCK. Total elapsed time is about 2 μs.

b. WFG at EOT.
   1. Program issues WFG and GO.
   2. Controller removes READY and initiates tape motion.
   3. After about 30 ms, READY sets with ERROR and CLEAR LEADER.

c. WFG enters EOT.
   1. Program issues WFG and GO.
   2. Controller removes READY and initiates tape motion.
   3. When tape enters EOT, READY sets with ERROR and CLEAR LEADER.

3.3.2 Write

The WRITE function is used to record data as a block of bytes on tape. The number of bytes per block is variable and is under program control.
A normal WRITE sequence is as follows:

1. Program issues WRITE and GO.
2. Controller removes READY, initiates tape motion, and sets TRANSFER REQUEST.
3. Program responds to TRANSFER REQUEST by loading TADB with data. Controller removes TRANSFER REQUEST.
4. At the appropriate time, the data is transferred to the cassette and the controller sets TRANSFER REQUEST again.
5. Steps 3 and 4 are repeated n times for an n-byte block.
6. After all bytes have been transferred, the program sets ILBS instead of loading TADB with more data, i.e., in response to the n+1 TRANSFER REQUEST, the program sets ILBS.
7. In response to ILBS, the controller clears TRANSFER REQUEST and the writing of the CRC bytes and block gap is initiated. When this sequence is complete and the tape is stopped, the controller sets READY.

Abnormal WRITE sequences are:

a. WRITE from BOT
   1. Program issues WRITE and GO.
   2. Controller senses CLEAR LEADER and issues a WFG command to the cassette.
   3. When the Load Point Gap has been written, the normal WRITE sequence is started. Note: Steps 2 and 3 are invisible to the program except for overall execution time.

b. WRITE attempted on a write-protected cassette
   1. Program issues WRITE and GO.
   2. Controller removes READY.
   3. Controller senses write-locked condition and sets READY with ERROR and WRITE LOCK. Total elapsed time is about 2 μs.

c. WRITE from EOT
   1. Program issues WRITE and GO.
   2. Controller senses CLEAR LEADER and issues a WFG command to the cassette.
   3. When the WFG is complete, the controller issues a WRITE command to the cassette and sets TRANSFER REQUEST.
   4. When the program services TRANSFER REQUEST, READY immediately sets, with ERROR and CLEAR LEADER. Total elapsed time is approximately 60 ms.
d. WRITE enters EOT

1. Assume a WRITE operation in progress.

2. Tape enters EOT.

3. When any pending TRANSFER REQUEST is serviced, READY sets with ERROR and CLEAR LEADER.

e. WRITE with TIMING ERROR

1. Assume a WRITE operation in progress.

2. Program does not respond within 1.8 ms to TRANSFER REQUEST.

3. CRC bytes and block gap are written.

4. When the program eventually services TRANSFER REQUEST, READY sets with ERROR and TIMING ERROR.

3.3.3 Read

The READ function is used to recover a block of data that was previously written on tape. To assure proper cyclic redundancy checking, the program must know the number of bytes written in the block. BLOCK CHECK will normally result if the program issues ILBS at the wrong time.

The normal READ sequence is as follows:

1. Program issues READ and GO.

2. Controller removes READY and initiates tape motion.

3. When a byte of data is available, the controller sets TRANSFER REQUEST. Program reads TADB and the controller clears TRANSFER REQUEST.

4. Step 3 is executed n times for an n-byte block.

5. After the nth byte is read, the program waits for the n+1 TRANSFER REQUEST and then sets ILBS.

6. Controller clears TRANSFER REQUEST and initiates block check sequence. When complete, READY is set. If a block check error is detected, ERROR and BLOCK CHECK are set. READY sets before the tape actually stops in the block gap.

Abnormal READ sequences are as follows:

a. READ enters EOT

1. Assume a READ operation in progress.

2. Tape enters EOT.

3. When any pending TRANSFER REQUEST is serviced, READY sets with ERROR and CLEAR LEADER.
b. READ issued on blank tape or at the beginning of a file gap (but not BOT).
   1. Program issues READ and GO.
   2. Controller removes READY and initiates tape motion.
   3. Since no data is encountered within 450 ms, READY sets with ERROR and FILE GAP.

c. READ from BOT
   1. Program issues READ and GO.
   2. Controller removes READY and initiates tape motion.
   3. Tape is moved forward off BOT and over the Load Point Gap. Reading begins when data is encountered. Note: the 450 ms timer mentioned in b step 3 is disabled.

d. READ with TIMING ERROR
   1. Assume a READ operation in progress.
   2. Program does not respond within 1.8 ms to TRANSFER REQUEST.
   3. When the program eventually services TRANSFER REQUEST and the tape has stopped in the block gap, READY sets with ERROR and TIMING ERROR.

3.3.4 Space Reverse File (SRF)
SRF is used to move the tape in reverse into the preceding file gap. Previously written data must be encountered before the transport begins to look for the blank tape of the file gap.

The normal SRF sequences is as follows:
   1. Program issues SRF and GO.
   2. Controller removes READY and initiates tape motion.
   3. When positioned in the previous file gap, READY sets with FILE GAP.

If an SRF enters BOT or SRF is attempted from BOT, the following abnormal sequence occurs:
   1. Program issues SRF and GO.
   2. Controller removes READY and initiates tape motion.
   3. When BOT is detected, READY sets with ERROR and CLEAR LEADER.

3.3.5 Space Reverse Block (SRB)
SRB is used to move the tape in reverse into the preceding block gap. Previously written data must be encountered before the transport begins to look for the blank tape of the block gap.
The normal SRB sequence is as follows:

1. Program issues SRB and GO.
2. Controller removes READY and initiates tape motion.
3. When positioned in the previous block gap, READY sets.

If an SRB enters BOT or SRB is attempted from BOT, the following abnormal sequence occurs:

1. Program issues SRB and GO.
2. Controller removes READY and initiates tape motion.
3. When BOT is detected, READY sets with ERROR and CLEAR LEADER.

3.3.6 Space Forward File (SFF)

SFF is used to advance the tape to the next file gap. In contrast to SRF, SFF does not look for data prior to looking for the blank tape of the file gap (except from BOT); therefore, SFF and SRF are not symmetrical functions. In addition, this implies that if SFF is initiated at the beginning of a file gap, a FILE GAP indication will result in the same gap. The following example clarifies this point.

Assume that three files exist on a cassette separated by two file gaps. Also assume that the tape finishes reading to the end of the last record in the first file. Now the tape is positioned almost at the beginning of the first file gap. Now, if a SFF (or SFB) is initiated, FILE GAP condition will be indicated even before entering into the second file. On the other hand, if the tape came into the first file gap due to a SFF or SRF and a SFF is initiated, tape will be positioned in the second file gap, i.e., second file of data is skipped.

The normal SFF sequence is as follows:

1. Program issues SFF and GO.
2. Controller removes READY and initiates tape motion.
3. When the next file gap is detected, READY sets with FILE GAP.

Abnormal SFF sequences are as follows:

a. SFF from BOT
   1. Program issues SFF and GO.
   2. Controller removes READY and initiates tape motion.
   3. Tape moves off EOT, through the load point gap, and forward until data is encountered.
   4. When the first file gap is detected (after data), READY sets FILE GAP.
b. SFF from EOT; SFF enters EOT
   1. Program issues SFF and GO.
   2. Controller removes READY and initiates tape motion.
   3. When EOT is detected, READY sets with ERROR and CLEAR LEADER.

3.3.7 Space Forward Block (SFB)

SFB is used to advance the tape to the next block gap. In contrast to SRB, SFB does not look for data prior to looking for the block gap (except from BOT); therefore, if SFB is initiated at the beginning of a file gap, a FILE GAP indication will result in that same gap. SFB is actually a READ operation with no TRANSFER REQUESTS.

The normal SFB sequence is as follows:

   1. Program issues SFB and GO.
   2. Controller removes READY and initiates tape motion.
   3. When the next block gap is detected, READY sets with BLOCK CHECK.

Abnormal SFB sequences are as follows:

a. SFB from BOT
   1. Program issues SFB and GO.
   2. Controller removes READY and initiates tape motion.
   3. Tape moves off EOT, through the load point gap, and forward until data is encountered.
   4. When the first block gap is detected, READY sets with BLOCK CHECK.

b. SFB from EOT; SFB enters EOT
   1. Program issues SFB and GO.
   2. Controller removes READY and initiates tape motion.
   3. When EOT is detected, READY sets with ERROR and CLEAR LEADER.

c. SFB enters FILE GAP
   1. Program issues SFB and GO.
   2. Controller removes READY and initiates tape motion.
   3. When the file gap is detected, READY sets with ERROR and FILE GAP.
3.3.8 Rewind
REb\IND is used to position the tape at BOT.

The normal REWIND sequence is as follows:

1. Program issues REWIND and GO.
2. Controller removes READY and initiates tape motion.
3. When REWIND is complete, READY sets with CLEAR LEADER.

3.3.9 Off-Line
An OFF-LINE condition exists when no cassette is in a drive, or when power is off in the TU60. If any function is attempted on an off-line cassette, the following sequence occurs:

1. Program issues FUNCTION and GO.
2. Controller removes READY.
3. Controller senses off-line condition and sets READY with ERROR and OFF-LINE. Total elapsed time is about 2 μs.

3.4 STATUS INDICATIONS
Provisions are made in the TACS to indicate what type of error occurs if an abnormal sequence is attempted. Listed below are status conditions that could occur for the different sequences. Note that unless ERROR = 1, no error condition exists even though one of the status bits may be set.

### NORMAL VS. ERROR STATUS CONDITIONS

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>POSSIBLE NORMAL INDICATORS, ERROR = 0</th>
<th>POSSIBLE ERROR INDICATORS, ERROR = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 — WRITE FILE GAP</td>
<td>NONE</td>
<td>WRITE LOCK, CLEAR LEADER, OFF-LINE</td>
</tr>
<tr>
<td>1 — WRITE</td>
<td>NONE</td>
<td>WRITE LOCK, CLEAR LEADER, TIMING ERROR, OFF-LINE</td>
</tr>
<tr>
<td>2 — READ</td>
<td>NONE</td>
<td>CLEAR LEADER, FILE GAP, TIMING ERROR, BLOCK CHECK, OFF-LINE</td>
</tr>
<tr>
<td>3 — SPACE REV FILE</td>
<td>FILE GAP</td>
<td>CLEAR LEADER, OFF-LINE</td>
</tr>
</tbody>
</table>

(continued on next page)
### NORMAL VS. ERROR STATUS CONDITIONS (Cont)

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>POSSIBLE NORMAL INDICATORS, ERROR = 0</th>
<th>POSSIBLE ERROR INDICATORS, ERROR = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 – SPACE REV BLOCK</td>
<td>NONE</td>
<td>CLEAR LEADER</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF-LINE</td>
</tr>
<tr>
<td>5 – SPACE FWD FILE</td>
<td>FILE GAP</td>
<td>CLEAR LEADER</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF-LINE</td>
</tr>
<tr>
<td>6 – SPACE FWD BLOCK</td>
<td>BLOCK CHECK</td>
<td>FILE GAP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CLEAR LEADER</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF-LINE</td>
</tr>
<tr>
<td>7 – REWIND</td>
<td>CLEAR LEADER</td>
<td>OFF-LINE</td>
</tr>
</tbody>
</table>

### 3.5 RESTRICTIONS

To ensure reliable operation, the following restrictions must be followed: If a WRITE or WFG function is initiated at some point on the tape, then all previously recorded data from that point to the end of tape is lost. This implies that a block or file is not replaceable unless it is the last block or file on the tape.

A WRITE or WFG function must be preceded by the completion of one of the following functions: WRITE, WFG, REWIND, READ without a FILE GAP indication, or SFB without a FILE GAP indication. This ensures correct file and block gap lengths.

An example of this restriction is covered in the procedure to add a new file:

1. Repeat SFF until beyond the last file.
2. SRB. Back up over last block of last file.
3. SFB. Position tape at end of last block of last file.
4. WFG.
5. Repeat WRITE for each block.
6. WFG. Close file.

This rule can be violated in the following situation. Since there is no hardware read after write, it is necessary for increased reliability to read back what was written out. This is accomplished on a block basis by issuing a SRB followed by a READ with a software data comparison. If the check is good then the next block can be written or the file closed with WFG. If there is an error, then a SRB followed by a WRITE can be issued, but this rewrite sequence can be executed only three times. This ensures minimum gap distortion.

If this limit must be exceeded, the following procedure, which obeys the second rule, should be used. Three cases arise: Case 1 the block to be rewritten is not the first block in the file; after the read check fails, perform two SRBs, one SFB, and then rewrite the block. Case 2 the block to be rewritten is the first block in a file that is not the first file; perform two SRBs, one SFB, (now at end of previous file), WFG, and then rewrite the block. Case 3 the block to be rewritten is the first block in first file; perform a REWIND, WRITE FILE GAP, and then rewrite, or REWIND then rewrite.

From clear leader at the beginning of tape, no software detectable file gap can be written, since READ, SFB, and SFF from clear leader ignore all blank tape until data is encountered. Thus, the load point gap (between BOT and the
the first block of data) is essentially invisible to programmed operation except for overall timing. However, if the
tape is initially loaded on the load point gap, then multiple file gaps will be found under the READ, SFB, and SFF
functions.

NOTE
The WRITE function from BOT writes the load point gap and
then begins to write data; therefore, WFG from BOT is optional.

Each cassette has identical clear leader at each end. For physical reasons, forward motion at the end and reverse motion
at the beginning should be prevented. To accomplish this, the TU60 control logic assumes that when a cassette
is loaded initially and a clear leader is seen, it is EOT. The functions WFG, WRITE, READ, SFF, and SFB operate
as if the tape is actually at EOT, and forward tape motion is not allowed. However, the SRF and SRB functions
cause the TU60 to hang up, and READY will never set until the system is initialized. Only the REWIND function
will be accepted and properly executed and, when complete, any function can then be issued.

These restrictions do not apply if the cassette is initially loaded and the tape is on oxide.

Unless the TA11 OFF-LINE status bit is continually checked by the program, a cassette can be removed from the
TU60 transport and replaced with another randomly positioned cassette without giving any indication to the program.

A cassette cannot be removed and then reinserted in the transport without repositioning of the tape. For example,
if a WRITE operation detects a write-locked cassette and reports the error, the cassette can be removed, the write-
lock tabs flipped, and then reinserted. The program can not assume the tape is now at the same point. Rather, it
must properly reposition the tape prior to writing. A time saving method is to check WRITE LOCK prior to position-
ing by selecting the desired unit and loading the function bits with a WFG or WRITE (but not the GO bit).

The cassette REWIND button can be activated whenever the cassette is not already in motion. No direct indication
of this repositioning is given to the program; however, after a manual rewind is complete, the tape is at BOT and
CLEAR LEADER can be checked prior to the next operation.

TRANSFER REQUEST in the TA11 Status register is cleared by ILBS, referencing the TADB, and by initialize. It
is not cleared by issuing a new function. Thus, if TRANSFER REQUEST has been left set by some previously
aborted READ or WRITE function and a new function is initiated, then TRANSFER REQUEST hides the READY
bit until TRANSFER REQUEST is serviced. This problem arises because the TA11/TU60 has been left in some
random state (e.g., a READ or WRITE function was aborted) and a new function is to be initiated. It is imperative
not to issue the new command until the TA11/TU60 is ready to accept a new command, as indicated by the READY
bit. The TA11 is not ready until all TRANSFER REQUESTs are serviced; the TU60 is not ready until tape motion
has stopped.

This hang up can be avoided by never aborting a READ or WRITE without ILBS, or by issuing commands as follows:

```
BIS # ILBS, TACS ;Terminate function that might
:be in progress.
WAIT:
BIT # READY, TACS ;Test READY
BEQ WAIT ;Wait
MOV B # COMMAND, TACS ;Issue command
```
3.6 FLAG CHECKING SEQUENCE

The relationship between TRANSFER REQUEST, READY, and ERROR dictates the sequence in which these flags should be checked. First, the bits 14:09 of TACS are transport status bits that may or may not set ERROR as a function of the command which is being issued. For example, CLEAR LEADER after rewind is normal; CLEAR LEADER after READ results in ERROR set. Next, ERROR is not valid until READY is set. Finally, READY does not set until TRANSFER REQUEST is clear.

In addition, it should be noted that OFF-LINE, WRITE LOCK, and CLEAR LEADER status indicators are dependent on the cassette selected. (In addition, WRITE LOCK is dependent on a WRITE or WFG in the function bits.) When a cassette unit is selected by setting or clearing the UNIT SELECT bit, these status indicators immediately reflect the status of the newly selected unit. In contrast, status indicators FILE GAP, BLOCK CHECK, and TIMING ERROR are cleared to 0 when a function is successfully initiated and updated when the function completes, and simply selecting the other cassette unit will not clear out these status bits. In addition, a function cannot be “successfully initiated” on a cassette if that cassette indicates an OFF-LINE or WRITE LOCK status. Thus, FILE GAP, BLOCK CHECK, or TIMING ERROR can be “left over” from a previous operation. For example, a function on unit 0 results in a FILE GAP flag. A WFG is then attempted on unit 1, which happens to be write protected. The status will now indicate both WRITE LOCK and FILE GAP.

These relationships between the status indicators, ERROR, READY, and TRANSFER REQUEST dictate the flag checking sequence as shown in Figure 3-1.

![Flag Checking Sequence Diagram](image-url)

Figure 3-1 TA11 Flag Checking Sequence
The TA11 will request an interrupt when the following condition goes from false to true:

\[
(\text{TRANSFER REQUEST} + \text{READY}) \ast \text{INTERRUPT ENABLE}
\]

where

\[
+ = \text{logical OR} \\
\ast = \text{logical AND}
\]

The interrupt request will remain until the interrupt occurs until the condition goes false. Thus, assuming INTERRUPT ENABLE is set, the 0 to 1 transitions on READY or TRANSFER REQUEST request interrupts; in addition, setting INTERRUPT ENABLE with READY or TRANSFER REQUEST previously set also requests an interrupt. The request for an interrupt becomes an actual interrupt when the processor allows it, e.g., the proper priority level.

3.7 PROGRAMMING EXAMPLE

The following programming example is a subroutine call that is used to read a block of data. It is assumed that the tape has been properly positioned and the UNIT SELECT bit has been previously set/clear for unit 1 or 0. The number of bytes to be read and the buffer address are arguments stored following the JSR %5, READ instruction.

The subroutine first terminates any previous READ or WRITE function that might have been aborted and then waits for READY. When the control is ready, the READ function is issued and the block of data is read into the specified buffer. If no errors have been detected, program control is returned to the normal return address. OFF-LINE, CLEAR LEADER, and FILE GAP errors cause program control to return immediately to the error return address; however, a BLOCK CHECK or TIMING ERROR are considered “soft” errors and a SRB function is issued and the block is re-read. At most, three rereads are attempted.

**NOTE**

If the byte count specified by the program does not equal the number of bytes written in the block, then a BLOCK CHECK error will always result.
177500 TACS= 177500
177502 TAUB= 177502
177504 TLMS= 20
000046 READY= 40
000140 TMLST= 200
301900 ODLIN= 1000
500004 FCAP= 4000
511000 WRLCK= 10000
527000 CLMDR= 20000

;CASSette READ ROUTINE, ASSUMES UNIT SELECT BIT HAS BEEN PREVIOUSLY ESTABLISHED,
;ICalling Sequence
;J CALL JSR 15,READ
;J BYTE COUNT
;J ADDRESS
;J ERROR RETURN
;J NORMAL RETURN
;J CONTROL RETURNS HERE ON ERROR
;J CONTROL RETURNS HERE ON SUCCESSFUL READ COMPLETION
081000 012767 000093 038160 READ1 MOV #3,RETTRY
081006 012767 000193 HEAD01 MOV (X5),COUNT
081012 012767 000146 MOV (X5),POINT
081018 055767 000220 176494 DIS #1LBS,TACS
081024 055767 000200 176466 HEAD1 BIT #READY,TACS
081032 051774 HEQ READ1 IF #READY= 0
081034 112767 000055 176436 MOVB #5,TACS IWAIT IF READY = 0
081042 112767 000248 176430 READ21 BIT #READY=RETTRY,TACS ICHECK TAIL FLAGS
081050 011774 HEQ READ2 HEAD02
081056 103026 HPL ERROR IIF READY = 1, THEN MUST BE SOME ERROR
081058 035567 000102 DEC COUNT JERROR = 1, CHECK BYTE COUNT
081066 135066 HMI READ3 IIF LAST BYTE WAS READ, GO SET ILBS
081068 135066 MOV TDAB,POINTER IMEM DATA FROM TDAB INTO MEMORY
081070 005267 000070 INC POINT IADVANCE POINTER
081074 000626 HRI READ6 HR READ
081076 035767 000220 176347 READ11 BIT #1LBS,TACS
081084 035767 000200 176346 READ2 BIT #READY,TACS
081092 010453 HEQ READ4 INCREMENT TAIL FLAGS
081112 301774 READ5 IF #READY = 0
081114 057567 176360 TST TACS IWAIT IF READY = 0
081120 010463 BMI ERROR ICHECK TAIL FOR ERROR
081122 067795 000002 ADD #2,55 IIF READY IS 0, THEN IMMEDIATELY DO ERROR RETURN
081126 037295 READ5 RFS NS
081130 037295 02506 176342 ERRORM1 BIT ODLIN=CLMDR=FCAP,TACS IIF THE ERROR IS OFF-LINE, CLMDR, OR
081134 037295 016773 HME READS IF ERROR, THEN IMMEDIATELY DO ERROR RETURN
081140 005367 000022 DEC RETRY IIF BLOCK CHECK ERROR OR TIMING ERROR, TRY AGAIN
081144 005776 BMI READS ITRY AT MOST THREE TIMES
081146 162795 00204 SUB #4,55 IBACK UP TO BYTE COUNT AND POINTER
081152 112767 000111 176320 MOVB #11,TACS ISSUE SPACE REVERSE BLOCK FUNCTION
081160 000712 HR READ6
081162 000000 COUNTER R COUNT
081164 000000 POINTER R POINT
081166 000000 RETTRY R REPLY

Operating Program Example

3-15
CHAPTER 4
THEORY OF OPERATION

This chapter describes the theory of operation of the TA11 Cassette Interface. Two levels of discussion are presented: a block diagram discussion which presents a general functional description, and a detailed functional description which presents a discussion of the individual functional area. In these discussions, it is assumed that the reader is familiar with Unibus operations, as described in the PDP-11 Peripherals and Interfacing Handbook.

4.1 BLOCK DIAGRAM DESCRIPTION
A block diagram of the TA11 is shown in Figure 4-1. The operation of the various elements is discussed in the following paragraphs. Figure 4-2 is a flowchart of the TA11 system.

4.1.1 Address Decoder
The address decoder determines whether its associated TA11 is being addressed and which register (control or data) within the TA11 is selected. The selection of the discrete address is made by means of jumpers on the circuit board.

4.1.2 Data Path Selection
The data path selection section is a network of combinational logic that receives the output signals from the address decoder and the C1 and C0 signals from the Unibus. From these signals, it establishes the source or destination of data flow, from either the TA11 Control and Status register (TACS) or the Tape Data Buffer register (TADB) to or from the Unibus. The state of the C1 bit determines whether data is to be written into or read from these registers.

4.1.3 Tape Control and Status Register (TACS)
The TACS is a buffer register that provides temporary storage of the selected function to be performed by the TA11. The contents of the TACS are discussed in Paragraph 3.1.1.

4.1.4 Tape Data Buffer Register (TADB)
The TADB actually comprises two separate registers (read and write) that provide temporary storage of data between the TU60 and the Unibus. It receives data at the appropriate time from the Unibus or the TU60, as determined by the data path selection logic and the sequence and flag control logic.

4.1.5 Function Decoder
The function decoder is a 32-word by 8-bit ROM that receives the function select bits stored in the TACS and decodes them to generate discrete function signals, which are sent to the TU60.

4.1.6 Status ROM
The status ROM is a 256-word by 4-bit ROM that receives status information from the TU60 and the function select bits from the TACS. Its outputs provide error sensing indications that are used by the other TA11 logic networks; the outputs also provide status indications that are gated into the TACS for use by the main program.
4.1.7 Sequence and Flag Control Logic

The sequence and flag control is a combinational logic network consisting of one-shots and logic elements. It receives input signals from all of the previously described elements of the TA11 and provides the required timing and sequencing signals to the rest of the TA11.

4.1.8 Interrupt Control Logic

The interrupt control is a combinational logic network that receives and generates the Unibus control signals required for Unibus transactions. When a data transfer is to be initiated, this network generates the bus request signal, receives the bus grant, then generates SACK, BUS BUSY, and INTERRUPT.

4.1.9 Vector Address Generator

The vector address generator consists of a number of logic gates, whose outputs can be hardwired via jumpers to the data lines. When an INTERRUPT signal is generated by the interrupt control logic, a vector address, which is determined by the placement of the jumpers, appears on the data lines.

4.2 FUNCTIONAL DESCRIPTION

This section contains a detailed description of each of the major functional areas comprising the TA11. Each of these areas is discussed in the following paragraphs. Drawing references are made to the sheet numbers in the TA11 Engineering Drawings Manual.
Figure 4-2 TA11 System Flowchart
4.2.1 Address Decoder

The address decoder shown on sheet TA-2 is a combinational logic network that decodes two discrete addresses assigned to the TA11. Address bits A(17:13) must always be 1s to satisfy the decoder. The state of address bits A(12:03) is determined by the placement of jumpers A12 through A3 on the board. For each of these bits, one 8242 Exclusive-NOR gate is used. Insertion of a jumper for a particular bit position stores a 0 on one leg of the Exclusive-NOR gate, so that a 1 appearing on the other leg causes the output to go low. This is a mismatch condition, and it is met when the associated address bit is a 0. When both legs match, (1s on one and 0s on both) the output is high. The output of these 12 gates are ANDed and applied to one leg of a 7400 NAND gate. The other leg of this gate receives the ANDed signal of A17 and MSYN. The state of address bits A02 and A01 is used to determine whether the TADB or the TACS is being addressed. Bit A02 is inverted and applied to one leg of two 7427 3-input NAND gates. A second leg of each of these gates receives the ANDed signal of address bits A(17:03) and MSYN. Bit A01 is inverted and applied directly to the third leg of one of these gates, and is inverted again and applied to the third input leg of the other gate. Thus, the state of A01 determines which of the mutually exclusive signals, TA-2 SELECT 00 H or TA-2 SELECT 02 H, is generated. These signals, in turn, enable data paths to the TACS in the case of SELECT 00 H, or to the TADB in the case of SELECT 02 H. Because of this configuration in the decoding logic, it is necessary that the address of the TADB be always the next word address after that of the TACS.

Note that it was not necessary to decode bit A00 to generate SELECT 00 or SELECT 02 signals. PDP-11 system architecture dictates that all word addresses be even numbers, but byte addresses may be even or odd. Therefore, A00 will be a 1 only if an odd byte address is being selected. If a byte address is specified, then C0 will be a 1. If C0 is a 1 and A00 is a 0, then the low order byte is specified. The two signals A00 and C0 are logically combined in two 7450 gates to provide two signals, TA-2 OUT HIGH H and TA-2 OUT LOW H, depending on the state of A00 when C0 is a 1. These signals select the appropriate byte in the data path selection logic.

4.2.2 Data Path Selection

The data path selection logic, shown on sheets TA-3 and TA-4, is a network of combinational logic that receives the output signals from the address decoder. From these signals it establishes the data paths within, into, and out of the TA11. The signal TA-2 IN H is derived from the BUS C1 signal, and is high whenever BUS C1 is high, indicating a data in condition to the bus master, and thus a data out to the TA11. TA-2 IN H is ANDed with TA-2 SELECT 00 H or TA-2 SELECT 02 H from the address decoder, and generates an enabling signal to the TACS in the case of TA-2 SELECT 00 H or to the TADB in the case of TA-2 SELECT 02 H. The TADB or TACS data path is enabled to the Unibus and the contents of the selected register appears on the data lines. If data is to be written into the TADB or TACS, then TA-2 IN H will be low.

The TADB is an 8-bit register; therefore, the data transfers to and from the bus master will always be the lower byte. If the state of C1 and C0 indicates a DATO or DATOB transfer, the signals TA-2 OUT LOW H, TA-2 OUT HIGH H, or both will be generated. These signals are ANDed with TA-2 SELECT 00 H or TA-2 SELECT 02 H to generate clock signals to the TACS or TADB. In the case of the TACS, TA-3 BUS → TACS H is generated. This signal is used in the sequence and control logic to initiate the timing sequences. It also clocks the Unibus data to the TACS. If the upper byte of the TACS is addressed during a DATO or DATOB, signal TA-2 OUT HIGH H is generated, which is ANDed with TA-2 SELECT 00 H to clock the upper byte of the TACS.

4.2.3 Tape Control and Status Register (TACS)

The TACS is a buffer register that provides temporary storage of commands and status information between the TA11 and the processor. It is a 16-bit register, but not all 16 bits are read/write; some are read only and one is write only. A summary of these bits is given below:

| Read/Write | 8, 6, 4, 3, 2, 1 |
| Read Only  | 15, 14, 13, 12, 11, 10, 9, 7, 5 |
| Write Only | 0 |

4-4
The treatment of the signals for each of these bit positions varies depending on its type. The read/write bits are both command and status bits; commands when they are written, and status when they are read. The read only bits are status indications and the write only bit, the GO signal, is a command. All of the read/write bits are stored in flip-flops in the TA-11. Bit 8, the UNIT SELECT bit, has its own storage flip-flop, since it is the only read/write bit in the upper byte, and the other read/write bits are stored in a 74174 latch. The read only bits or status bits do not have storage flip-flops, but are signals which originate elsewhere in the TA11, either from the TU60 or the M7892, and then are gated onto the Unibus data lines when the TACS is read. The GO bit, which is the write only bit, is ANDed directly with TA-3 BUS → TACS H to initiate the timing cycle in the sequence and flag control section.

4.2.4 Tape Data Buffer Register (TADB)

The TADB, shown on sheets TA-3 and TA-4, actually comprises two separate registers, a read and a write register. It provides temporary storage of data between the TU60 and the Unibus. Two 74175 quadruple latches comprise each section of the TADB, making a total of four chips for the entire TADB. The operation of each section is essentially similar.

During the read operation, the data is stored in the read buffer. The data is transferred via the Unibus to the bus master at the appropriate time, under program control.

The write buffer, shown on sheet TA-4, performs a data storage function when data is being written onto the tape. The byte of data to be written is clocked in when TA-3 CLK WRITE BUFF H is active. The data is stored until the next clock pulse or TA-2 BINIT L occurs. The data outputs of the write buffer are NANDed with TA-5 DISAB WRITE BUFF H to control the flow of data to the TU60.

4.2.5 Function Decoder

The function decoder, shown on sheet TA-5 is a 32-word by 8-bit ROM that receives the function select bits stored in the TACS and decodes them to generate the function signals to the TU60. One additional logic signal, REPEAT H, is decoded by the function decoder to provide proper tape format. The fifth input is unused; thus, the decoder in actuality becomes a 16-word device. The inputs A1 through A5 specify a word address in the ROM; the 8-bit contents of the addressed location appear on the outputs M1 through M7. Thus, for every possible combination of input conditions, the state of eight output conditions is specified. The ROM pattern specification is given in Table 4-1.

4.2.6 Status ROM

The status ROM, shown on sheet TA-4, is a 256-word by 4-bit ROM that receives status information from the TU60, and the function select bits from the TACS. One of its functions is to determine whether or not an error condition exists. Its outputs (M3 through M0) enable either the selected action or error action. Its operation is similar to that of the function decoder ROM, but in this case, there are 256 possible input conditions for which the state of four output signals is defined. The ROM pattern specification for the status ROM is given in Table 4-2.

4.2.7 Sequence and Flag Control Logic

The sequence and flag control network provides sequencing and control signals to the controller, the processor, and the transport. When a GO command is written into the TACS, signals TA-3 BD00 H and TA-3 BUS → TACS H are asserted, causing one-shot A to generate a 1 μs pulse. The leading edge of the pulse clears the READY flip-flop and the trailing edge triggers one-shot B, which generates a 1 μs pulse. The leading edge of one-shot B enables TA-4 ENAB REPEAT H to set the REPEAT flip-flop; however, for the purpose of this discussion, it is assumed that TA-4 ENAB REPEAT H is not asserted at this time, and the REPEAT flip-flop remains reset. The trailing edge of one-shot B triggers one-shot C, which generates a 2 μs pulse. The leading edge of this pulse sets the READY flip-flop if TA-4 ENAB GO H is not asserted. With READY set, TA-5 INT H is also asserted. The trailing edge of one-shot C clocks the START flip-flop, which generates TU60 START L which, in turn, causes the TU60 to initiate tape motion. START is also NANDed with WRITE H from the function decode ROM, and if a WRITE function had been selected,
TRANSFER REQUEST is also set. This causes the bus master to load the TADB with data. When the TADB is addressed, TA-2 SELECT 02 is asserted, clearing the TR flip-flop. When the TU60 is ready to write the data onto the cassette, it asserts TU60 TRANSFER REQ L, which is delayed 2 µs and clocks the TRANSFER flip-flop; this flip-flop sets when TR is reset, generating TU60 TRANSFER L. At the end of the transfer, the TR flip-flop sets, which requests the bus master to load another byte into the TADB, and the controller continues to transfer data onto the cassette. After all bytes have been transferred, the next transfer request from the controller will request the program to set ILBS. This causes TR to clear, and the TU60 automatically writes the CRC bytes and block gap, stops the tape, and resets TU60 READY.

The function performed by the TU60 is determined by the output signals from the function decode ROM at the time TU60 START L is asserted. In the event of a READ function, the operation is similar to that described for a WRITE function except that the TADB is first loaded with data from the cassette, then the data is transferred to the bus master.

To initially achieve the correct format on the tape, it is necessary to create the load point gap at the beginning of the tape. This gap can be created by causing a WFG command to be issued when the tape is a BOT. However, if a WRITE command is issued when the tape is a BOT, the load point gap will be generated automatically by the controller hardware. Assume that a WRITE function is attempted when the tape is at BOT. The following sequence will occur: The GO command causes the two one-shots A and B to trigger, as previously described. However, the status ROM sees TU60 EOT/BOT L asserted and a WRITE function selected, and causes TA-4 ENAB REPEAT H to be asserted. This signal allows the REPEAT flip-flop to set at the leading edge of B. When REPEAT is set, two things happen: First, the data input to the READY flip-flop is held high, which prevents it from setting when it is clocked. Also, the address presented to the function decode ROM is changed. The address change is effected by making input A4 high. Thus, the original address for the WRITE command (01A), which was presented to the ROM, becomes 11A, which contains a WFG command. The trailing edge of the pulse from one-shot C sets START, and the TU60 creates a file gap instead of performing the originally selected WRITE. When TU60 READY L is asserted at the end of the WFG function, the REPEAT flip-flop is clocked and is reset. The TA11 READY flip-flop is also clocked at the same time, but does not set because the REPEAT flip-flop was set. The resetting of REPEAT restores the address of the function decode ROM to 01A (WRITE) and causes one-shot C to trigger. At the trailing edge of C, START is again set, and the TU60 performs the WRITE function, which was originally commanded by the program.

4.2.8 Interrupt Control Logic

The interrupt control logic, shown on sheet TA-2, is a combinational logic network that receives and generates the control signals required for the TA11 to become bus master. With signals TA-5 INT H and TA-5 INT ENB H both asserted, TA-2 REQUEST L will be generated if the SACK and BBSY flip-flops are not set. The TA-2 REQUEST signal is routed to the appropriate bus request line (normally BR6) through the priority plugs shown on sheet TA-4. Etch on the plug selects both request and grant lines. When the bus grant signal is generated by the processor, it is routed via the priority plug and becomes signal TA-4 BG IN H. This signal clocks the GRANT flip-flop and the SACK flip-flop. Both of these flip-flops set because the TA11 had requested bus mastership. The BBSY flip-flop is clocked and set when BUS BBSY L, BUS SSYN L, and TA-4 BG IN H are not asserted on the Unibus. Thus, the BUS BBSY L signal will be asserted again by the TA11, which is now bus master. The BBSY (0) H signal is inverted and applied to the vector address generator, generating the BUS INTR L signal and the vector address.

4.2.9 Vector Address Generator

The vector address generator consists of eight bus drivers that are used to generate a vector address and the BUS INTR L signals. When BUS BBSY L is being asserted by the TA11, the inputs to the bus drivers are active. Seven drivers are connected to the Unibus data lines D(08:02) via jumpers. The placement of these jumpers determines the vector address. The remaining bus driver is wired directly to the Unibus interrupt line.
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<th>Octal Loc</th>
<th>Binary Data</th>
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CHAPTER 5
MAINTENANCE

This chapter contains maintenance procedures for the TA11 system. The information presented covers preventive maintenance as well as troubleshooting and repair procedures.

The diagnostics for the TA11/TU60 are supplied on a maintenance cassette. The cassette stores a cassette absolute loader and the five cassette diagnostics. The primary method of loading the diagnostics utilizes a hardware bootstrap (BM792-YH) module to load the cassette absolute loader, which can then be utilized to load the diagnostic programs.

A toggle-in bootstrap may be used instead of the BM792-YH to get the cassette absolute loader into memory. The absolute and bootstrap loader program code are both listed in MAINDEC-11-DZTAF.

If failures occur that prevent the loading of the programs from cassette, the only recourse is to utilize one of the following:

1. Use the listings and troubleshoot using the loaders as diagnostics.
2. Use the tape motion toggle-in routines listed in MAINDEC-11-DZTAA-D.
3. Use the PMK02 and load diagnostics. PMK02 and TU60 cassettes are not compatible.

The maintenance philosophy of the TU60 is module replacement. The TA11 controller should be repaired to the component level.

Several procedures contained in this section pertain to the TU60. This information, however, pertains to the TU60 as a component of the TA11 system, and is included for convenience. It is not intended to supersede the maintenance information contained in Chapter 5 of the TU60 Cassette Tape Transport Maintenance Manual.

The following procedures are written for rev D M7761 Servo and Read/Write module. Read the following general comments before proceeding:

a. All measurement setups given are for actual scope settings assuming a X10 probe is used.

b. All measurements, unless otherwise stated, will be made with the channel 1 probe and the CH MODE switch is in CH1 position.

c. All measurements are made with the probe ground on the nearest ground TP for M7760 measurements — M7760-TP20; for M7761 measurement — M7761-TP13 is used. Other measurements will specify the grounding method.

d. All references to right or left will be made as one faces the front of the unit.

e. To prevent interaction, simultaneously adjust the drive A & B servos. Do not attempt any individual adjustments unless all previous adjustments have first been checked.
SAMPLE TAIL PROGRAM, CAN BE TOGGLED IN.

TA11 CONTROL AND STATUS REGISTER
TA11 DATA BUFFER REGISTER
ILBS TO BIT #4 IN TACS
READY IS BIT #5 IN TACS
R0 IS USED FOR COUNTING BYTES
R1 IS USED FOR A BUFFER POINTER
SELECT UNIT 0
USE 00040 TO SELECT UNIT 1

001000 017737 000000 177500
START: MOV #000000,**TACS

001006 112737 000017 177500
FIRST REWIND THE CASSETTE AND WAIT FOR READY

001014 032737 000040 177500
LOOP1: RIT READY,**TACS

001022 001774
RED LOOP1

001024 012700 000040 177500
ISCOND, ISSUE READ (OR WRITE) AND WAIT FOR TRANSFER REQUEST

001030 012781 002000 177500
MOV #2000,R1

001034 112737 000005 177500
MOV #5,**TACS

001042 132737 000240 177500
LOOP2: RIT #240,**TACS

001050 001774
REG LOOP2

001052 100021
RPL ERROR

001054 005300
TRANSFER REQUEST IS UP, SO READ DATA (OR WRITE DATA) OR ISSUE ILBS

001056 100483
DEC R0

001060 113721 177502
RMI LOOP3

001064 000766
MOV #TADR,(R1)+

001066 052737 000020 177500
LOOP3: RIS #ILBS,**TACS

001074 037737 000040 177500
LOOP4: RIT READY,**TACS

001100 000731
ERROR HALT, PROGRAM HALTS HERE IF THERE IS A TAIL ERROR.

001116 000000
ERROR: WAIT

001120 000727
BR START

Maintenance Program Example

5-3
5.1 VOLTAGE VERIFICATION

On the left side of the M7761 (top module) is an 8-pin Amphenol connector (J7). Pin numbers are from left to right.

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<tr>
<th>Voltage</th>
<th>Pin</th>
<th>Scale</th>
<th>Notes</th>
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</thead>
<tbody>
<tr>
<td>+15 VDC</td>
<td>J7-Pin 1</td>
<td>5V/div</td>
<td>+5 ± 1.4 Vdc (300 mV P-P ripple)</td>
</tr>
<tr>
<td>-15 VDC</td>
<td>J7-Pin 2</td>
<td>5V/div</td>
<td>-15 ± 1.4 Vdc (300 mV P-P ripple)</td>
</tr>
<tr>
<td>+5 VDC</td>
<td>J7-Pin 4</td>
<td>1V/div</td>
<td>+5 ± 0.25 Vdc (50 mV P-P ripple)</td>
</tr>
<tr>
<td>+12 VDC</td>
<td>M7761-TP46</td>
<td>5V/div</td>
<td>+12, +2V Vdc (100 mV P-P ripple)</td>
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<tr>
<td>-12 VDC</td>
<td>M7761-TP47</td>
<td>5V/div</td>
<td>-12, +2 Vdc (100 mV P-P ripple)</td>
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</tbody>
</table>

*Div: only available adjustment for these voltages occurs for the ±12V. If this voltage is out of tolerance, adjustment should occur as directed in Paragraph 5.9.

5.2 COARSE TACHOMETER ADJUSTMENT

**NOTE**

This adjustment is done to prevent motor damage on a completely out-of-adjustment servo. This adjustment, under normal conditions need not be done; however, it should be checked as a precautionary measure whenever the state of the drive is unknown. If this adjustment is required, the motors will be vibrating (humming).

1. Load cassette into drives A and B and perform manual rewind on both drives.

2. Set the oscilloscope controls as follows:
   a. HORIZONTAL DISPLAY A TIME BASE
   b. A SWEEP MODE AUTO TRIGGER
   c. A SWEEP TIME 2 ms/div
   d. CH1 GAIN .2V/div, dc

3. Connect the oscilloscope probe to TP20 (AMP A) and observe the scope display for oscillations or creep (M7761) (Figure 5-1).

4. If either are present, adjust Tach Pot A counterclockwise until no ac signal is present. Continue to turn Tach Pot A another two turns counterclockwise.

   Tach Pot A is the only pot on the drive A terminator module. This module is mounted on the assembly containing the control and tension motor for unit A (left side).

5. Connect the oscilloscope probe to TP9 (AMP B) and again observe for indications of creep or oscillation.
6. If either are present, adjust Tach Pot B counterclockwise until no ac signal is present. Continue to turn Tach Pot B another two turns counterclockwise. Tach Pot B is the only pot on the drive B terminator module.

**NOTE**
These pots can be easily accessed by swinging the logic modules to their up positions.

### 5.3 COARSE SPEED ADJUSTMENT

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Set the oscilloscope controls as follows:
   a. HORIZONTAL DISPLAY A TIME BASE
   b. A SWEEP MODE AUTO TRIGGER
   c. A SWEEP TIME 2 ms/div
   d. CH1 GAIN .1V/div dc

3. Connect the oscilloscope probe to TP24 (SPEED A) on the M7761 module.

4. Toggle in the following program:
   - 200/013737 MOVE SWR to CSR
   - 177570
   - 177500
   - 000137 JMP 200
   - 000200

5. Load address 200, set Switch register (SWR) to 00005 (drive A), and press START.

6. Adjust Speed Pot A on the M7761 module for a $-2.7 \pm 0.5$ Vdc scope indication:

7. Halt the program.
8. Connect the oscilloscope probe to TP2 (AMP B).

9. Load address 200, set SWR to 00405 (drive B), and start the read forward.

10. Adjust Speed Pot B on the M7761 module for a \(-2.7 \pm 0.5\) Vdc scope indication.

11. Halt the program.

Coarse speed adjustment has now been performed on both drives.

5.4 CONTROL MOTOR SOLENOID ADJUSTMENT

1. Unload the cassette from both drives.

2. Set the oscilloscope controls as follows:
   a. HORIZONTAL DISPLAY
   b. A SWEEP MODE
   c. A SWEEP TIME
   d. CH1 GAIN
   A TIME BASE
   AUTO TRIGGER
   2 ms/div
   .1V/div, dc

3. Place logic modules in their up position.

4. Connect the oscilloscope probe and ground across the two test points (TP2 high, TP1 ground) on the edge of the terminator module beneath the assembly for drive A (left side).

   **NOTE**
   Be careful not to affect motor position or cause side-to-side motion with the oscilloscope probe.

5. Load address 200, set SWR = 00005, and press START

6. First cover drive A photosensor with masking tape (simulate tape presence), then tape down one of the cassette-present microswitches (simulate cassette presence).

   The lower spindle should start rotating at approximate read speed.

7. Monitor the scope display for a \(-225\) to \(-275\) mV average dc indication (Figure 5-2).

8. Halt the program.

![Figure 5-2 Control Motor Solenoid Adjustment Waveforms](image-url)
9. Using diagnostic 11-DZTAD, read continuous blocks of data from drive B.
   a. Load address 230
   b. Load address 200, set SWR = 00405, and press START

10. First cover drive B photosensor with masking tape (simulate tape presence), then tape down one of the cassette-present microswitches (simulate cassette presence). The lower spindle should begin rotating at approximate read speed.

11. Connect the oscilloscope probe and ground across the two test points (TP2 high, TP1 ground) on the edge of the terminator module beneath the assembly for drive B (right side).

   NOTE
   Be careful not to affect motor position or cause side-to-side motion with the scope probe.

12. Monitor the scope display for a ~225 to ~275 mV average dc indication (Figure 5-2).
   If the voltage is not correct, loosen the two solenoid mounting screws and slide the solenoid up or down until the proper voltage is obtained.

   NOTE
   Access to the screws for drive B solenoid can be obtained by removing drive A from the frame (4 screws).

13. Halt the program. The control motor solenoid is adjusted on drives A and B. Lower modules to their original position.

5.5 BALANCE ADJUSTMENT

   NOTE
   Drives must be mounted in frame and chassis for all the following adjustments.

1. Load a cassette into drive B (right side). Cassette is loaded into drive opposite the one to be tested.

2. Set the oscilloscope controls as follows:

   a. HORIZONTAL DISPLAY  A TIME BASE
   b. A SWEEP           AUTO TRIGGER
   c. A SWEEP TIME       5 ms/div
   d. CH1 GAIN           20 mV/div, dc

3. Connect the oscilloscope probe to TP20 (AMP A) and adjust Balance Pot A on the M7761 module for a 0V ± 200 mV indication.

4. Remove the cassette from drive B and load it into drive A.

5. Connect to scope probe to TP9 (AMP B) and adjust Balance Pot B a 0V ± 200 mV indication.
5.6 FINE TACHOMETER ADJUSTMENT

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Set the oscilloscope controls as follows:
   a. HORIZONTAL DISPLAY A TIME BASE
   b. A SWEEP MODE AUTO TRIGGER
   c. A SWEEP TIME 2 ms/div
   d. CH1 GAIN .2V/div, dc

3. Raise modules to their up position.

4. Connect the oscilloscope probe to TP20 (AMP A) of the M7761 module.

5. Load address 200, set SWR to 00005, and press START.

6. Adjust Tach Pot A (located on the drive A terminator module) clockwise until oscillations occur. Then back off until they stop. Then back off 1-1/4 more turns (Figure 5-3).

![Oscillations Diagram]

Figure 5-3  Fine Tachometer Adjustment Waveforms
7. Halt the processor.

8. Connect the oscilloscope probe to TP9 (AMP B) of the M7761 module.

9. Load address 200, set SWR at 00005, and press START.

10. Adjust Tach Pot B (located on the drive B terminator module) clockwise until oscillations occur. Then back off 1-1/4 more turns (same indications as above).

11. Halt the processor and return modules to their original position.

NOTE
The following adjustment requires use of a speed/azimuth reference cassette TU60-R. This cassette is available from product support.

5.7 FINE SPEED ADJUSTMENT

1. Load the speed/azimuth reference cassette (speed label out) into drive A, and a cassette into drive B. Perform a manual rewind on both drives.

2. Set the oscilloscope controls as follows:
   a. HORIZONTAL DISPLAY
   b. A SWEEP MODE
   c. A SWEEP TIME
   d. CH1 GAIN
   e. A TRIGGER

   A TIME BASE
   NORMAL TRIGGER
   .2 ms/div
   .2V/div, dc
   CHANNEL 1 ONLY
   SLOPE +
   LEVEL +
   HFREJ
   INTERNAL

3. Connect the oscilloscope probe to TP2 (AMP 2 OUT) of the M7761 module.

4. Load address 200, set SWR to 00005, and press START.

5. Adjust Speed Pot for drive A until the interval between positive pulses equals 1 ms ± .05 ms or what is called out on label of speed/azimuth cassette.

6. Halt the processor.

7. Perform a manual rewind on both drives.

8. Load the reference cassette into drive B and load a cassette into drive A.

9. Load address 200, set SWR to 00405, and press START.

10. Connect the oscilloscope probe to TP2 (AMP 2 OUT) of the M7761 module as in step 3.

11. Adjust Speed Pot for drive B until the interval between positive pulses equals 1 ms ± .05 ms or what is called out on label of the speed/azimuth cassette (see waveform in Figure 5-4).
12. Halt the processor. Rewind (manual) drive B.

5.8 HEAD AZIMUTH (SKEW) ADJUSTMENT

NOTE
The following adjustment requires use of a speed/azimuth reference cassette. This cassette is available from PDP-8 product support.

1. Load the speed/azimuth reference cassette into drive A. Perform a manual rewind on drive A (azimuth) label out).

2. Set the oscilloscope controls as follows:
   
a. HORIZONTAL DISPLAY
b. A SWEEP MODE
c. A SWEEP TIME
d. CH1 GAIN
e. A TRIGGER
   
   A TIME BASE
   NORMAL OR AUTO TRIGGER
   .2 ms/div
   20 mV/div, dc
   CHANNEL 1 ONLY
   SLOPE +
   LEVEL +
   HFREJ
   INTERNAL

3. Load address 200, set SWR to 00005, and press START.

4. Connect the oscilloscope probe to TP2 (AMP 2 OUT) of the M7761 module.

5. Turn the head alignment screw (directly below tape head, accessible from front of drive) for drive A. Adjust for a minimum peak-to-peak signal. The pulse pairs (at a 1-kHz rate) should be less than 750 mV PP. Hold the cassette pressed back lightly to simulate the door action, especially near the head. Check with door closed. (See Figure 5-5.)

Figure 5-5 Head Azimuth Alignment Waveform
6. Halt the processor. Rewind drive A.

7. Load the reference cassette into drive B.

8. Load address 200, set SWR = 00405, and press START.

9. Turn the head alignment screw (directly below tape head, accessible from front of drive) for drive B, right side.

   Adjust for a minimum peak-to-peak signal. The pulse pairs (at a 1-kHz rate) should be less than 750 mV PP. Hold the cassette pressed back lightly to simulate the door action, especially near the head. Check with door closed.


5.9 DECELERATION RAMP (-12 Vdc REGULATOR) ADJUSTMENT

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Set the oscilloscope controls as follows:

   a. HORIZONTAL DISPLAY     A INTEN BY B
   b. A SWEEP MODE            NORMAL TRIGGER
   c. A SWEEP TIME             20 ms/div
   d. B SWEEP MODE             B SWEEP STARTS AFTER A TIME
   e. B SWEEP TIME             5 ms/div
   f. CH1 GAIN                 .1V/div, dc
   g. A TRIGGER                
      { CHANNEL 1 ONLY
      SLOPE "-" "-"
      LEVEL "-" "-"
      INTERNAL
      HFREJ

3. Connect the oscilloscope probe to TP25 (AMP A) of the M7761 module.

4. Using diagnostic DZTAD, write continuous data blocks on drive A. (byte count = 1, data = 0s)

   a. Load address: 244
   b. Press START.
   c. At 1st halt, set SWR 7:0 to 000. Press CONTINUE.
   d. At 2nd halt, press CONTINUE.
   e. At 3rd halt, set SWR 15:0 = operations switches: SW 14 = 1
      loop on test, 13 = 1 inhibit error printout, 9 = 1
      loop on error, 7 = 1 lock on selected drive.
   f. Press CONTINUE; tape should write forward.

5. Adjust the oscilloscope controls to obtain waveform A in Figure 5-6. Intensity and delay time multiplier controls may have to be adjusted to obtain this waveform.

6. Expand the sweep by switching the oscilloscope horizontal display control to B DELAYED BY A.
Figure 5-6  Deceleration Ramp Adjustment Waveforms

7. Measure the negative slope time (X). Measure the positive slope time (Y). If (Y) is not 2 ms longer than (X), adjust R168 (-12V regulator adjust) on the M7761 module until (X) + 2 ms = (Y). Example: If Y = 17 ms, then X should equal 15 ms.

8. Halt the processor and rewind the drive.

5.10 WRITE FILE GAP ONE-SHOT ADJUSTMENT

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Set the oscilloscope controls as follows:

   a. HORIZONTAL DISPLAY  
   b. A SWEEP MODE  
   c. A SWEEP TIME  
   d. CH1 GAIN  
   e. A TRIGGER

       A TIME BASE
       NORMAL TRIGGER
       .1 sec/div
       .2V/div, dc

       CH1 ONLY
       SLOPE +
       LEVEL +
       LFREJ
       INTERNAL
3. Using diagnostic DZTAD perform repetitive WRITE FILE GAP operations on drive A.
   a. Load address: 220
   b. Set operational switches:
      SW 14 = 1 loop on test
      13 = 1 inhibit error printout
      9 = 1 loop on error
      7 = 1 lock on select drive
   c. Press START; tape should write forward.

4. Raise modules to their up position.

5. Connect the oscilloscope probe to TP2 (WF GAP H) of the M7760 module.

6. Adjust R12 (Pot A) on the M7760 module until t = 535 ms ± 20 ms. (See Figure 5-7.)

![Waveform Diagram](image)

Figure 5-7 Write File Gap One-Shot Adjustment Waveform

7. Halt the processor and rewind drive A.

5.11 GAP TIME ONE-SHOT ADJUSTMENT

1. Load cassettes into drives A and B and perform manual rewind on both drives.

2. Set the oscilloscope controls as follows:
   a. HORIZONTAL DISPLAY
   b. A SWEEP MODE
   c. A SWEEP TIME
   d. CH1, CH2 GAIN
      - CH1 ONLY
      - SLOPE —
      - LEVEL —
      - LFREJ
      - INTERNAL
   e. A TRIGGER
      - CHOP
   f. CHNL MODE

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3. Using diagnostic DZTAD, write continuous data blocks on drive A (byte count = 1, data = 0):
   a. Load address: 224
   b. Press START.
   c. At first halt, set SWR 7:0 = bytes/block = 001. Press CONTINUE.
   d. At second halt, set SWR 7:0 = pattern = 000. Press CONTINUE.
   e. At third halt, set SWR 15:0 = operational switches:
      SW 14 = 1 loop on test
      13 = 1 inhibit error printout
      9 = 1 loop on error
      7 = 1 lock on selected drive
   f. Press CONTINUE; tape should write forward.

4. Raise modules to their up position if not already done.

5. Connect the oscilloscope probes: channel 1 to TP6 (DRIVE L) and channel 2 to TP17 (GAP TIME H) of the M7760 module.

6. Adjust R23 (Pot B) on the M7760 until t = 40 ± 2 ms; t1 should equal 30 ± 5 ms (Figure 5-8).

![Figure 5-8 Gap Time One-Shot Adjustment Waveforms](image)

7. Halt the processor and rewind drive A.

5.12 THRESHOLD ADJUSTMENT

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Using diagnostic DZTAD, write continuous data blocks on drive A (byte count = 1, pattern = 377):
   a. Load address: 224
   b. Press START.
   c. At first halt, set SWR 7:0 = bytes/block = 001. Press CONTINUE.
   d. At second halt, set SWR 7:0 = pattern = 377. Press CONTINUE.
e. At third halt, set SWR 15:0 = operational switches:
   SW 14 = 1 loop on test
   13 = 1 inhibit error printout
   9 = 1 loop on error.
f. Press CONTINUE; tape should write forward.

3. After writing for about 10 seconds, halt the processor.
   
   NOTE
   Since the tape speed and read signal amplitude varies as the tape
   winds up, this adjustment must be done at the beginning 10
   seconds of tape.

4. Set the oscilloscope controls as follows:

   a. HORIZONTAL DISPLAY  A TIME BASE
   b. A SWEEP MODE  NORMAL TRIGGER
   c. A SWEEP TIME  2 ms/div
   d. GAIN CHNL 1-  .1V/div
      CHNL 2-  .2V/div
   e. A TRIGGER
      CHANNEL 1 ONLY
      SLOPE +
      LEVEL +
      HFREJ
      INTERNAL
   f. CHANNEL MODE  CHOP

5. Connect the channel 1 oscilloscope probe to TP33 (threshold delay) and the channel 2 probe to TP31
   (ENERGY H) of the M7761 module.

6. Using diagnostic DZTAD, read continuous data blocks from drive B.

   a. Load address: 230
   b. Setup operational switches:
      SW 14 = 1 loop on test
      13 = 1 inhibit error printout
      9 = 1 loop on error
      7 = 1 lock on selected drive
   c. Press START: tape should read forward. Loop on error switch will cause a rewind to occur
      when the tape reads off of the formatted 10 seconds, and another read forward is then initiated.

7. Adjust R142 (Threshold Pot) on the M7761 until t = 1 ms ± .05 ms (Raise modules to up position to
   access pot). (see Figure 5-9).

8. Put SW 7 on a 0 so that drive A becomes selected, then put SW 7 on a 1 again to hold program on
   drive A.

9. Compare the time t, being displayed for drive A, with the time that drive B was adjusted for (1 ms ±
   0.5 ms).

10. If t for drive A is longer, adjust R142 (Threshold Pot) on the M7761 for 1 ms ± .05 ms.
11. If t for drive A is shorter, the adjustment is complete.

12. Halt the processor and rewind drives A and B.

5.13 SIGNAL ONE-SHOT ADJUSTMENT

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Using diagnostic DZTAD, write file gaps and data blocks on drive A (byte count = 1, pattern = 000):
   
   a. Load address: 234
   b. Press START.
   c. At first halt, set SWR 7:0 = bytes/block = 001.
   d. At second halt, set SWR 7:0 = pattern = 000. Press CONTINUE.
   e. At third halt, set SWR 15:0 = operational switches:
      SW 14 = 1 loop on test
      13 = 1 inhibit error printout
      9 = 1 loop on error
      7 = 1 lock on selected drive
   f. Press CONTINUE; tape should write forward. Record almost all of the tape, then halt the processor.

3. Set the oscilloscope controls as follows:
   
   a. HORIZONTAL DISPLAY
   b. A SWEEP MODE
   c. A SWEEP TIME
   d. GAIN CHANNEL 1
      CHANNEL 2
     
     CHANNEL 1 ONLY
     SLOPE +
     LEVEL +
     HFREJ
     INTERNAL
   e. A TRIGGER
   f. CHANNEL MODE
     
     A TIME BASE
     NORMAL TRIGGER
     20 ms/div
     .2V/div
     .2V/div

5-16
4. Using diagnostic DZTAD, search for file gaps on drive A.
   a. Load address: 244
   b. Set operational switches:
      SW 14 = 1 loop on test
      13 = 1 inhibit error printout
      9 = 1 loop on error
      7 = 1 lock on selected drive.
   c. Press START; tape should rewind and then search forward.

5. Connect the channel 1 oscilloscope probe to TP2 (AMP 2 OUT) and channel 2 to TP39 (SIGNAL L) of the M7761 module.

6. Adjust R130 (signal) on the M7761 module until $t = 150 \pm 5$ ms (Figure 5-10).

7. Halt the processor.

8. Using diagnostic DZTAD, read data and file gaps from drive A.
   a. Load address: 240
   b. Set operational switches:
      SW 14 = 1 loop on test
      13 = 1 inhibit error printout
      9 = 1 loop on error
      7 = 1 lock on selected drive
   c. Press START; tape should rewind and then read forward.

9. Change the oscilloscope sweep time to 5 ms/div.

10. The value for $t$ should now equal 13 to 15 ms. If time indication is not within tolerance, adjust R130 (signal) until the time is just within tolerance. Set oscilloscope sweep time back to 20 ms/div.

11. Return to step 4 and perform the steps 4 through 11 until both are within tolerance.

12. Allow the tape to read forward until the far end of tape is near and then halt the processor.

13. Change the oscilloscope sweep time to 10 ms/div.

Figure 5-10  Signal One-Shot Adjustment Waveforms
14. Using diagnostic DZTAD, backspace file gaps on drive A.
   a. Load address: 250
   b. Set operational switches:
      SW 14 = 1 loop on test
      13 = 1 inhibit error printout
      9 = 1 loop on error
      7 = 1 lock on selected drive
   c. Press START; tape should read backward.

15. Check that $t$ equals 65 to 85 ms.

16. Halt the processor and rewind drive A.

5.14 TAPE BLANK ONE-SHOT ADJUSTMENT

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Set the oscilloscope controls as follows:
   a. HORIZONTAL DISPLAY
   b. A SWEEP MODE
   c. A SWEEP TIME
   d. GAIN CHANNEL 1
   e. A TRIGGER
   f. CHANNEL MODE
      \[
      \begin{align*}
      &\text{A TIME BASE} \\
      &\text{NORMAL TRIGGER} \\
      &50 \text{ ms/div} \\
      &.2V/\text{div}, \text{dc} \\
      &.2V/\text{div}, \text{dc} \\
      &\text{CHANNEL 1 ONLY} \\
      &\text{SLOPE +} \\
      &\text{LEVEL +} \\
      &\text{LFREJ} \\
      &\text{INTERNAL} \\
      &\text{CHOP}
      \end{align*}
      \]

3. Using diagnostic DZTAD, perform repetitive read data and read file gap operations on drive A.
   a. Load address: 240
   b. Set operation switches:
      SW 14 = 1 loop on test
      13 = 1 inhibit error printout
      9 = 1 loop on error
      7 = 1 lock on selected drive
   c. Press START; tape should read forward.

4. Connect the channel 1 oscilloscope probe to TP39 (SIGNAL L) of the M7761.

5. Raise modules to their up position and connect the channel 2, oscilloscope probe to TP6 (DRIVE L) of the M7760.

6. Adjust R24 (Pot C) on the M7760 module until $t = 385 \pm 15$ ms.

7. Halt the processor and rewind drive A.
Figure 5-11  Tape Blank One-Shot Adjustment Waveforms
APPENDIX A
SAMPLE MAINTENANCE PRINTOUT

S
MAINDEC-11-DZTAA-A
TESTING DRIVE A

TESTING DRIVE B
TESTING DRIVE A
TESTING DRIVE B

MAINDEC-11-DZTAB-A
TESTING DRIVE A
TESTING DRIVE B
TESTING DRIVE A
TESTING DRIVE B

MAINDEC-11-DZTAC-A
TESTING DRIVE A

DIRECTIONS WILL BE TYPED ON THE TTY
HIT 'CR' WHEN READY TO CONTINUE

POWER DOWN TU60
POWER UP TU60
REMOVE CASSETTE FROM DRIVE UNDER TEST
REPLACE CASSETTE
SET WRITE LOCK
SET WRITE ENABLE

(Continued on next page)
TESTING DRIVE B
POWER DOWN TU60
POWER UP TU60
REMOVE CASSETTE FROM DRIVE UNDER TEST
REPLACE CASSETTE
SET WRITE LOCK
SET WRITE ENABLE
TESTING DRIVE A
POWER DOWN TU60

MAINDEC-11-DZTAD-A
TESTING DRIVE A AND DRIVE B
TESTING DRIVE B AND DRIVE A
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What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? __________________________________________

________________________________________________________________________

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What features are most useful? __________________________________________

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What faults do you find with the manual? __________________________________

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Does this manual satisfy the need you think it was intended to satisfy? __________

Does it satisfy your needs? ___________ Why? ______________________________

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