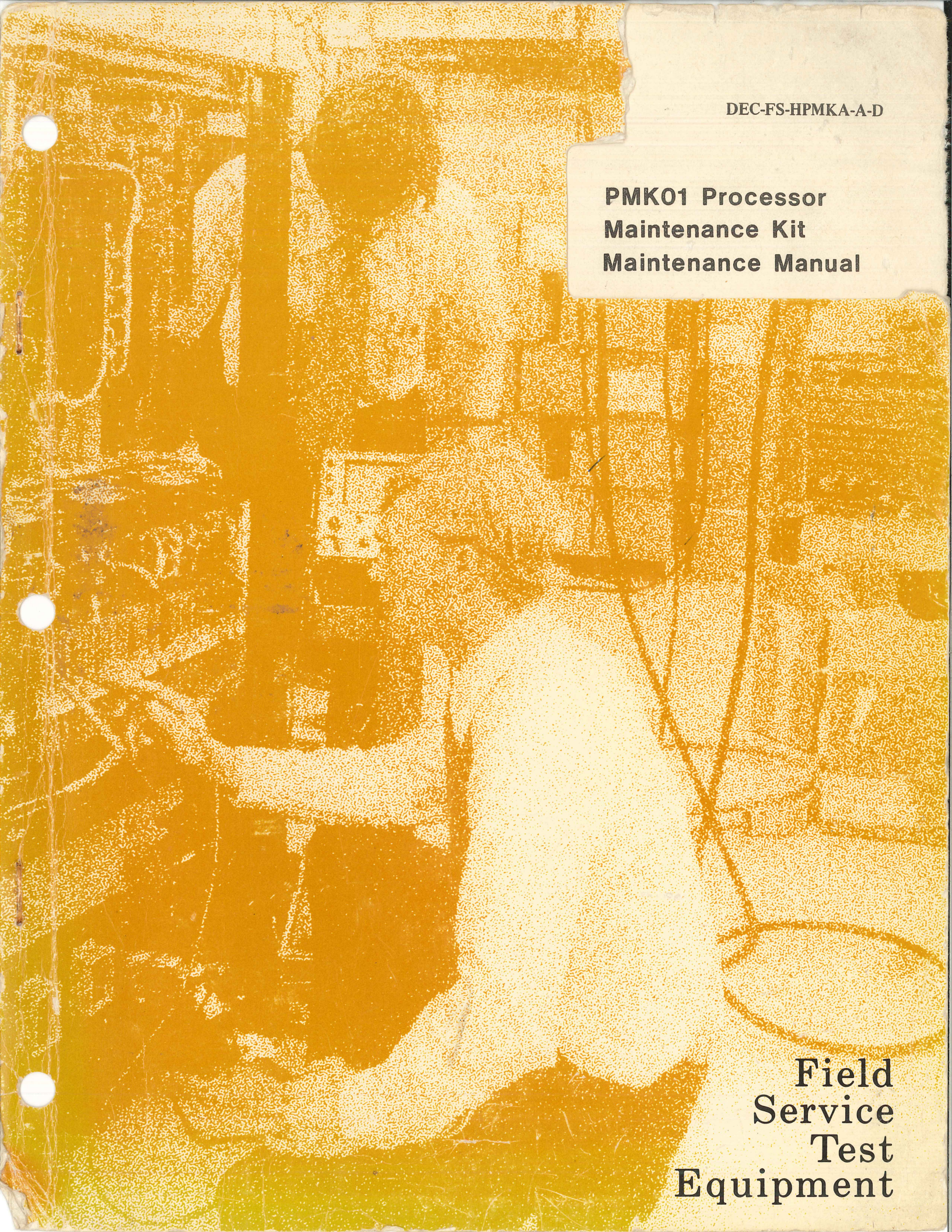
DEC-FS-HPMKA-A-D

PMK01 Processor Maintenance Kit Maintenance Manual



Field Service Test Equipment

DEC-FS-HPMKA-A-D

PMK01 Processor Maintenance Kit Maintenance Manual

DC POWER CABLE/BOARD CAN GO IN ANY E SOCKET IN PROC/MEM SECTION OF THE BACKPLANE.

digital equipment corporation · maynard, massachusetts

1st Edition, April 1974

Printed in U.S.A.

CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

ILLUSTRATIONS

ILLUSTRATIONS (Cont)

TABLES

PMK01 Processor Maintenance Kit

PMK01 PROCESSOR MAINTENANCE KIT MAINTENANCE MANUAL

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides a complete description of the PMK01 (Processor Maintenance Kit) including physical, functional, and detailed descriptions; programming, utilization, and maintenance information; and equipment specifications.

1.2 GENERAL DESCRIPTION

The PMK01 is a portable, high speed, paper-tape reader capable of loading diagnostic programs into PDP-8E/8F/8M and PDP-11 computers. The unit is designed to facilitate diagnostic program loading on computer systems that are not equipped with a high speed paper-tape reader or other rapid means of loading diagnostic programs.

The two different configurations used in the PMK01 are the PDP-8E/8F/8M configuration and the PDP-11 configuration. Block diagrams are illustrated in Figures 1-1 and 1-2.

The PMK01 is housed in a field carrying case and is equipped with a 3-wire ac input power cord that provides power to drive the reader motor, and with a 3-wire dc power cable assembly that provides power to the logics and the reader light source.

1.3 PHYSICAL DESCRIPTION

The PMK01 consists of the following components: (Figures 1-3 and 1-4)

- Carrying Case
- Reader Plate Assembly
- Photo Transistor Amplifier Module (G918)
- Solenoid Driver Module (M060)
- Reader Control Module (M7050-YA)
- Reader Clock Module (M715-YA)
- Jumper Board Module (W025)
- Reader/Punch Control Module (M840-YA)
- PC11 Interface Module (M7810)
- Wired Assembly
- DC Power Cable
- BC08 Interface Cables
- H851 Edge Connector
- Reader Software Maintenance Kits

1.3.1 Reader Plate Assembly (70-06573-03)

See Appendix A for an IPB (Illustrated Parts Breakdown) of the reader plate assembly; this assembly has been modified to exclude the reader selected indicator used on the PR68-D Reader Plate Assembly.

1.3.2 Photo Transistor Amplifier Module (G918)

The G918 is a dual height module which mounts in slot 2 of the wired assembly and contains all the logic necessary to amplify the data and feed hole signals generated by the reader plate assembly. (Refer to engineering drawing C-CS-G918-0-1 for physical layout and parts description.)

1.3.3 Solenoid Driver Module (M060)

The M060 is a single height module which mounts in slot A3 of the wired assembly. This module contains switching circuits which control the current to the reader drive motor. (Refer to engineering drawing B-CS-M060-0-1 for parts identification.)

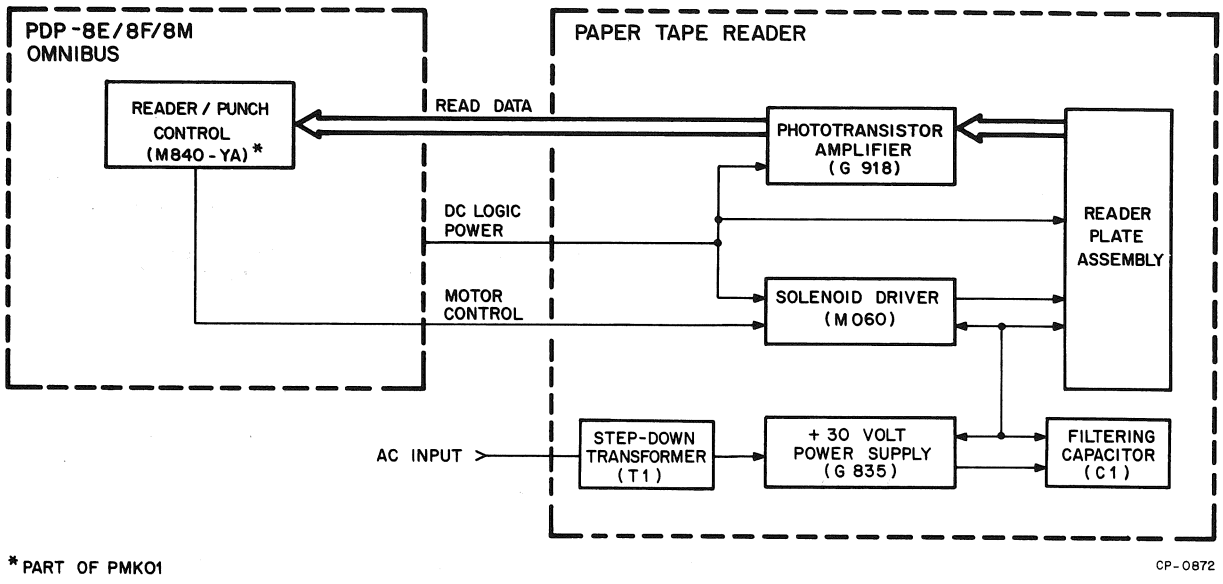


Figure 1-1 PDP-8E/8F/8M Configuration Block Diagram

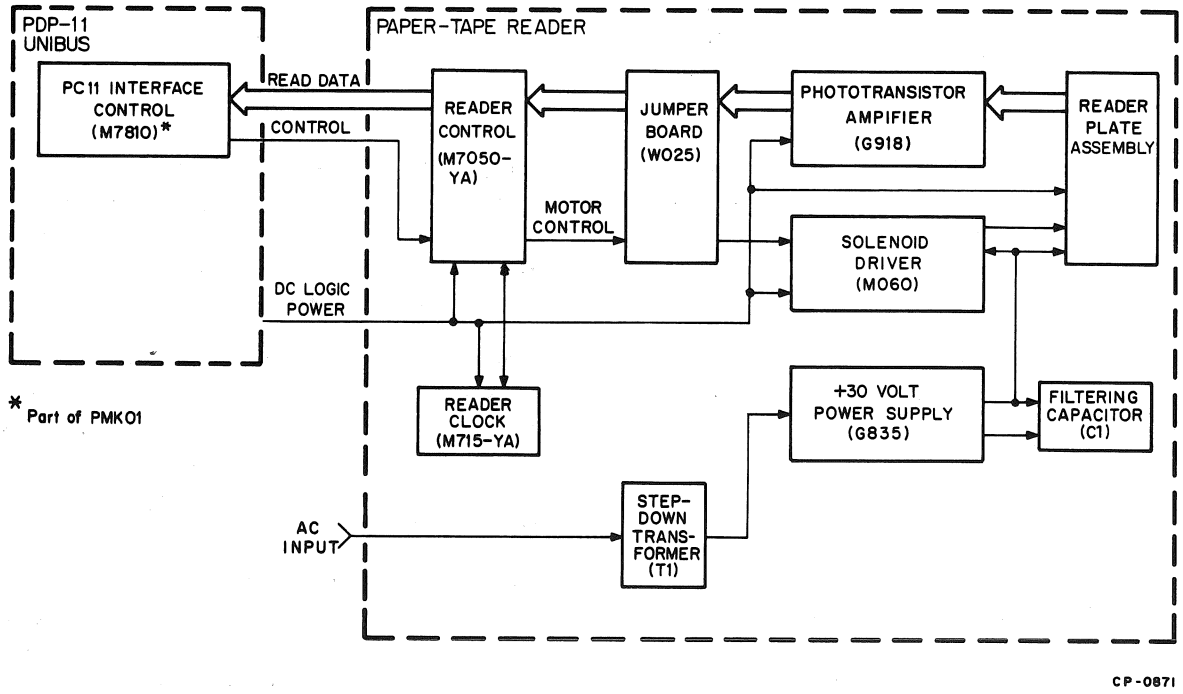


Figure 1-2 PDP-11 Configuration Block Diagram

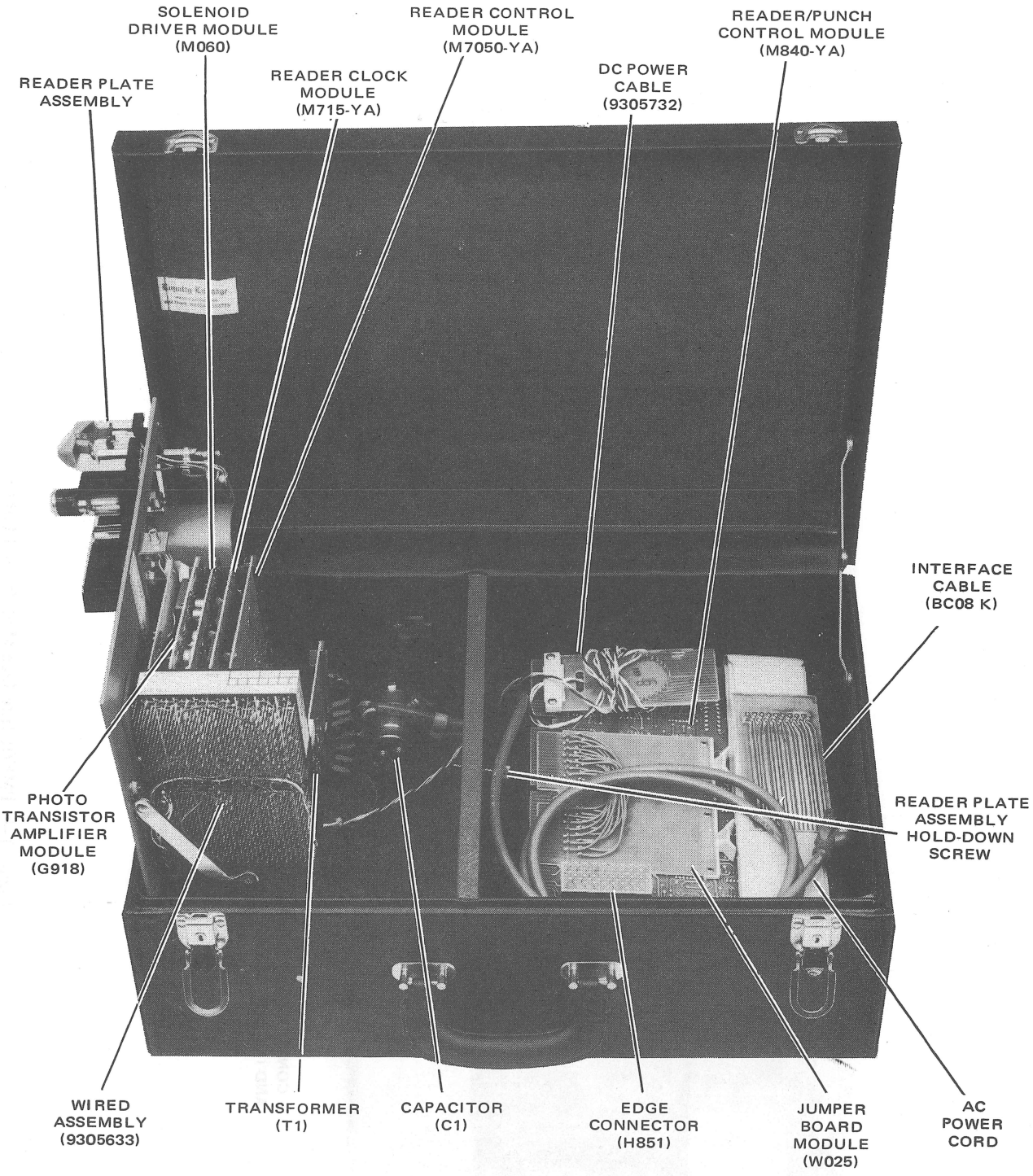


Figure 1-3 PMK01 Components

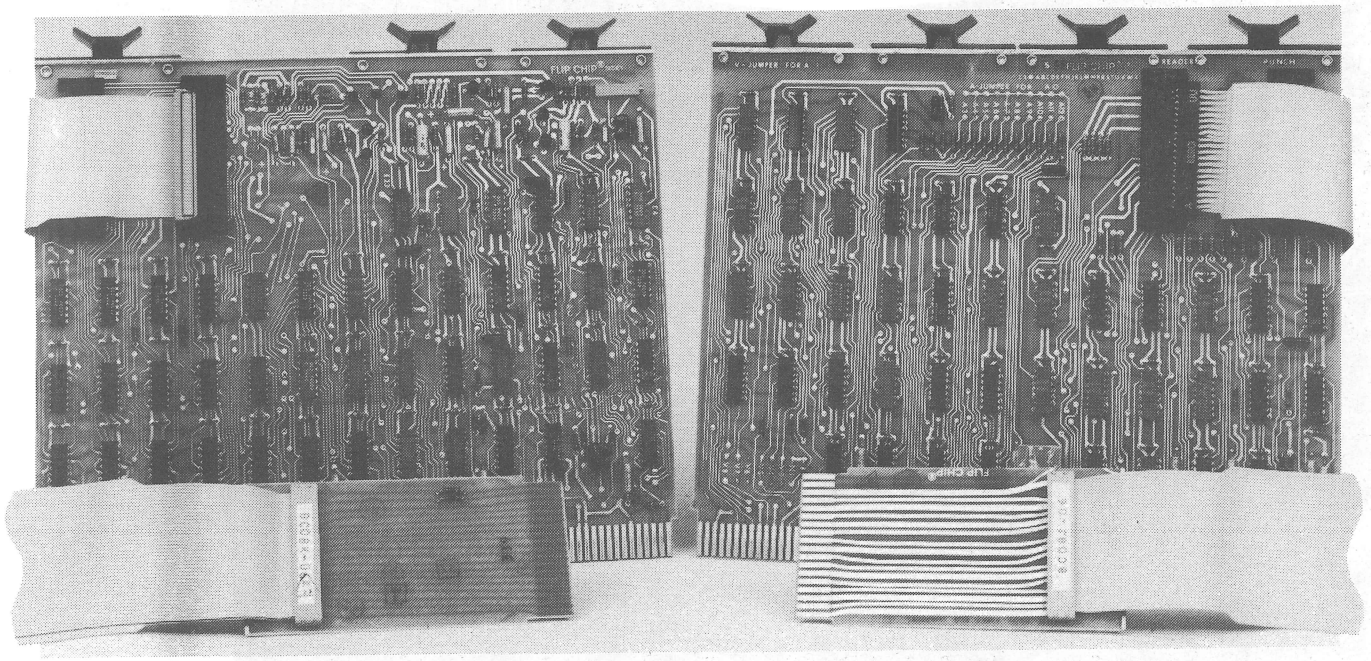


Figure 1-4 PMK01 Interface Modules and Cables

1.3.4 Reader Control Module (M7050-YA)

The M7050-YA is a dual height module which mounts in slot 4 of the wired assembly. In response to PDP-11 computer initiated inputs, this module controls the solenoid drivers and the transfer of read data when the paper-tape reader is interfaced with a PDP-11 computer. (Refer to engineering drawing D-CS-M7050-YA-1 for physical layout and parts description.)

1.3.5 Reader Clock Module (M715-YA)

The M715-YA is a dual height module which mounts in slot 5 of the wired assembly. This module generates all timing required by the paper-tape reader when the reader is interfaced with a PDP-11 computer. (Refer to engineering drawing D-CS-M715-YA-1 for physical layout and parts identification.)

1.3.6 Jumper Board Module (W025)

This W025 is a dual height module which is mounted in slot 6 of the wired assembly *only* when the paper-tape reader is interfaced with a PDP-11 computer – otherwise the jumper board must be removed. The jumper board provides wiring for the additional signal routing which is necessary in the PDP-11 configuration. (Refer to engineering drawing D-IA-9305647-0-0 for physical layout and wiring data.)

1.3.7 Wired Assembly (9305633)

The wired assembly consists of an 8-slot, dual height connector block with backpanel wiring which distributes dc power and interconnects all 8 slots.

1.3.8 DC Power Cable (9305632)

The dc power cable consists of a 3-wire, 9-foot cable harness and one connector. The connector mounts in section A of computer bus (Unibus or OMNIBUS) and the harness wires connect to the PMK01 wired assembly. The cable routes dc power from the computer to the paper-tape reader. (Refer to engineering drawing C-IA-9305632-0-0 for physical layout and wiring data.)

1.3.9 Reader/Punch Control Module (M840-YA)

The M840-YA is a quad height module which mounts in the PDP-8E/8F/8M computer OMNIBUS. This module not only performs all the functions necessary to interface the paper-tape reader to the PDP-8E/8F/8M computer, but also controls the solenoid drivers and the transfer of read data to the PDP-8E/8F/8M computer. (Refer to engineering drawing E-CS-M840-YA-1 for physical layout and parts identification.)

1.3.10 PC11 Interface Module (M7810)

The M7810 is a quad height module which mounts in the PDP-11 Computer Unibus. This module performs all the functions necessary to interface the paper-tape reader to PDP-11 computer. (Refer to engineering drawing E-CS-M7810-0-1 for physical layout and parts identification.)

NOTE

The M7810 module is a direct replacement from the M781, M782, and M105 modules which were used in earlier model PMK01's.

1.3.11 Interface Cables

Two interface cables are provided with the PMK01: The BC08K which is used with the M840-YA module, and the BC08J which is used with the M7810 module. These cables route all control and data signals between the paper-tape reader and the interface modules which mount in the computer.

1.3.12 H851 Edge Connector

The H851 is provided for use in the PDP-11 configuration when all power sections (section A) on the Unibus are taken. Simply plug the dc power cable connector (W023) into the edge connector and mount the edge connector to the edge of a processor module that has the required dc voltage.

1.3.13 Reader Software Maintenance Kits

Two software maintenance kits are provided with the PMK01: 1) The PDP-8E kit (LIBKIT-8E-PC8E-0-1) contains a program identification document, and a PDP-8E reader test program tape (MAINDEC-8E-DZCA-D-PB). 2) The PDP-11 kit (LIBKIT-11-PC11-06) contains a program identification document, a PDP-11 reader test program tape (MAINDEC-11-DZBA-PB), a special binary count tape (MAINDEC-00-D2G4-PT), and an alternate ones and zeros tape (MAINDEC-00-D2G2-PT). The kits are used to check out the paper-tape reader and the reader interface and control logic.

1.4 SPECIFICATIONS

1.4.1 Environmental

Ambient Temperature
50° to 100° F (67° to 73° F nominal) operating

Relative Humidity
8 to 80% (without condensation)

1.4.2 Power Requirements

Input Power (ac)
PMK01-CA 115V @ 60 Hz, 1A max
PMK01-CB 230V @ 50 Hz, 1A max

Motor Power (dc)
+30 Vdc, 800 mA

Logic Power (dc)
+5 Vdc (±0.15 V), 710 mA, 0.7 A
-15 Vdc (±0.45 V), 1010 mA, 1A

1.4.3 Reader Speed

Continuous reading
110 (±5) cps (characters per second)

Single character
19–23 cps

1.4.4 Paper Tape

Non-oiled with less than 12% transmissivity.

1.4.5 Carrying Case Dimensions

Height
13 in.

Width
19 in.

Depth
9 in.

Weight
less than 25 lb

CHAPTER 2
UNPACKING, SET-UP, ACCEPTANCE TESTING

2.1 UNPACKING PROCEDURE

To unpack the PMK01:

1. Remove the carrying case from the shipping carton and inspect for exterior damage. Damage claims should be directed to the responsible shippers.

2. Open the carrying case and inspect the PMK01 components for damage.

3. Verify that all components are present. (See Paragraph 1.3 for kit contents.)

2.2 SET-UP PROCEDURE

2.2.1 Equipment Set-up Procedure

Two procedures describe set-up of the PMK01: 1) The PDP-8E/8F/8M configuration set-up procedure and 2) The PDP-11 configuration set-up procedure.

PDP-8E/8F/8M Configuration Set-Up Procedure – To connect the PMK01 to a PDP-8E/8F/8M processor:

1. Open the PMK01 carrying case and unscrew the reader plate assembly hold-down screw (Figure 1-3).

2. Raise the right edge of the reader plate assembly until it snaps into the vertical position.

3. Power down the PDP-8E/8F/8M processor to be tested.

4. Remove the Reader/Punch Control Module (M840-YA) and the interface cable (BC08K) from the right side storage compartment of the carrying case.

5. Install the interface cable Berg connector into J2 on the Reader/Punch Control Module (see Figure 1-4 to ensure proper installation).

6. Remove the PDP-8E/8F/8M processor top cover and install the Reader/Punch Control Module into sections A, B, C, and D of any vacant non-memory option slot on the OMNIBUS.

7. Install the M955 connector attached to the other end of the BC08K interface cable into slot A06 of the PMK01 wired assembly.

8. Install the PMK01 dc power cable connector P1 (W023) into any vacant power section (section A) on the OMNIBUS.

9. Plug the PMK01 ac power cord into an outlet with the correct voltage level (115 V ac for PMK01-CA, 230 V ac for PMK01-CB).

10. Apply power to the PDP-8E/8F/8M processor.

PDP-11 Configuration Set-Up Procedure – To connect the PMK01 to a PDP-11 processor:

1. Open the PMK01 carrying case and unscrew the reader plate assembly hold-down screw (Figure 1-3).

2. Raise the right edge of the reader plate assembly until it snaps into the vertical position.

3. Power down the PDP-11 processor to be tested.

4. Remove the PC11 interface module (M7810) and the interface cable (BC08J) from the right side storage compartment of the carrying case.

NOTE

Earlier model PMK01's were equipped with interface cable BC08F and three interface modules: PC11 Control (M781), Interrupt Control (M782), and Address Selector (M105). The M7810 module and cable BC08J are used in all PMK01s delivered after January 1, 1974 and are direct replacements for the aforementioned modules and cable.

5. Install the interface cable Berg connector into the Reader Connector on the PC11 interface module (see Figure 1-4 to ensure proper installation).

6. Remove the PDP-11 processor top or bottom cover (if necessary to gain access to the processor Unibus) and install the PC11 module into sections C through F of the processor small peripheral controller slot.

NOTE

If the PMK01 is equipped with Modules M781, M782, and M105, Module M781 must be installed into sections C and D of the small peripheral controller slot, Module M105 in section E, and Module M782 in section F.

7. Install the M903 connector attached to the other end of the BC08J interface cable into slot A07 of the PMK01 wired assembly.

8. Install the PMK01 dc power cable connector P1 (W023) into any vacant power section (section A) on the PDP-11 Unibus.

9. Verify that the Reader Control (M7050-YA), Reader Clock (M715-YA), and Jumper Board (W025) Modules are installed in slots 04, 05, and 06 respectively of the PMK01 wired assembly. If the M7050-YA, M715-YA, and W025 modules are not mounted in the wired assembly, they will be found in the right side storage compartment of the carrying case; remove them from the compartment and mount them in the proper slots.

10. Plug the PMK01 ac power cord into an outlet with the correct voltage level (115 Vac for PMK01-CA, 230 Vac for PMK01-CB).

2.2.2 Paper Tape Loading Procedure

To load perforated paper tape for reading: (Figure 2-1)

1. Raise the tape depressor and thread the tape under the tape hold-down bracket.

2. Place the tape on the sprocket teeth and lower the tape depressor.

3. Press the Reader Feed switch; observe the tape advances through the reader.

2.3 ACCEPTANCE TESTING

The PMK01 is shipped ready-to-use. If the unit is not operating properly, refer to the Maintenance Chapter (Chapter 5) to diagnose and correct the problem. Service should be performed by qualified service personnel only.

2.3.1 PDP-8E/8F/8M Configuration Acceptance Test Procedure

To checkout the PMK01:

1. Perform the correct PMK01 set-up procedure per Paragraph 2.2.1.

2. Verify that the RIM (Read-In-Mode) Loader program is intact in computer core memory (see Paragraph 6.2.1, Step 9). If the RIM Loader is not intact, toggle in RIM (per Paragraph 6.2.1).

3. Load the BIN (Binary) Loader program into core memory per Paragraph 6.2.2.

4. Load the high-speed Reader/Punch Test program (MAINDEC-8E-D2CA-PB) into core memory per Paragraph 6.2.3.

NOTE

If faulty operation is detected at any point in the following procedure, refer to Chapter 5 and correct the fault before proceeding to the next step.

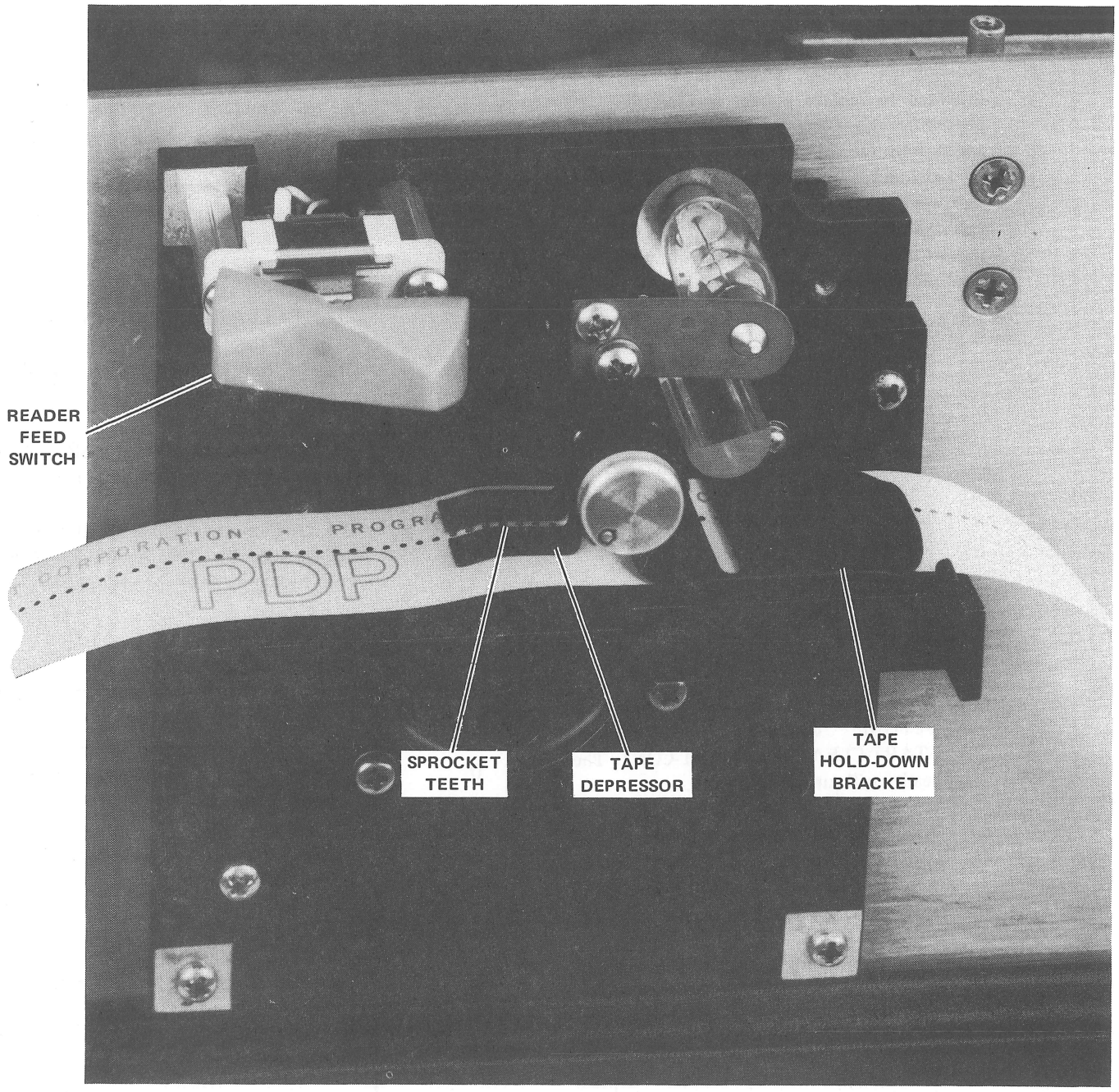


Figure 2-1 Loading Paper Tape

5. To operate the Reader Speed Print Loop (PRG13):

NOTE

PRG13 is intended to be an aid in determining reader speed. It is not intended to replace regular oscilloscope procedures to correctly set the reader speed. With the aid of a watch with sweep second hand, the reader can be timed in two ways: 1) 30 second timing is used for approximate speed settings, and 2) 300 second timing is used for accurate and final verification of reader speed.

a. Be sure that the output device (teletype or LA30 DECwriter) is on-line.

b. Load any tape into the reader station.

c. Set the SR (Switch Register) to 0200 and depress ADDR LOAD. The selected address is displayed in the MEMORY ADDRESS display.

d. Set the SR to 0013; for 30 second timing, leave SR1=0; for 300 second timing, set SR1=1.

e. When ready to start the measurement period, depress and release START-CLEAR and START-CONT. The reader will run continuously.

f. When the selected measurement period ends, set SR0 to 1 and then to 0. The output device types out the reader speed in cps. (Correct speed is 110 ± 5 cps.)

g. Observe program halts after the print-out and 4230 is displayed in MEMORY ADDRESS display.

h. To retime the reader, depress START-CONT.

NOTE

Any operator error in the measurement period length is reflected in the reader speed measurement.

6. To run the basic reader and reader control logic test (PRG0):

a. Be sure that the output device is on-line.

b. Load an all zero's tape into the reader; the tape should be spliced into a loop.

c. Set SR to 0200 and depress ADDR LOAD. The selected address should be displayed in the MEMORY ADDRESS display.

d. Set SR to 0000 and depress and release START-CLEAR and START-CONT.

e. Observe the program's halts; 0242 is displayed in the data display.

f. Set SR switches to select the SR options desired. See Table 2-1 for SR settings.

g. The program runs and halts at program end at location 0305 unless prevented from ending by errors or SR options.

Table 2-1
PRG0 SR Options

SR Switches	Option
0	Halt at Routine End; Routine number in AC register.
1	Select Routine – a number set in SR8–SR11.
2	Loop program.
3	0=halt on error; 1=do *not* halt on error.
4	Skip test after error.
8–11	Routine number to be selected.

7. To run the special binary count pattern reader test (PRG2):

a. Be sure that the output device is on-line.

b. Load Special Binary Count tape (MAINDEC-00-D2G4-PT) into reader station; the tape should be spliced into a loop at any point where the count matches so that it is continuous.

c. Set SR to 0200 and depress ADDR LOAD. The selected address should be displayed in the MEMORY ADDRESS display.

d. Set the SR to 0002. Depress and release START-CLEAR and START-CONT.

e. The program runs continuously unless errors occur. Set SR switches for the desired SR option (see Table 2-2 for PRG2 SR Options).

Table 2-2
PRG2 SR Options

SR Switches	Options
3	0=Halt on error; 1=No halt on error
6	0=Stall (Random); 1=Run full speed
7	0=Lock in current stall

2.3.2 PDP-11 Configuration Acceptance Test Procedure

To check out the PMK01:

NOTE

If faulty operation is detected at any point in the following procedure, refer to Chapter 5 and correct the fault before proceeding to the next step.

1. Perform the correct PMK01 set-up procedure per Paragraph 2.2.1.

2. Verify that the Bootstrap Loader program is intact in computer core memory (Paragraph 6.3.1, Step 12). If the Bootstrap Loader program is not intact, toggle in the Bootstrap per Paragraph 6.3.1.

3. Load the Absolute Loader program into core memory per Paragraph 6.3.2.

4. Load the PC11 Reader and Punch Tests program (MAINDEC-11-D2PCA-C-PB) into core memory per Paragraph 6.3.3.

5. To run the reader speed print routine (PRG12):

NOTE

PRG12 is intended as an aid in determining reader speed. It is not intended to replace regular oscilloscope procedures to correctly set the reader speed. With the aid of a watch with a sweep second hand, the reader can be timed in two ways: 1) 30 second measurement period (plus or minus 10 cps accuracy), and 2) 300 second measurement period (plus or minus 1 cps accuracy).

a. Be sure that the output device (teletype or LA30 DECwriter) is on-line.

b. Load any tape into the reader station.

c. Set the SR to 000200 and depress LOAD ADRS. The selected address is displayed in the ADDRESS display.

d. Set the SR to 000012 and depress START. The program identifies itself and types out instructions to load the reader and make it ready, and to select the desired measurement period. (SR14=0 selects 30 second measurement period; SR14=1 selects 300 second measurement period).

e. When ready to start the measurement period, depress CONT. The reader starts running.

f. At end of measurement period, set SR15 to 1 and to 0. The output device types out the reader speed in cps. (Correct speed is 110 ± 5 cps.)

g. To repeat measurement, repeat steps e and f.

NOTE

Any operator error in the measurement period length is reflected in the reader speed measurement.

6. To run the reader logic tests (PRG0):

   a. Be sure that the output device is on-line.

   b. Load the Special Binary Count tape (MAINDEC-00-D2G4-PT) into reader.

   c. Set the SR to 00200 and depress LOAD ADRS. The selected address is displayed in the ADDRESS display.

   d. Set SR to 00000 and depress START. The program identifies itself and types out instructions to set any desired SR options (See Table 2-3 for PRG0 SR options).

   e. Set SR8 to 1 and depress CONT.

   f. If no errors occur, the program rings the bell and types out "*" at the end of each pass. If errors do occur, refer to Paragraph 6.2 of the MAINDEC-11-DZPCA-C-D program identification document which is provided with the PMK01.

7. To run the reader test (PRG1):

   a. Be sure that the output device is on-line.

   b. Load Special Binary Count tape loop into reader.

NOTE

A test loop must be used because a normal length test tape is not long enough to conduct the test. If a tape loop is not used, data must be positioned over the photo transistor, i.e., the leader cannot be used.

   c. Set the SR to 00200 and depress LOAD ADRS. The selected address is displayed in the ADDRESS display.

   d. Set the SR to 000001 and depress START. The program identifies itself and types instructions to set any desired SR options (See Table 2-3 for PRG1 SR options).

   e. Depress CONT.

   f. If no errors occur, the program rings the bell and types out "*" at the end of each pass. If errors do occur, refer to Paragraph 6.2 of the MAINDEC-11-DZPCA-C-D program identification document which is provided with the PMK01.

Table 2-3
PRG0 and PRG1 SR Options

SR Switches	Options
15	1=Halt on ERROR
14	1=Enter scope mode
13	1=Inhibit error print
11	1=Inhibit iteration
10	1=Halt at end of current test
9	1=Select a specific routing for execution
8*	1=Bypass manual intervention routine
6–0	Number of routine to be selected

*SR8 applies only to PRG0.

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 OPERATION

The Reader Feed switch, located on the front of the reader plate assembly, is the only manual control on the PMK01. It advances the paper through the reader when depressed.

NOTE

The feed switch advances the tape but it does not perform a complete data read operation, i.e., the read data is not transferred to the computer. Data can only be transferred to the computer by the program.

READER FETCH CHARACTER	
Mnemonic Octal Code Operation	RFC 6014 Fetches a character from the tape; clears the reader flag, loads one character into the reader buffer from the tape, and sets the reader flag when reader buffer loading is complete.

READ BUFFER AND FETCH NEW CHARACTER	
Mnemonic Octal Code Operation	RRB, RFC 6016 Micro-instruction of 6012 and 6014. The contents of the reader buffer is ORed into the accumulator register, the reader flag is cleared, a new character is loaded into the reader buffer from the tape, and the reader flag is set.

CLEAR INTERRUPT ENABLE	
Mnemonic Octal Code Operation	PCE 6020 Clears interrupt enable flip-flop so interrupt request can not be generated.

3.2 PROGRAMMING

There are distinct differences between the control methods used by the PDP-8E/8F/8M and the PDP-11 processors. The PDP-8E/8F/8M processors use a total of six IOT (Input/Output Transfer) instructions to read and advance the paper tape. The PDP-11 processors only use two device registers which may be serviced by instructions referencing their addresses.

3.2.1 PDP-8E/8F/8M Programming Information

3.2.1.1 IOT Instructions – Reader operation is controlled by the following IOT instructions:

SET INTERRUPT ENABLE	
Mnemonic Octal Code Operation	RPE 6010 Sets the interrupt enable flip-flop so an interrupt request can be generated when the reader flag is set (the reader is logically connected to the processor interrupt system).

SKIP ON READER FLAG	
Mnemonic Octal Code Operation	RSF 6011 Senses the reader flag; if the flag is set, the program counter is incremented by one so the next sequential instruction is skipped.

READ READER BUFFER	
Mnemonic Octal Code Operation	RRB 6012 Reads the reader buffer; causes the contents of the reader buffer to be ORed into the accumulator register and clears the reader flag.

3.2.1.2 **Program Example** – A typical program to read and store characters from a paper tape can be written as follows:

```
START   CLA         ; Clear ac
        RFC         ; Fetch character from tape and
                    ; set reader flag
LOOK    RSF         ; Skip if reader flag = 1
        JMP LOOK    ; Jump back and test flag again
        RRB         ; Load ac from reader buffer,
                    ; clear reader flag
        DCA         ; Store data
        JMP START   ; Return and repeat
```

3.2.1.3 **PMK01 Programs** – The following programs must be used when there is no TTY bell to ring. All these programs are contained in LIBKIT-8E-PMK1-01.

INSTRUCTION TEST 1
MAINDEC-8E-D9AA-D (write-up)
MAINDEC-8E-D9AA-PB (Binary Tape)

INSTRUCTION TEST 2
MAINDEC-8E-D9BA-D
MAINDEC-8E-D9BA-PB

8E ADDER TESTS
MAINDEC-8E-D9CA-D
MAINDEC-8E-D9CA-PB

RANDOM AND TEST
MAINDEC-8E-D9DA-D
MAINDEC-8E-D9DA-PB

RANDOM TAD TEST
MAINDEC-8E-D9EA-D
MAINDEC-8E-D9EA-PB

RANDOM ISZ TEST
MAINDEC-8E-D9FA-D
MAINDEC-8E-D9FA-PB

RANDOM DCA TEST
MAINDEC-8E-D9GA-D
MAINDEC-8E-D9GA-PB

RANDOM JMP TEST
MAINDEC-8E-D9HA-D
MAINDEC-8E-D9HA-PB

BASIC JMP-JMS TEST
MAINDEC-8E-D9IA-D
MAINDEC-8E-D9IA-PB

RANDOM JMP-JMS TEST
MAINDEC-8E-D9JA-D
MAINDEC-8E-D9JA-PB

MEMORY ADDRESS TEST
MAINDEC-8E-D9KA-D
MAINDEC-8E-D9KA-PB

MM8-E 4K MEMORY CHECKERBOARD
MAINDEC-8E-D9LA-D
MAINDEC-8E-D9LA-PB

KP8E POWER FAIL TEST
MAINDEC-8E-D9MA-D
MAINDEC-8E-D9MA-PB

MEMORY POWER ON/OFF TEST
MAINDEC-8E-D9NA-D
MAINDEC-8E-D9NA-PB

JMP SELF TEST
MAINDEC-8E-D9PA-D
MAINDEC-8E-D9PA-PB

3.2.2 PDP-11 Programming Information

3.2.2.1 **Device Registers** – The PDP-11 processors control the paper-tape reader with two device registers. These registers have been assigned bus addresses and can be read or loaded (with the exceptions noted) using any PDP-11 instruction referring to their addresses.

The following figures and tables describe the content of each register. The mnemonic INIT is used frequently in the following tables and refers to the initialization signal generated by the processor. The processor will issue an INIT signal when:

- a programmed RESET instruction is processed.
- the processor START switch is depressed.
- the power fail sequence occurs.

During a power fail sequence, INIT is asserted when power is going down and again when power is coming up.

PAPER TAPE READER STATUS REGISTER

Mnemonic	PRS
Address	777550
Bit Assignment	Figure 3-1
Bit Description	Table 3-1

Table 3-1
Paper-Tape Reader Status Register
Bit Description

Bit	Name	Description
15	ERROR	Set when one of the following conditions occurs: a. reader out of tape b. no power to reader c. reader off-line* If bit 06 of this register is set, setting this bit initiates an interrupt sequence. Read-only bit.
11	BUSY	Sets when the reader is performing a read operation. This bit sets when RDR ENB (reader enable) is set and clears when DONE is set. Read-only bit.
07	DONE	Sets when a character is available in the reader data buffer. If bit 06 of this register is set, setting this bit initiates an interrupt sequence. Read-only bit; cleared by INIT, by setting the RDR ENB bit or by reading the paper-tape reader buffer register.
06	Reader Interrupt Enable (RDR INTR ENB)	When set allows an interrupt sequence to be initiated by setting the DONE or ERROR bits. Read/Write bit; cleared by INIT.
00	Reader Enable (RDR ENB)	When set, this bit initiates a read cycle, sets the BUSY bit, and clears the DONE bit. Write-only bit.

*This condition does not occur in the PMK01 since there is no reader ON/OFF switch.

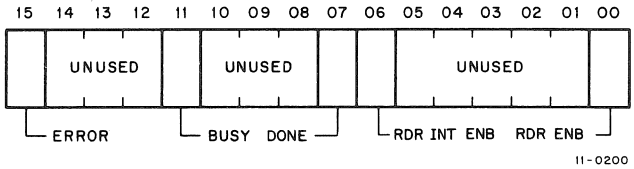


Figure 3-1 Paper-Tape Reader Status Register Bit Assignment

PAPER-TAPE READER BUFFER REGISTER

Mnemonic PRB
Address 777552
Bit Assignment Figure 3-2
Bit Description Table 3-2

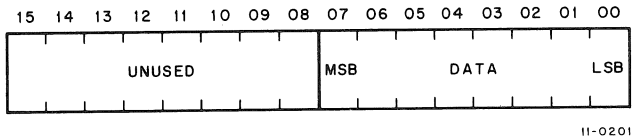


Figure 3-2 Reader Buffer Register Bit Assignments

Table 3-2
Reader Buffer Register
Bit Description

Bit	Name	Description
07–00	DATA (07:00)	This register holds the read character for reading by the program.

3.2.2.2 **Program Example** – The program listed on the following page reads one byte from the paper tape and deposits it in general register 0. If a reader error is sensed, the program branches to an error routine which types out a message and waits for operator intervention.

NOTE

Because the RDR ENB bit is bit 00 in PRS register, the INC instruction can be used to set it.

```
READ:   INC     PRS     ; SET RDR ENB
LOOP:   TST     PRS     ; LOOK FOR ERROR
        BMI     ERR     ; BRANCH ON ERROR=1
        TSTB    PRS     ; LOOK FOR DONE
        BPL     LOOP    ; WAIT IF DONE=0
        MOV     PRB, R0 ; READ CHARACTER
        HALT            ; STOP
ERR:    (type out message)
        HALT            ; WAIT FOR OPERATOR INTERVENTION
        JMP READ        ; TRY AGAIN WHEN CONTINUE IS HIT
```

3.2.3 Reader Timing Considerations

Reader operating speed is dependent on the frequency of read commands received from the computer. If the frequency of the read commands is such that each successive read command occurs within 6.81 ms after a character is loaded into the reader buffer, the reader will maintain a continuous operating speed of 110 cps (characters/second). If the read command frequency is such that each successive read command exceeds the 6.81 ms time limit, the tape advance circuitry is inhibited for at least 40 ms to allow the reader motor to come to a complete stop after each character read operation. The maximum possible start/stop operating speed is 21 cps.

The reader clock directly controls the reader operating speed. In response to read commands, the reader clock produces pulses that:

- strobe the data into the reader buffer,
- set the reader flag when data transfer into the buffer is complete, and
- control the reader motor.

The inertial characteristics of the reader motor and the tape advance wheel account for the large difference between the continuous reader operating speed and the start/stop operating speed. Time must be allowed for the motor to accelerate from rest to the proper operating speed. And then to decelerate from operating speed to rest. To allow acceleration time, an accelerator circuit, integral to the reader clock, extends the first few clock periods at the beginning of a continuous read operation. To allow deceleration time, a time-out circuit integral to the reader control logic inhibits the tape advance circuitry for at least 40 ms whenever the continuous operation time limit is exceeded. Therefore, operating the reader in a start/stop fashion greatly reduces the operating speed.

3.3 PAPER-TAPE FORMAT

For paper-tape format, refer to Figure 3-3.

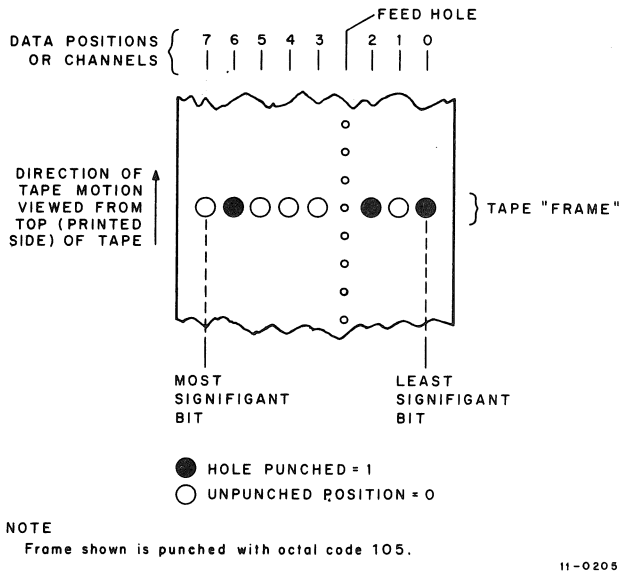


Figure 3-3 Paper-Tape Format

CHAPTER 4
THEORY OF OPERATION

4.1 SCOPE

This chapter provides a detailed description of the PMK01 which covers both the PDP-8E/8F/8M and PDP-11 configurations and is divided into two parts: a functional description and a detail logic level description.

4.2 FUNCTIONAL DESCRIPTION

The PMK01 is a portable paper-tape reader used to load diagnostic programs into either PDP-8E/8F/8M or PDP-11 computers.

4.2.1 Basic Operation

4.2.1.1 PDP-8E/8F/8M Configuration – The PDP-8E/8F/8M version of the PMK01 will only perform paper-tape read operations when directed by the program via IOT instructions. Before the PMK01 can process instructions it must be initialized via the INIT signal. Initializing the PMK01 clears all the control flip-flops in the reader/punch control except the INT ENA (interrupt enable) flip-flop which it set. Once it is initialized, the PMK01 simply awaits IOT instructions from the processor. Figure 4-1 is a flow diagram explanation of PMK01 basic operation when interfaced with PDP-8E/8F/8M processors.

4.2.1.2 PDP-11 Configuration – The PDP-11 version of the PMK01 will only perform paper-tape read operations when directed by the program via instructions referencing the two device registers:

1. the PRS (reader status register) and
2. the PRB (paper-tape reader buffer register).

Before the device registers can be addressed, the PMK01 must be initialized via the INIT signal. Initializing the PMK01 clears all control flip-flops in the PC11 interface and Reader Control Modules. Once initialized, the PMK01 simply awaits register instructions from the processor. Figure 4-2 is a flow diagram explanation of PMK01 basic operation when interfaced with PDP-11 processors.

4.2.2 PDP-8E/8F/8M Configuration Functional Block Diagram Description

Physically this configuration consists of two separate units (Figure 4-3): 1) the Reader/Punch Control Module which mounts in the OMNIBUS and 2) the paper-tape reader which is housed in the carrying case.

4.2.2.1 Reader/Punch Control – The reader/punch control performs all the functions necessary to interface the paper-tape reader to the PDP-8E/8F/8M processor. The control decodes IOT instructions generated by the processor and generates data handling and reader motor control signals.

Functionally the reader/punch control can be divided into seven logic sections; each section performing a specific function in accomplishing the overall task of data handling and control (Figure 4-3). The following paragraphs describe the specific function of each logic section.

Device Select and IOT Decoder Logic – The device select and IOT decoder logic detects and decodes IOT instructions generated by the processor and generates the gating and strobe signals necessary to perform the operation decoded. Upon detecting an IOT instruction (MD03–11), the logic decodes the instruction and generates signals necessary to perform one or more of the following operations:

- Loads data into the reader buffer (RDR IOP 4)
- Gates data onto the OMNIBUS (RDR DATA TO OMNIBUS)
- Clears the reader flag (RDR IOP 2/RDR IOP 4)
- Sets or resets the INT ENA flip-flop (SET/RESET INT ENA F/F)
- Gates the Skip flag onto the OMNIBUS (RDR IOP 1)

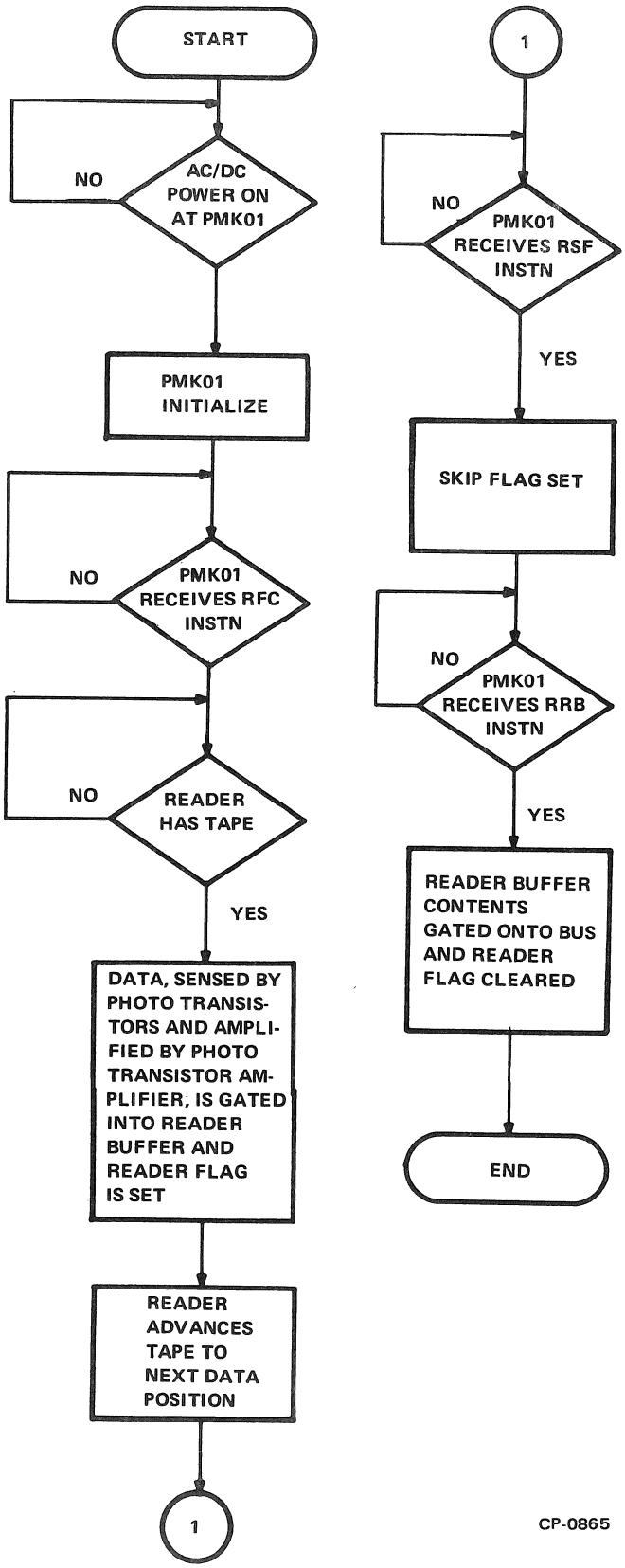


Figure 4-1 PMK01 Basic Operation Flow Diagram
(PDP-8E/8F/8M Configuration)

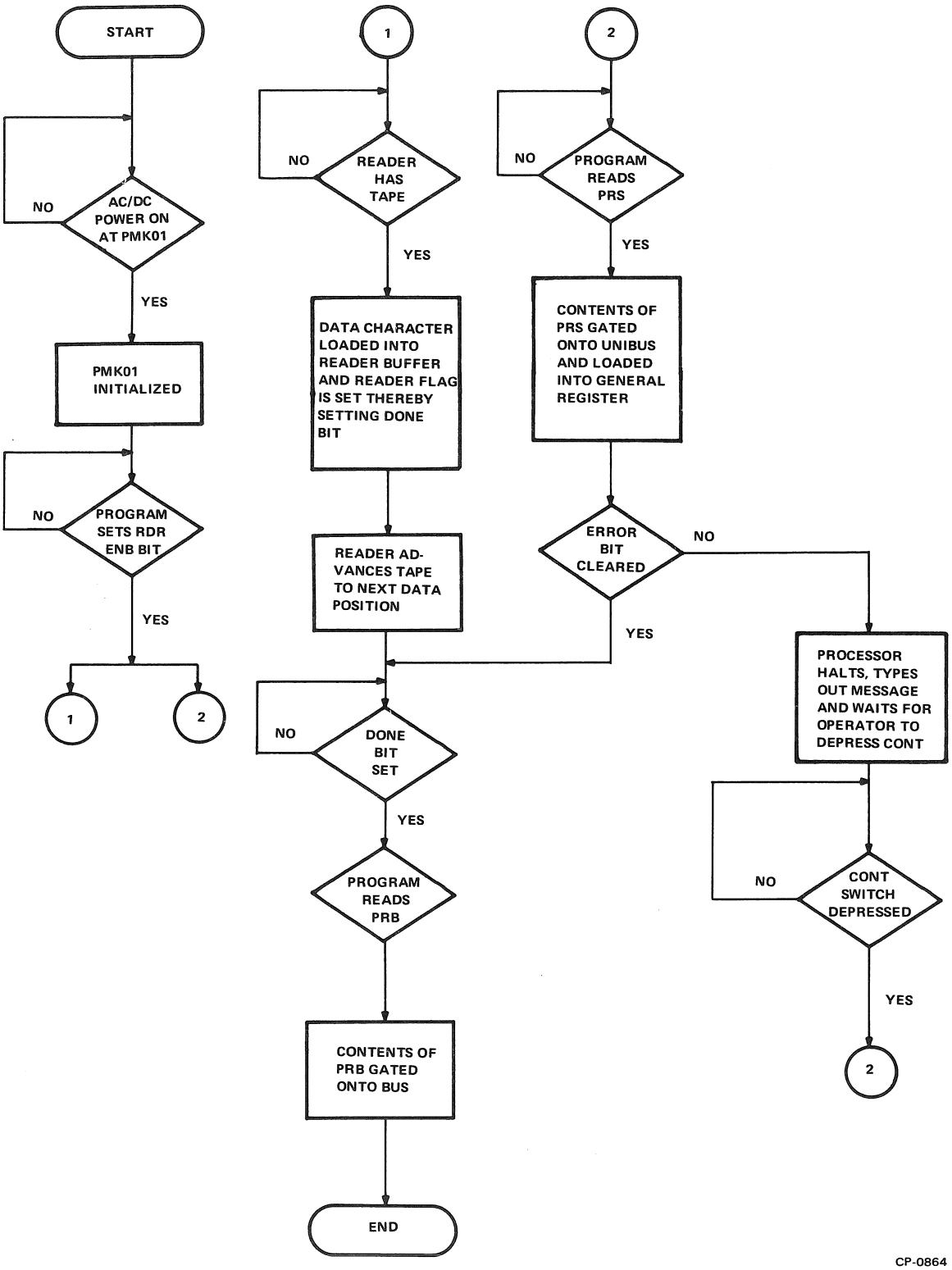


Figure 4-2 PMK01 Basic Operation Flow Diagram
(PDP-11 Configuration)

The two remaining signals perform specific interface functions. The I/O PAUSE input merely serves to gate the IOT instructions to the reader/punch control. The INTERNAL I/O output asserts a ground on the bus when a Reader/Punch IOT instruction is decoded so that the positive I/O BUS interface cannot generate IOPs.

Reader Control Logic – The reader control logic controls the tape read operation. In response to a load reader buffer strobe (RDR IOP 4) from the Device select and IOT decoder logic, the reader control logic enables the reader motor control logic, the clock logic, and the tape status logic, and asserts the RDR COMMANDED TO RUN line to the interrupt logic. When the clock logic outputs the first clock pulse, assuming the FEED HOLE line is asserted, the reader control logic asserts the RDR DATA STROBE line which loads the read data into the reader buffer register and sets the reader flag at the interrupt control logic.

The reader control logic also monitors other inputs from the reader motor control logic, the clock logic and the tape status logic. If the RDR MOTOR IS STOPPING line or the CLOCK PULSE line is asserted when the RDR IOP 4 input asserts, the ENABLE output is inhibited until the motor stopping and clock lines are cleared. The inputs from the reader motor control logic [A (0), B (0) and $\overline{A} \cdot \overline{B}$] indicate the status of the motor stepping logic. Using these inputs and the FEED HOLE PRESENT input from the tape status logic, the reader control logic restricts the generation of RDR DATA STROBE to the periods in time that the tape data holes are over the photo transistor and keeps the ENABLE line asserted long enough to permit the reader motor logic to advance the tape to the next data position. The OUT OF TAPE line from the tape status logic indicates the presence or absence of tape in the reader. If OUT OF TAPE is true, the RDR COMMANDED TO RUN output is inhibited thereby preventing the interrupt control logic from generating a SKIP or INT RQST flag. If neither of these flags can be asserted, data cannot be transferred to the OMNIBUS.

When the Reader Feed switch is depressed, the reader control logic asserts the ENABLE line, RDR DATA STROBE loads the Reader Buffer and the tape is advanced. However, the Reader Feed switch does *not* assert the RDR DATA to OMNIBUS line; therefore the data is not transferred to the OMNIBUS.

Clock Logic – The clock logic provides the timing for the reader/punch control. When enabled, the clock logic outputs clock pulses (which are used by the reader control logic and the interrupt control logic) and shift pulses (which step the reader motor control logic). To compensate for the inertia of the reader motor and drive wheel, the clock is equipped with an accelerator circuit which initially slows the clock pulse rate to allow the motor to reach operating speed.

Reader Motor Control Logic – The reader motor control logic controls the solenoid drivers which step the reader motor, and notifies the reader control logic of motor stepping status. To step the reader motor, two drivers must be enabled, and to advance the tape from one data character position to the next, the motor must be stepped four times. The reader motor control logic accomplishes this stepping by sequentially enabling the drivers in four different combinations. To advance the tape continuously (full speed) from character to character, the driver combinations are merely repeated over and over. When the reader control logic determines that tape advancement should be terminated, the ENABLE line is cleared and the motor control logic stops the tape at the next data position.

The reader motor control logic is also equipped with a motor stopping time-out circuit. This circuit allows the reader motor to come to a complete stop whenever the ENABLE line is cleared. When the ENABLE line clears, the time-out circuit activates and asserts RDR MOTOR IS STOPPING. The assertion of RDR MOTOR IS STOPPING inhibits program controlled tape reading and advancing operations until the 40 ms time-out period is completed.

The status outputs to the reader control logic [$\overline{A} \cdot \overline{B}$, A (0) and B (0)] indicate the position of the reader motor relative to the tape data position. The effect of these signals on the reader control logic was discussed previously.

Tape Status Logic – The tape status logic monitors ENABLE and the FEED HOLE signal from the photo transistor amplifier and controls the HAVE TAPE, OUT OF TAPE, and FEED HOLE PRESENT lines accordingly. With the motor stopped and the tape data holes and feed hole over the photo transistor, the FEED HOLE input is asserted and the HAVE TAPE and FEED HOLE PRESENT outputs are asserted. When the processor generates an RFC (Reader Fetch Character) instruction, the ENABLE input is asserted and the FEED HOLE input clears as the tape is advanced. Clearing the FEED HOLE input clears the FEED HOLE PRESENT output; however, the HAVE TAPE line remains asserted. If no more RFC instructions are generated, the tape is advanced to the next data position and stopped. The data is strobed into the reader buffer register before the tape is advanced; therefore clearing FEED HOLE PRESENT is of no consequence. If the tape runs out while being advanced, the FEED HOLE input is asserted (there is no tape to block the light) causing the OUT OF TAPE

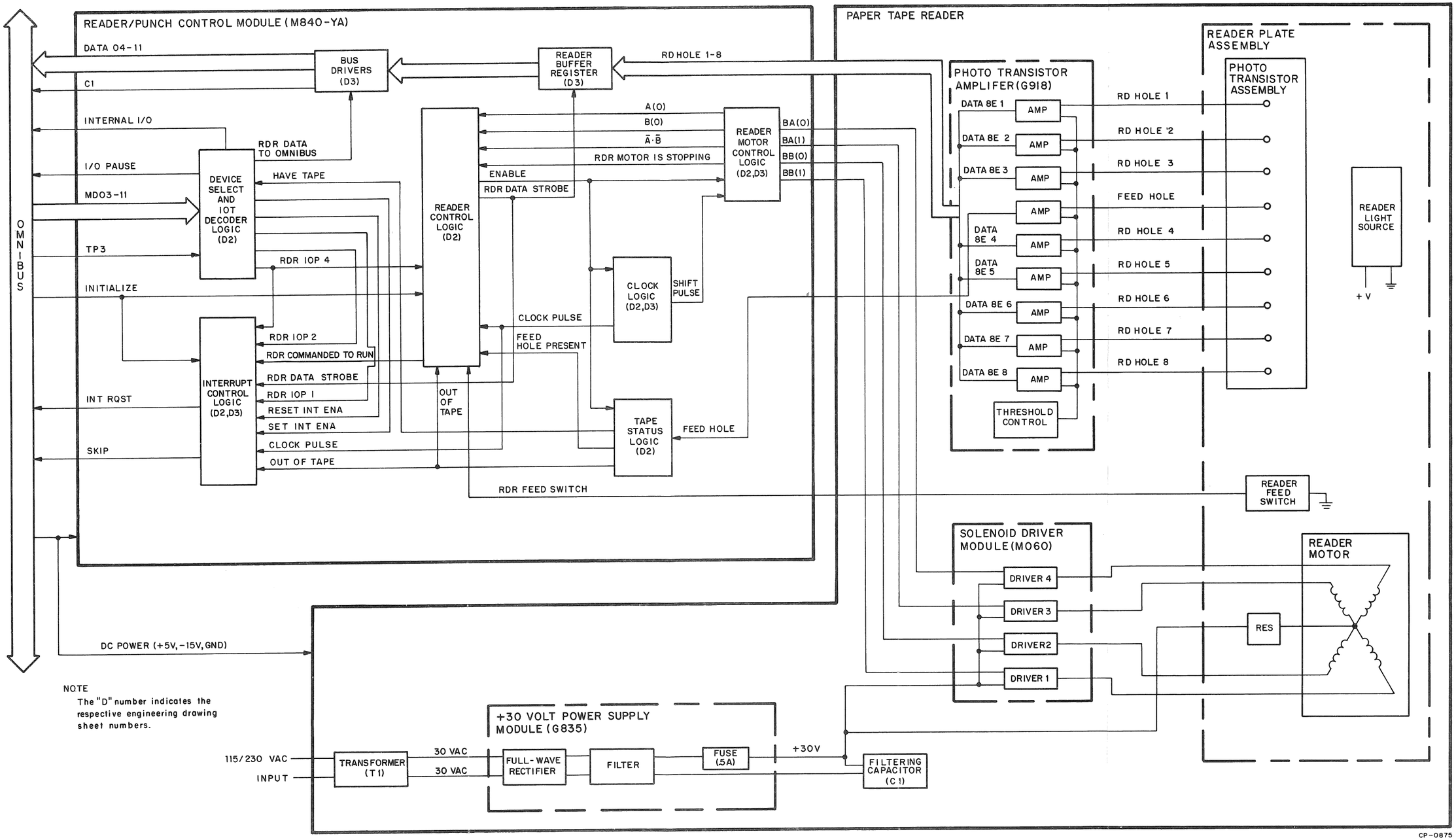


Figure 4-3 PDP-8E/8F/8M Configuration Functional Block Diagram

output to assert and the HAVE TAPE output to clear. With the HAVE TAPE line cleared, the RDR IOP 4 output from the device select and IOT decoder logic are inhibited, preventing any subsequent processor generated RFC instructions from being processed. If the reader is then reloaded with paper tape, OUT OF TAPE is cleared by the transition of the FEED HOLE line and HAVE TAPE asserts, allowing RFC instructions to be processed.

Reader Buffer Register and Bus Driver – When the processor generates an RFC instruction, the reader control logic asserts RDR DATA STROBE and the outputs from the photo transistor amplifier are loaded into the reader buffer register. The processor then generates an RRB (Read Reader Buffer) instruction causing the device select and IOT decoder logic to assert RDR DATA TO OMNIBUS. RDR DATA TO OMNIBUS enables the bus drivers placing the data onto the OMNIBUS and asserts the C1 line which enables the processor to load the data into the accumulator register.

Interrupt Control Logic – The interrupt control logic monitors outputs from the device select and IOT decoder logic, the reader control logic, and the tape status logic, and issues INT RQST and SKIP flags to the OMNIBUS accordingly. If the OUT OF TAPE line is asserted, both flags are inhibited.

4.2.2.2 **Paper-Tape Reader** – The paper-tape reader detects the data stored on the paper tape, outputs that data to the reader/punch control for reading and in response to motor control signals advances the paper tape to the next data position.

Functionally, the paper-tape reader can be divided into four sections, each section performing specifically in reading and advancing the tape:

1. The reader plate assembly consists of a tape advance motor, a Reader Feed switch to allow the tape to be advanced manually, and a light source and phototransistor assembly which detect the absence or presence of feed and data holes in the paper tape.

2. The photo transistor amplifier detects the feed and data holes signals from the phototransistor assembly, amplifies those signals, and outputs them to the reader/punch control.

3. The solenoid drivers enable current flow through the motor field windings in response to inputs from the reader/punch control. The drivers are selected two at a time in four different combinations in sequential order such that the motor always rotates in the same direction. When a new driver combination is selected, current flow results in the motor field winding causing the motor to rotate until the field winding current is reduced to zero. All four driver combinations must be selected to advance the tape from one data position to the next.

4. The +30 V power supply rectifies and filters the 30 Vac input from the step-down transformer and outputs +30 Vdc to drive the reader motor.

4.2.3 PDP-11 Configuration Functional Block Diagram Description

Physically, this configuration consists of two separate units (Figure 4-4): 1) the PC11 Interface Module which mounts in the Unibus and 2) the paper-tape reader which is housed in the carrying case.

4.2.3.1 **PC11 Interface** – The PC11 interface performs all the functions necessary to interface the paper-tape reader to a PDP-11 processor. The interface decodes register instructions generated by the processor and generates data handling and Reader Control Module control signals. Functionally, the PC11 interface can be divided into six logic sections, each section performing a specific task to accomplish the overall task of data handling and control.

Address Selection and Mode Control Logic – The address selection and mode control logic decodes the A (address) and C (control) bits placed on the Unibus and generates the gating and strobe signals necessary to perform the operation decoded. Upon detecting a register instruction the logic generates the signals necessary to perform one of the following operations:

- Load the PRS (LOAD PRS).
- Assert PRB read control signals to the Reader Control Module (IOP 2 and QUALIFY) and gate PRB data onto the Unibus (READ PRB).
- Gate PRS data onto the Unibus (READ RRS).

The BUS MSYN (MASTER SYNC) input is asserted by the processor whenever a Unibus device is addressed. The BUS SSYN (SLAVE SYNC) output to the Unibus is raised to signify the completion of transfer.

Paper-Tape Reader Status Register (PRS) – The PRS stores reader control data and monitors the I/O BUS INT (DONE), RDR RUN (BUSY), and OUTAPE (ERROR) inputs from the Reader Control Module.

Reader Data and Reader Status Bus Driver – The bus drivers serve to assert the register content data lines onto the Unibus. If a read PRS instruction is decoded, the reader status bus drivers are enabled by the assertion of READ PRS. If a read PRB instruction is decoded, the reader data bus drivers are enabled by the assertion of READ PRB.

Interrupt Control Logic – The interrupt control logic enables the PC11 interface to gain control of the Unibus (become bus master) and causes a program interrupt to an interrupt address vector.

Interrupts are enabled or disabled via the program. Setting the RDR INT ENB bit in the PRS enables the interrupt logic. With the RDR INT ENB bit set, the assertion of INT A initiates an interrupt sequence. The bus is requested (BUS BR REQ), granted (BUS BG IN), and acknowledged (BUS SACK); the interrupt is identified (BUS INTR and VECTOR ADDRESS) and acknowledged (BUS SSYN) and the processor then branches to the subroutine identified by the vector address and services the interrupt.

The BG OUT (BUS GRANT OUT) line propagates the BG IN to the Unibus whenever the PC11 is not requesting the bus. This, in effect, accomplishes the daisy chaining of BG IN to all devices on the same BR level.

4.2.3.2 **Paper-Tape Reader** – Functionally, the only difference between the PDP-11 paper-tape reader and the previously discussed PDP-8E/8F/8M paper-tape reader is the addition of the reader control and clock logic. The functions performed by these logics are identical to the functions performed by the Reader/Punch Control Module (M840-YA) previously discussed.

4.3 DETAILED LOGIC DESCRIPTION

4.3.1 PDP-8E/8F/8M Configuration

The following paragraphs provide detailed logic level descriptions of the functional blocks shown in Figure 4-3 and listed below:

- Device Select and IOT Decoder Logic
- Reader Control Logic
- Clock Logic
- Reader Motor Control Logic
- Tape Status Logic
- Reader Buffer Register and Bus Drivers
- Interrupt Control Logic
- Phototransistor Assembly
- Photo Transistor Amplifier
- Tape Advance Circuit

4.3.1.1 **Device Select and IOT Decoder Logic** – The device select and IOT decoder logic detects and decodes IOT instructions generated by the processor and generates the gating and strobe signals necessary to perform the operation decoded (Figure 4-5 and engineering drawing E-CS-M840-YA-1, sheet 2). When I/O PAUSE L asserts, memory data bits MD (3–8) L are gated to the input AND gates. If AND gate A or B is satisfied, the reader/punch device is selected, the respective decoder is enabled, bits MD (09–11) L are gated to the decoder, and INTERNAL I/O L is asserted on the bus. The binary to decimal decoder then decodes bits MD (09–11) L and asserts the proper output. If, for example, an RFC instruction is issued by the processor, the 6014 (RFC) L line is asserted and at TP3 H (timing pulse), RDR IOP 4 L asserts provided HAVE TAPE H is asserted. When the RRB, RFC instruction is decoded, strobes are generated to read the buffer register (RDR DATA TO OMNIBUS H) and load the reader buffer register (RDR IOP 4 L).

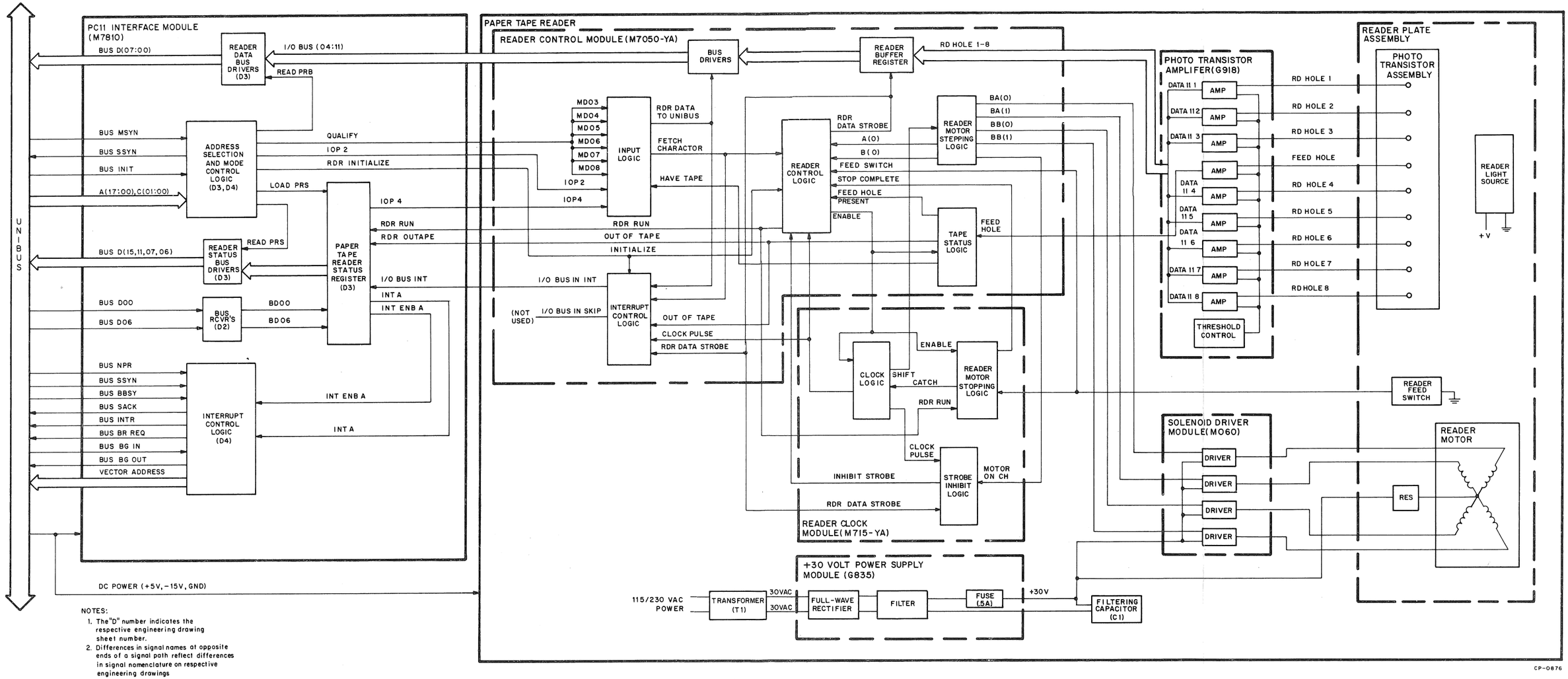


Figure 4-4 PDP-11 Configuration Functional Block Diagram

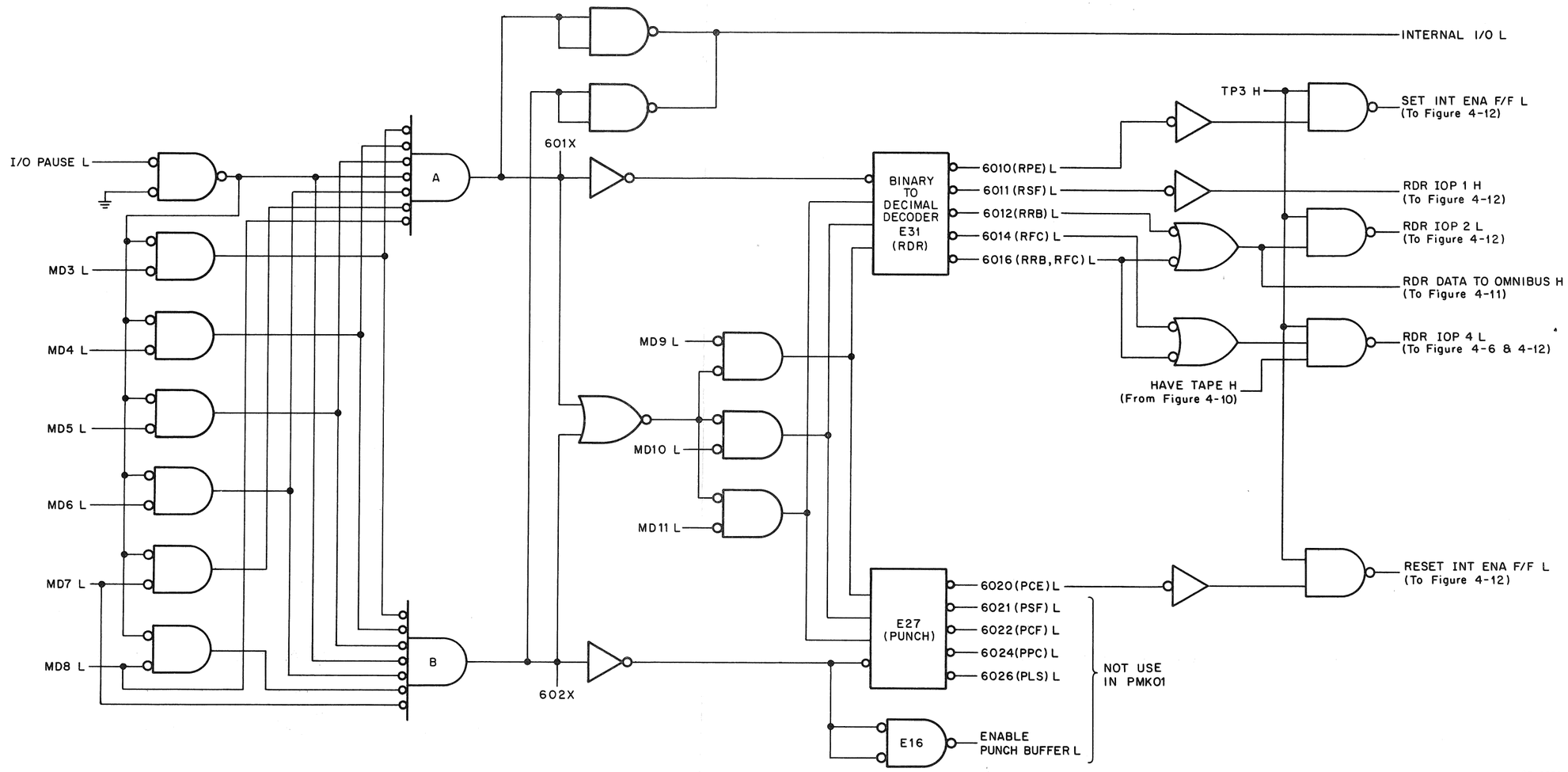


Figure 4-5 Device Select and IOT Decoder Logic

NOTE

TP3 H is generated by the processor timing generator as a positive going 100 ns pulse.

4.3.1.2 **Reader Control Logic** – The reader control logic controls the tape read operation (Figure 4-6 and engineering drawing E-CS-M840-YA-1, sheet 2). When RDR IOP 4 L is asserted, the RDR RUN flip-flop sets and asserts RDR COMMANDED TO RUN H. If the motor stop cycle is complete and CLOCK PULSE L is clear, the RDR ENABLE flip-flop is also set asserting ENABLE (1) H and ENABLE (1) L. ENABLE (1) H starts the clock and CLOCK PULSE H asserts. When the data and feed holes are positioned over the phototransistor assembly, $(\overline{A} \cdot \overline{B})$ L is true. Hence CLOCK PULSE H sets the R/S flip-flop satisfying AND gate E23 and, after a short delay, RDR DATA STROBE H asserts, clearing the RDR RUN flip-flop and loading the Reader Buffer. When RDR DATA STROBE asserts, the 150 ns clock pulse has cleared, hence the R/S flip-flop is reset immediately and, after a short delay, RDR DATA STROBE H is cleared.

The reader motor then advances the tape and $(\overline{A} \cdot \overline{B})$ L, A (0) L and FEED HOLE PRESENT H are cleared while B (0) L remains asserted; thus, the RDR data strobe logic is disabled. When the next clock pulse occurs the RDR ENABLE flip-flop remains set, holding the clock on and the reader motor continues to advance the tape clearing the B (0) L input. When the next clock pulse occurs, the RDR ENABLE flip-flop is cleared disabling the clock. The final pulse to complete the advancement of the motor to the next data position is generated within the reader motor control logic.

The remaining inputs to the reader control logic serve to inhibit reader operations. If an OUT OF TAPE condition occurs, the RDR RUN flip-flop is reset when CLOCK PULSE H asserts clearing the RDR COMMANDED TO RUN H output. This feature prevents the reader flag from being set if there is no tape in the reader. If the reader motor is stopping (RDR MOTOR IS STOPPING L) or CLOCK PULSE L is asserted when the RDR RUN flip-flop is set, the RDR ENABLE flip-flop will not set until both inputs are cleared. This prevents a new character read operation from starting before the 40 ms motor stopping time-out period is completed.

4.3.1.3 **Clock Logic** – The clock logic provides the timing pulses for the reader/punch control (Figure 4-7 and engineering drawing E-CS-M840-YA-1, sheets 2 and 3). The logic consists of a ramp generator, a triggered free-running multivibrator, and two pulse forming networks.

During continuous operation, the reader motor is stepped once every 2.27 ms. However, when the motor is started from a dead stop, the inertia of the motor and the tape drive wheel must be overcome; hence, the tape moves over the photo transistors more slowly than at continuous operating speed and a ramp generator must be used to maintain a nearly constant ratio of tape speed to CLOCK PULSE frequency. The ramp generator consists of transistors Q1 and Q2.

When ENABLE (1) H is asserted by the tape read logic, the ramp generator is triggered and the free-running multivibrator, Q4/Q5, is triggered on via Q3. The emitter of Q2 provides the charging potential for the multivibrator. The emitter potential of Q2 rises at a rate determined by the RC time constant which can be varied by R27. As the potential rises, the capacitors in the base circuits of Q4 and Q5 take less time to charge. Thus, the on/off cycle of Q4 and Q5 decreases. Ultimately, when the ramp has ended, the CLOCK PULSE period is 2.27 ms.

The timing diagram (Figure 4-8) illustrates the operation of the pulse forming delay networks.

4.3.1.4 **Reader Motor Control Logic** – The reader motor control logic controls the solenoid drivers which in turn control the current through the reader motor field windings (Figure 4-9 and engineering drawing E-CS-M840-YA-1, sheets 2 and 3).

When the reader control logic asserts ENABLE (1) H the reader motor control logic is in its quiescent state, i.e., the one shots are cleared, flip-flops A and B are reset and outputs $(\overline{A} \cdot \overline{B})$ L, A (0) L, B (0) L, BA (1) L and BB (1) L are asserted. Therefore, asserting ENABLE (1) H has no effect on the reader motor control; however, it does turn the clock on and the clock outputs a minimum of three shift pulses. Each shift pulse asserts ROTATE PULSE H and clocks the flip-flops. (See Table 4-1 for the outputs resulting from each shift pulse.)

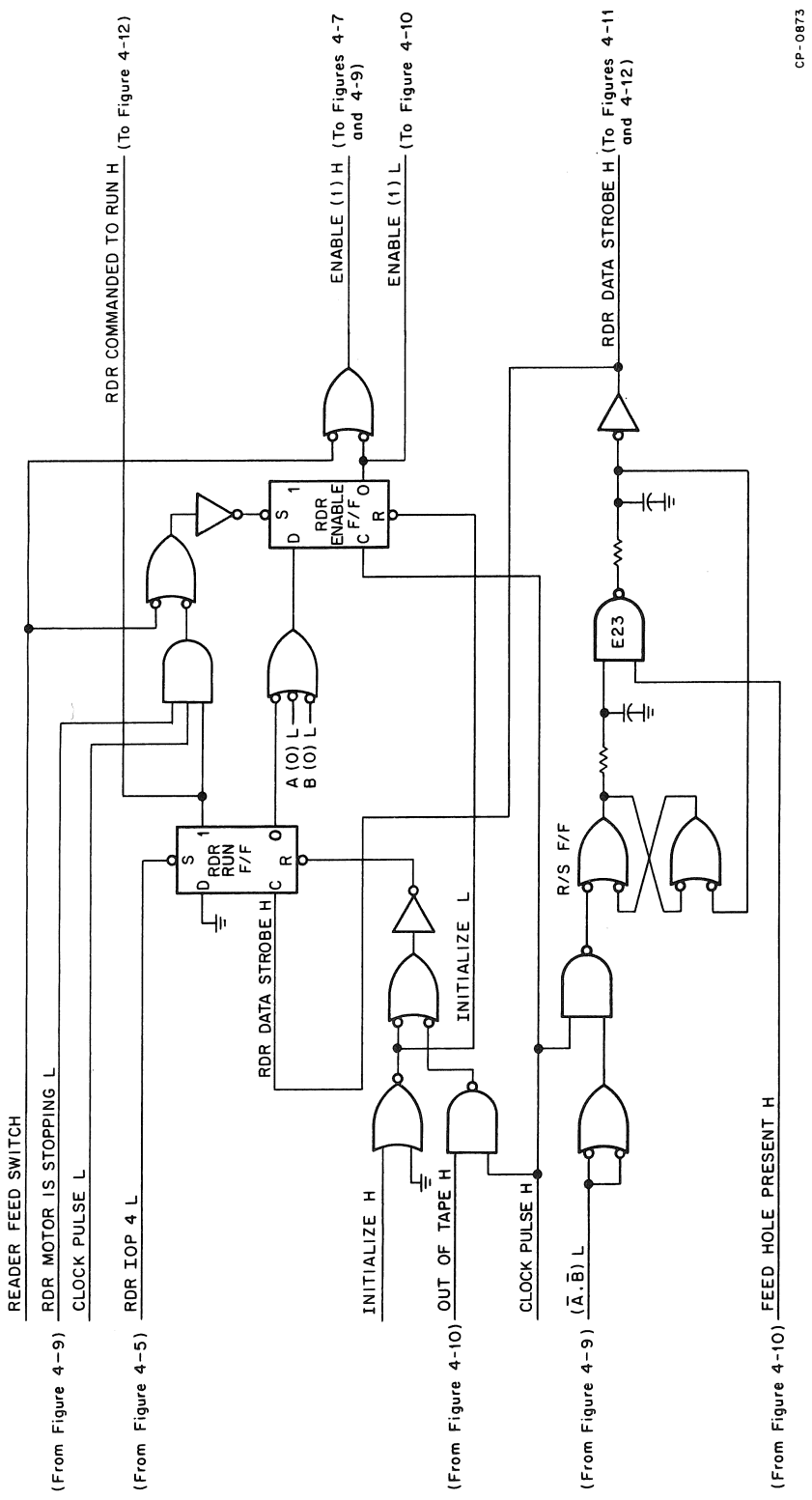


Figure 4-6 Reader Control Logic

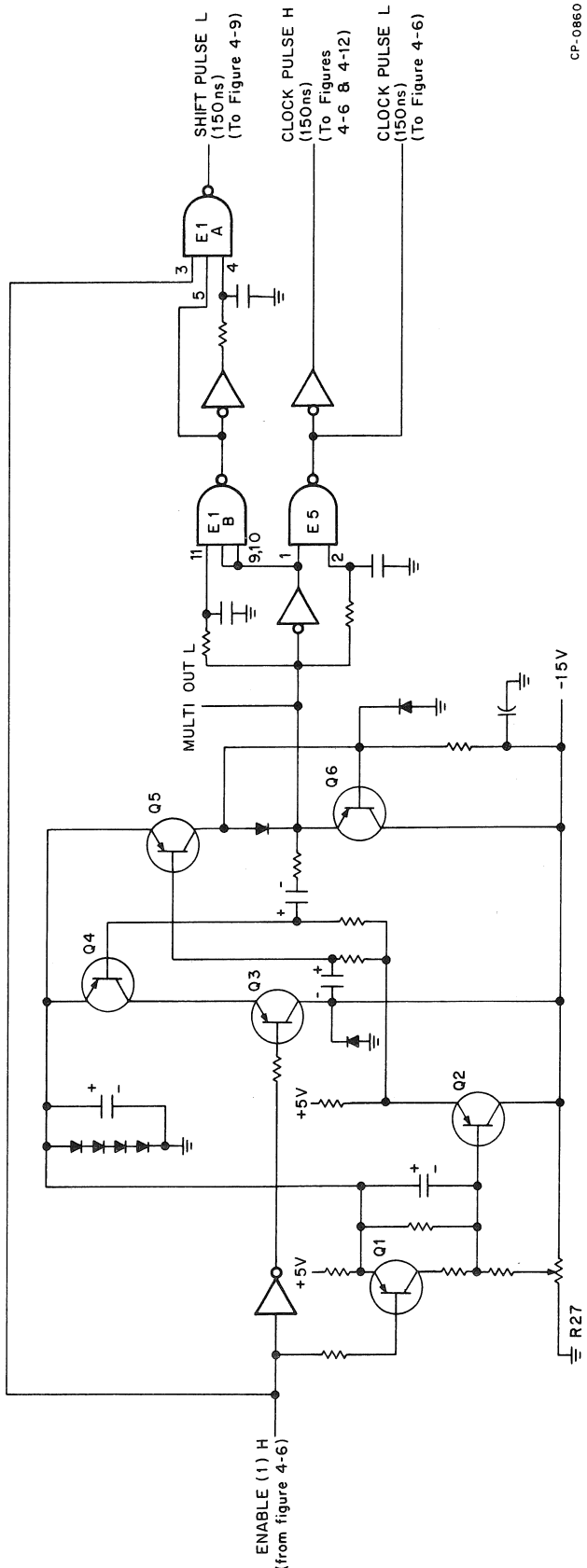


Figure 4-7 Clock Logic

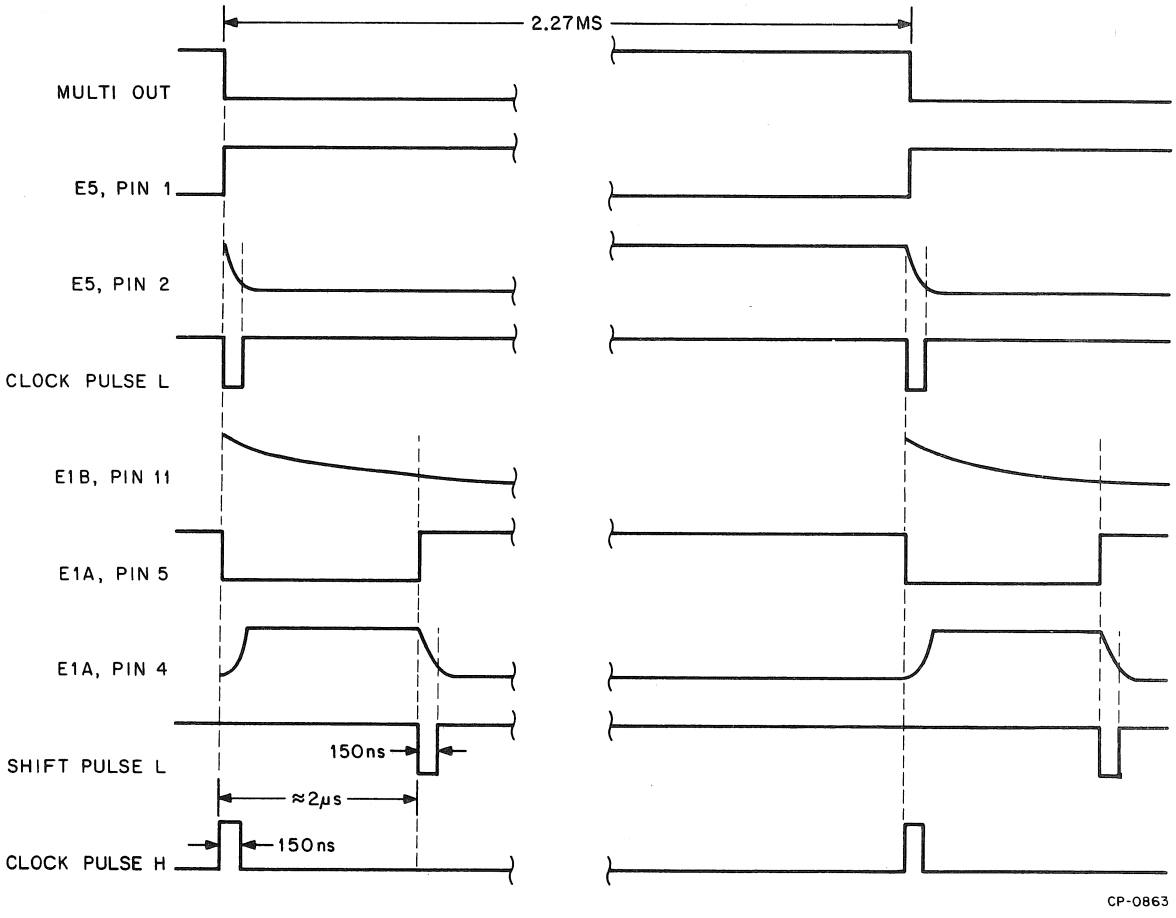


Figure 4-8 Clock Timing

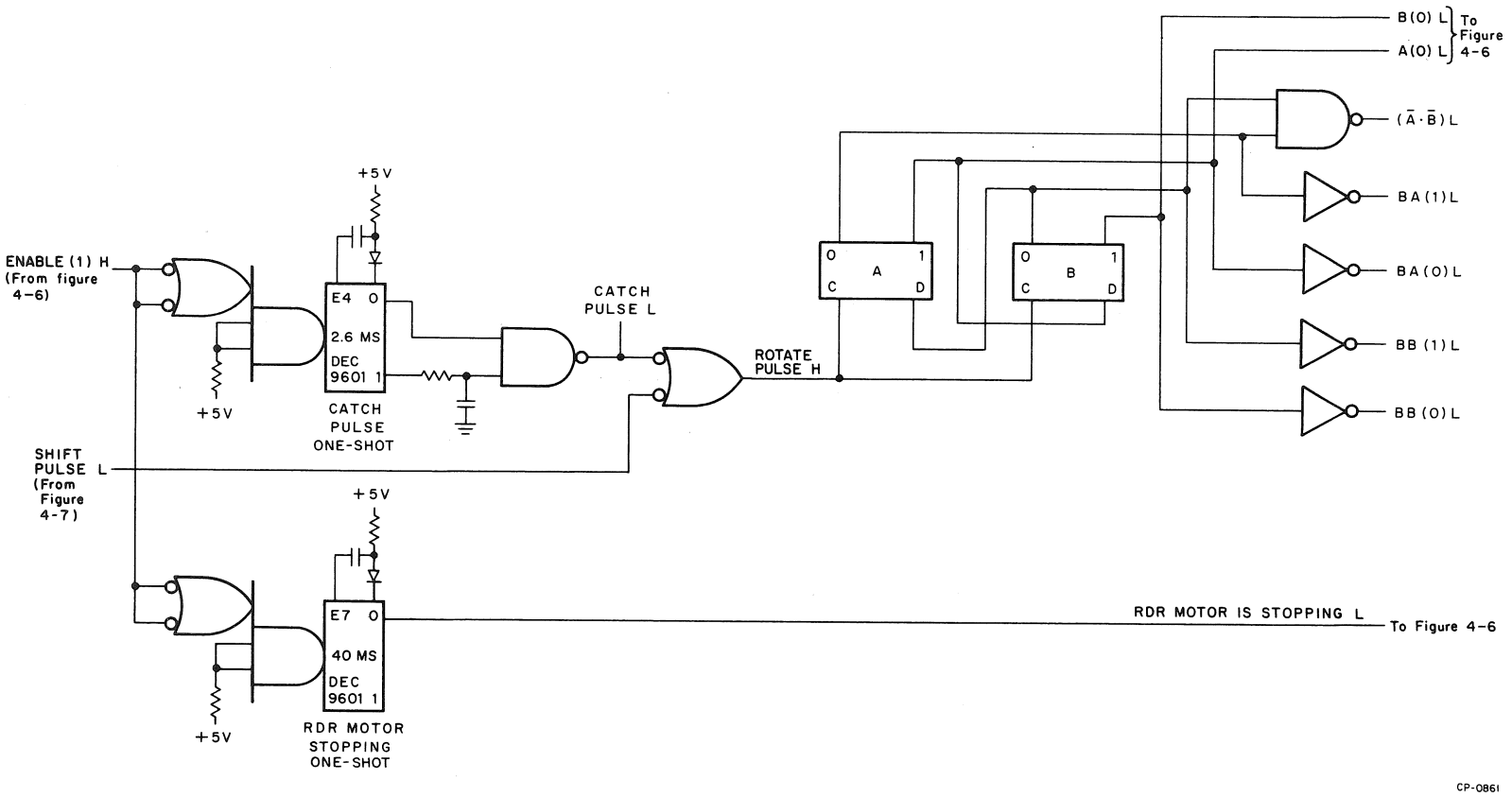


Figure 4-9 Reader Motor Control Logic

Table 4-1
Reader Motor Control Logic Stepping Sequence

	$(\overline{A}\cdot\overline{B})$ L	A (0) L	B (0) L	BA (1) L	BA (0) L	BB (1) L	BB (0) L
1st Shift Pulse	H	H	L	H	L	L	H
2nd Shift Pulse	H	H	H	H	L	H	L
3rd Shift Pulse	H	L	H	L	H	H	L
CATCH PULSE	L	L	L	L	H	L	H

The elapsed time between RFC instructions determines whether the motor is advanced continuously or STOPS. If a subsequent RFC instruction is not received within 6.81 ms after RDR ENABLE flip-flop is set, ENABLE (1) H is cleared, triggering one-shots E4 and E7. One-shot E4 times out in 2.6 ms and asserts CATCH PULSE L which generates the final rotate pulse. Triggering one-shot E7 asserts RDR MOTOR IS STOPPING L for 40 ms. The assertion of RDR MOTOR STOPPING L inhibits the setting of the RDR ENABLE flip-flop in the reader control logic (Figure 4-6), thereby inhibiting the initiation of a new read character operation. Thus, the reader motor is allowed 40 ms to come to a complete stop. If a subsequent RFC instruction is received within 6.81 ms after the RDR ENABLE flip-flop is set, the ENABLE (1) H remains asserted and the clock continues to generate shift pulses.

4.3.1.5 Tape Status Logic – The tape status logic monitors the presence of paper tape in the reader and inhibits read character operations when the tape runs out (Figure 4-10 and engineering drawing E-CS-M840-YA-1, sheet 2). With no tape in the reader, the tape status logic is in its quiescent state. The ENABLE (1) L input is cleared, the FEED HOLE line is HIGH (+3 V), transistor Q7 is on, Q8 is off, the output of E26 is HIGH, the R/S flip-flop is set placing a HIGH on inverter E3 and the one-shot is cleared asserting OUT OF TAPE H.

When a tape is loaded into the reader, the tape passing over the feed hole photo transistor momentarily blocks the light source forcing the FEED HOLE line LOW (+0.2 V). The resulting negative transition turns Q7 off, and Q8 on placing a HIGH on E26. The output of E26 then goes LOW triggering one-shot E19 and clearing the R/S flip-flop thus satisfying AND gate E17. The LOW from AND gate E17 serves to hold the one-shot in the triggered state asserting HAVE TAPE H. Once the tape is positioned properly in the reader the FEED HOLE line goes HIGH and remains HIGH until the tape is advanced or removed.

When the processor generates an RFC instruction, the ENABLE (1) L input asserts and sets the R/S flip-flop disabling AND gate E17 and one-shot E19 begins to time-out. As the tape is advanced the FEED HOLE line goes LOW, re-triggers E19, and remains LOW until the tape reaches the next data position. If the processor generates another RFC instruction within 6.81 ms after ENABLE (1) L asserts, ENABLE (1) L remains asserted, the tape is advanced to the next data position, the FEED HOLE line goes HIGH, FEED HOLE PRESENT H asserts, the data is strobed, the tape is advanced toward the next data position and the FEED HOLE line goes low again re-triggering the one-shot before it times out. On the other hand, if the processor fails to generate another RFC within 6.81 ms, ENABLE (1) L clears before the tape reaches the next data position, and the LOW on the FEED HOLE line resets the R/S flip-flop, satisfying AND E17, thereby holding the one-shot in the triggered state. When the next data position is reached the FEED HOLE line goes HIGH asserting FEED HOLE PRESENT H and the reader motor control logic inhibits tape advancement for at least 40 ms.

Should the tape run out while being advanced, the FEED HOLE input goes HIGH and remains HIGH. Thus the negative transition necessary to re-trigger the one-shot when the motor is being advanced continuously and the LOW which resets the R/S flip-flop when the motor is stopping are no longer generated. As a result, the one-shot times out and asserts OUT OF TAPE H.

4.3.1.6 Reader Buffer Register and Bus Driver – The reader buffer register stores the data read from the tape and the bus drivers assert the data onto the OMNIBUS (Figure 4-11 and engineering drawing E-CS-M840-YA-1, sheet 3). When the processor generates an RFC instruction, RDR DATA STROBE H asserts and loads the data into the register flip-flops. When an RRB instruction is generated, RDR DATA TO OMNIBUS H asserts, gates the data onto the OMNIBUS, and asserts C1 L.

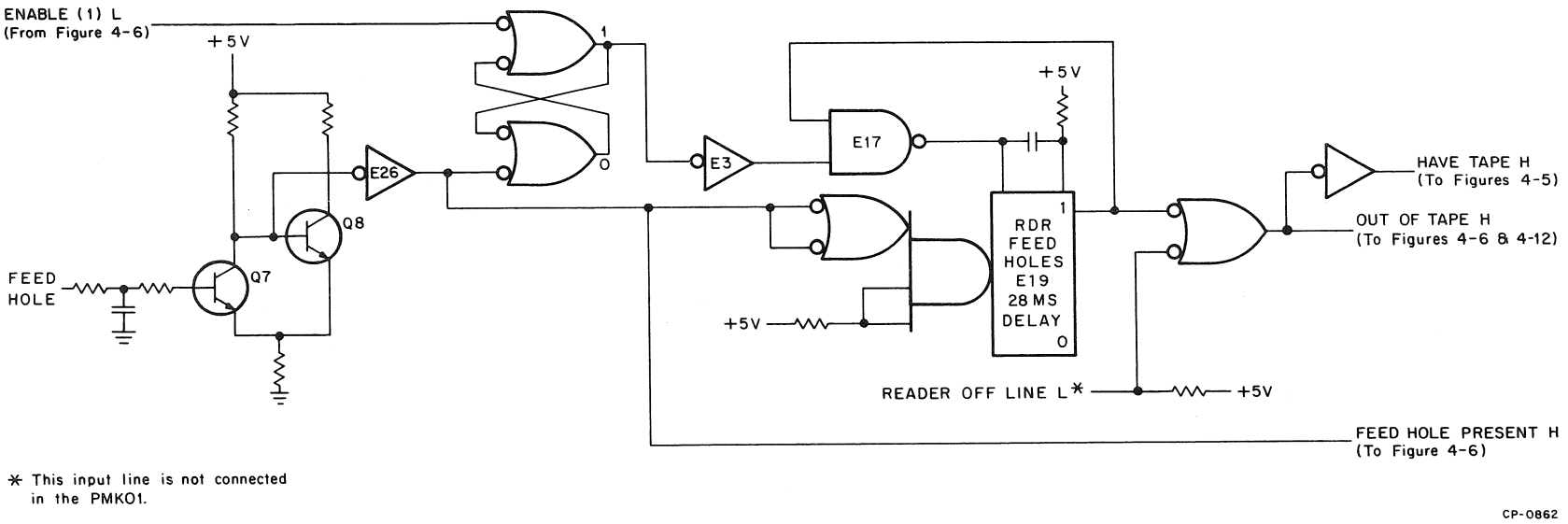


Figure 4-10 Tape Status Logic

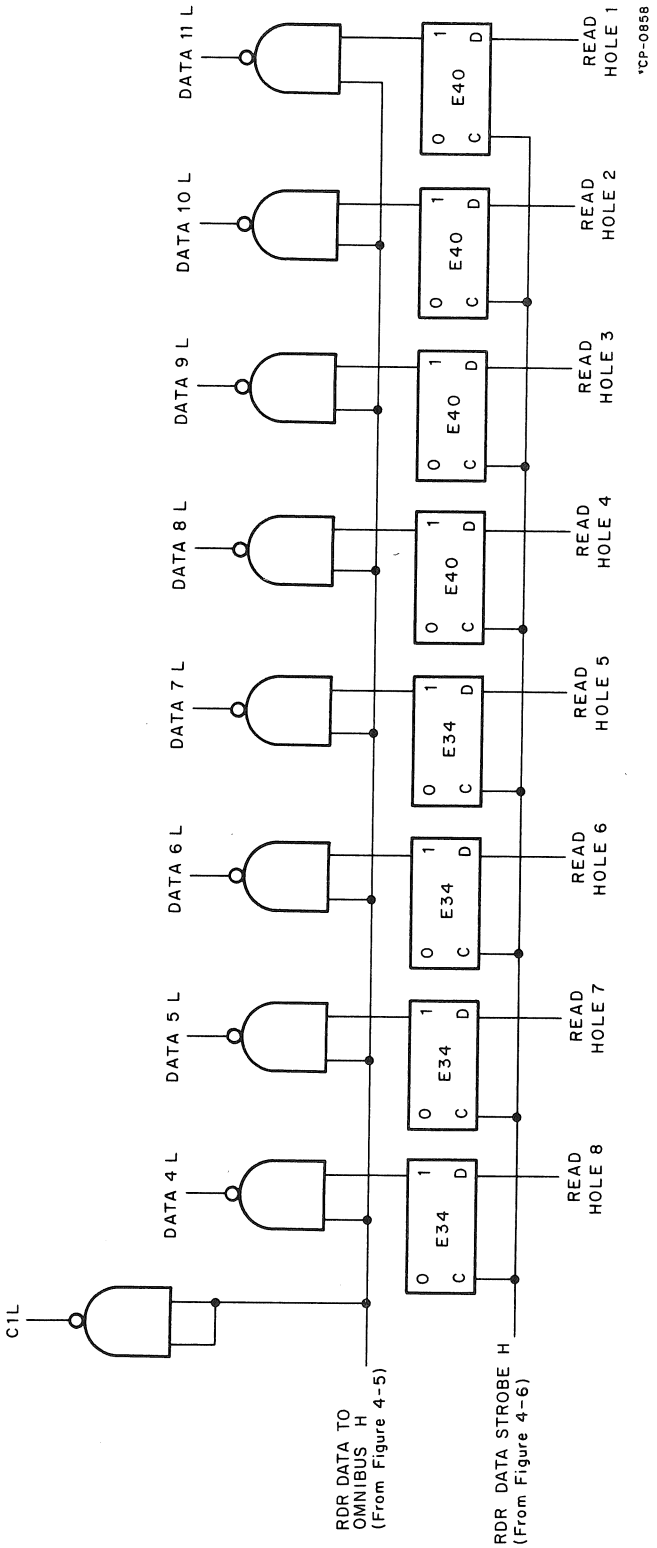


Figure 4-11 Reader Buffer Register and Bus Drivers

4.3.1.7 **Interrupt Control Logic** – The interrupt control logic asserts INT RQST L and SKIP L to the OMNIBUS notifying the processor of data being held in the reader buffer register for reading (Figure 4-12 and engineering drawing E-CS-M840-YA-1, sheets 2 and 3).

The interrupt control logic responds to processor generated instructions as follows:

- An RPE instruction causes the assertion of SET INT ENA L which sets the INT ENABLE flip-flop.
- An RSF instruction enables AND gate E18. If the RDR Flag flip-flop is set when the gate is enabled, SKIP L asserts on the OMNIBUS.
- An RRB instruction causes the assertion of IOP 2 L which resets the RDR Flag flip-flop.
- An RFC instruction causes the assertion of RDR IOP 4 L which resets the RDR Flag flip-flop and also the assertion of RDR COMMANDED TO RUN H and the RDR DATA STROBE which combine to set the RDR Flag flip-flop. Setting both flip-flops (RDR Flag and INT ENABLE) asserts INT RQST L to the OMNIBUS.
- A PCE instruction causes the assertion of RESET INT ENA L which resets the INT ENABLE flip-flop. If OUT OF TAPE H is asserted when a clock pulse occurs, the RDR Flag flip-flop is reset inhibiting both flag output AND gates.

4.3.1.8 **Phototransistor Assembly** – The Phototransistor Assembly, consisting of nine photosensitive transistors, is arranged below the tape track perpendicular to the direction of tape movement (Figure 4-13). A light source, located directly above the transistors, provides the light necessary for sensing holes in the tape. Eight of the transistors sense the coded holes; the ninth senses the feed hole.

The transistor output, when shuttered from light, is below the threshold of the photo transistor amplifier. If the transistor is exposed to light, its output current increases in a positive direction and overcomes the photo transistor amplifier circuit threshold.

4.3.1.9 **Photo Transistor Amplifier Circuit** – The photo transistor amplifier, consisting of nine amplifiers and a threshold control circuit, monitors the outputs of the photo transistors (Figure 4-13 and engineering drawing C-CS-G918-0-1). If the photo transistor output is below the base bias on transistor Q1 (the bias level is controlled by the threshold control), Q1 is off, Q2 is on, and the output is +0.2 V. When the input overcomes the bias level, Q1 turns on, turning Q2 off and +3.0 V is placed on the output.

4.3.1.10 **Tape Advance Circuit** – The tape advance circuit advances the tape in response to solenoid switching signals from the reader/punch control (Figure 4-14 and engineering drawing B-CS-M060-0-1).

Two drivers must be enabled to advance the motor. Driver No. 4 is disabled when a LOW is placed on the input OR gate turning Q1 on and Q2 off. To enable the driver a HIGH is placed on the input turning Q1 off and Q2 on, thereby causing current flow through Q2 to ground. The sequence of driver selection is shown in the motor stepping sequence chart in Figure 4-14. A complete motor stepping sequence advances the tape from one data position to the next data position.

4.3.2 PDP-11 Configuration

The following paragraphs provide a detailed logic level description of only the PC11 interface module logic, as the operation of the reader control and reader clock logic is identical to the operation of the logic contained on the Reader/Punch Control Module (M840-YA), which is used in the PDP-8E/8F/8M configuration.

4.3.2.1 **Address Selection and Mode Control Selection Logic** – The address selection and mode control logic decodes the A and C bits placed on the Unibus by the program and generates the gating and strobe signals necessary to perform the operation decoded (Figure 4-15 and engineering drawing D-CS-M7810-0-1, sheets 3 and 4).

The PC11 interface uses jumpers for address selection. These jumpers control the input to one pin of each of the ten comparators. The inputs to the other comparator pins are controlled by A bits 03–12. If the A bit input matches the jumper controlled input, the comparator is satisfied and the output pin goes HIGH. For example, jumper A7 is normally installed, therefore, BUS A 07 L must be cleared (+3 V) to satisfy the comparator.

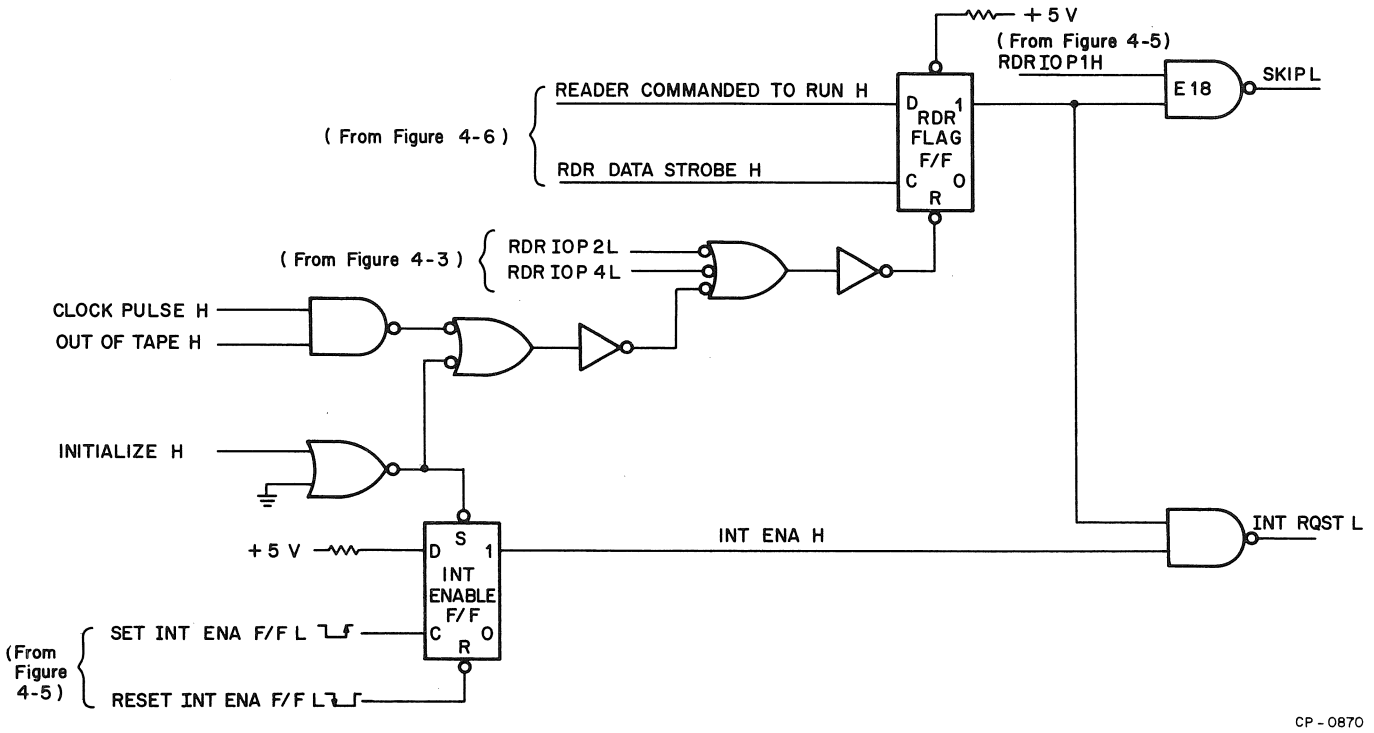


Figure 4-12 Interrupt Control Logic

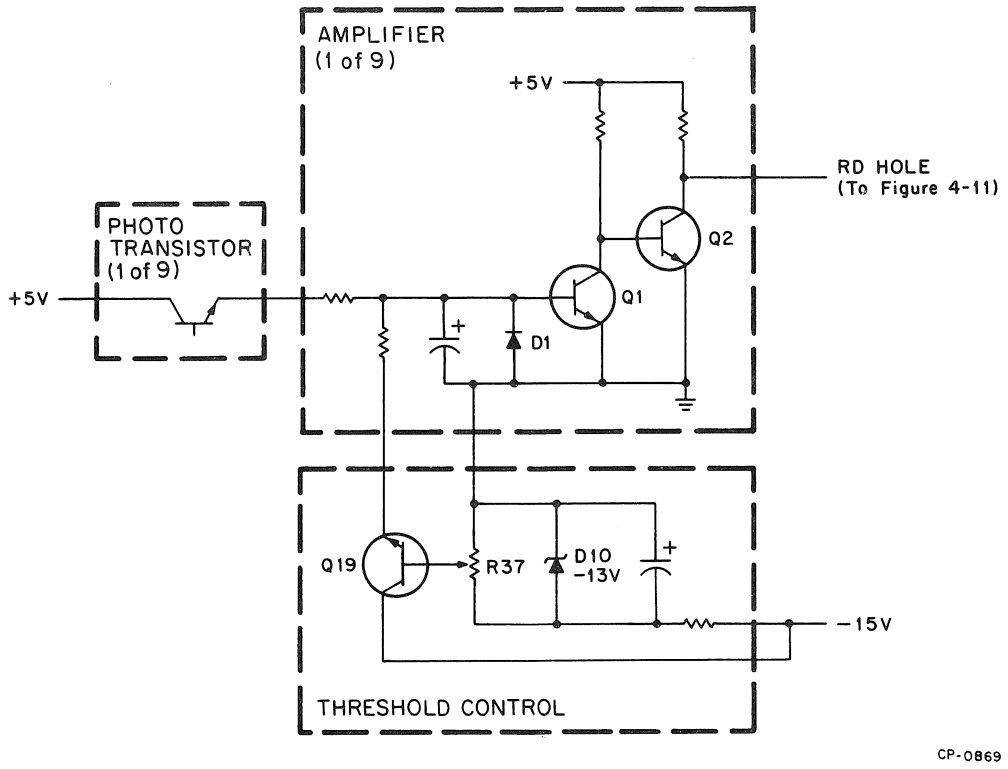


Figure 4-13 Tape Read Circuit

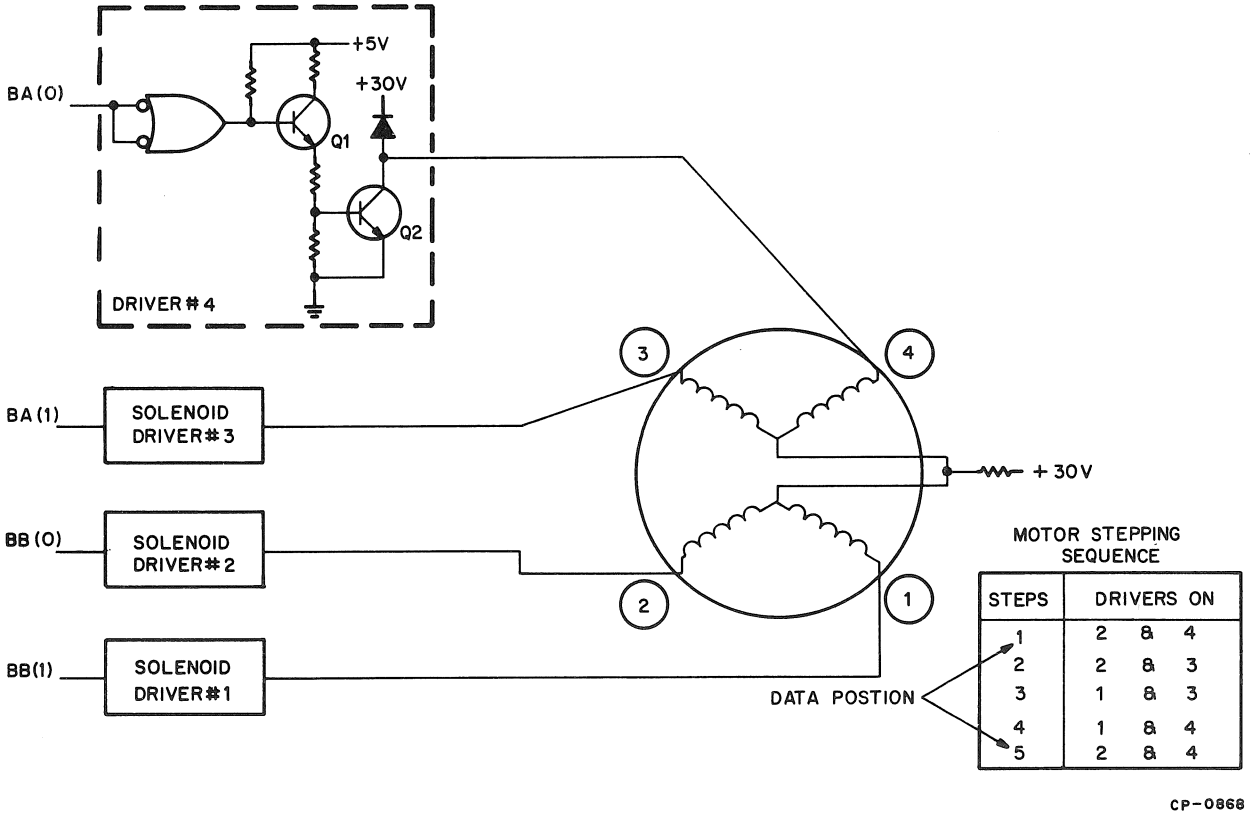


Figure 4-14 Tape Advance Circuit

Hence, to address the PC11 interface, the program must generate a bus address that matches all the jumper controlled inputs. When such an address is placed on the bus, all the comparators are satisfied and COMP H (Compare) asserts. Whenever the program generates a device address, DEV ADDR H (Device Address) asserts because all device addresses are relegated to the upper 4K words of address space and MSYN accompanies all addresses. Hence, REG SEL L (register select) is asserted enabling the BUS SSYN circuit and conditioning strobe select AND gates (E21, E28, and E29).

Thus, the PC11 is selected and the remaining A bits (A00–A02) and C bits (C00, C01) must be decoded to select the particular register and determine the mode of data transfer. Refer to Tables 4-2 and 4-3 for bit configurations required to select each register and each particular mode respectively.

Table 4-2
Bus Address Register Select Bit Configurations

Register	Bus Address Bits 02	01	00*
PRS	0	0	0
RRB	0	1	0

*This bit is cleared for all PMK01 operations.

Table 4-3
Bus Operation Control Bit Configurations

Mode	Control Bits C1	C0
DATI	0	0
DATIP	0	1
DATO	1	0
DATOB	1	1

Note: DATI causes data to be transferred from the interface to the computer. DATO causes data to be transferred from the computer to the interface.

If for example a DATO (data out) operation is to be performed to load the PRS, the BUS A (02–00) and BUS C0 L lines are cleared and BUS C1 L is asserted. This enables AND gates E29A, E28A, and E28B, asserting SELECT 0 H, OUT LOW H and OUT HIGH H. SELECT 0 H is then ANDed with OUT LOW H to assert LOAD PRS H.

The SSYN circuit accomplishes the assertion BUS SSYN L to notify the processor of completion of transfer. When REG SEL L asserts, the SYNC delay circuit starts to time out and after 500 ns, BUS SSYN L asserts. If the processor asserts SSYN INH L (syn inhibit), BUS SSYN L is inhibited.

4.3.2.2 **Paper-Tape Reader Status Register** – The paper-tape reader status register stores control data and monitors status lines to and from the Reader Control Module (Figure 4-16 and engineering drawing D-CS-M7810-0-1, sheet 3).

When the program places the necessary A, C, and D (data) bits on the Unibus to perform PRS load operation, the LOAD PRS H input asserts and sets the INT ENB flip-flop and gates bit 00 (RDR ENB) through the register, thereby asserting IOP 4 (1) H and disabling the INT A H AND gate. When LOAD PRS H clears the INT A H AND gate is re-enabled. The register also monitors the status lines from the Reader Control Module. If I/O BUS INT L asserts, DONE H asserts to the bus drivers and INT A H asserts to the interrupt control logic. If RDR OUTAPE H asserts, ERROR H asserts to the bus driver and INT A H asserts. If RDR RUN (1) L asserts BUSY H asserts.

4.3.2.3 **Interrupt Control** – The interrupt control logic permits the PC11 interface to gain control of the bus (become bus master) and perform an interrupt operation. The jumpers on this logic are arranged so that the logic has a normal vector address of 70 for a reader and 74 for a punch (jumpers in bit positions 3, 4, and 5). Although this is the recommended vector address, the user may change the jumpers to correspond to any address desired, but MAINDEC programs and other software referencing the standard vector address assignments must be changed to reflect the new assignments.

NOTE
A jumper represents a 1, no jumper represents a 0.

The interrupt control logic consists of a dual-input request and grant acknowledge circuit for establishing bus control.

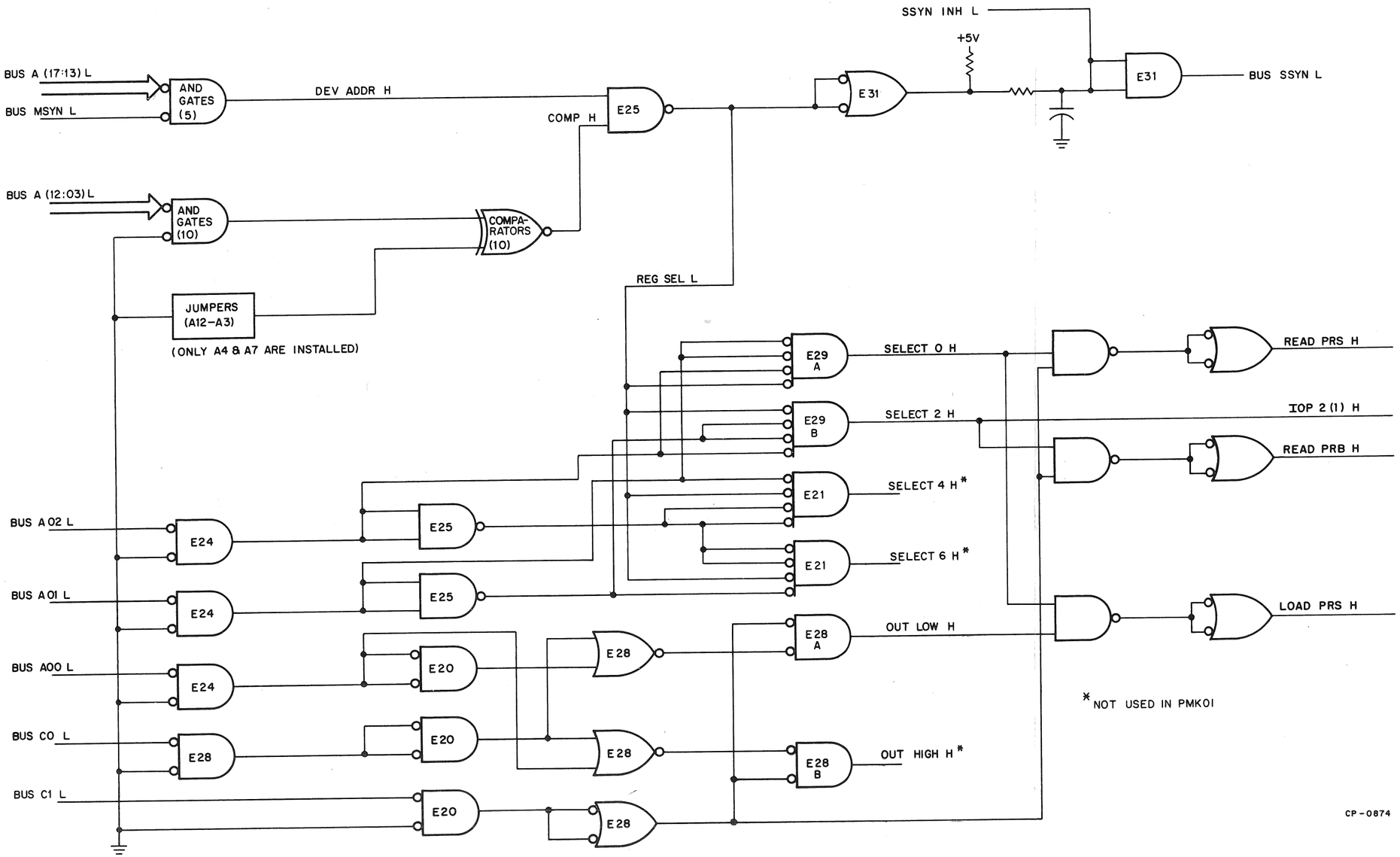


Figure 4-15 Address Selection and Mode Control Simplified Logic Diagram

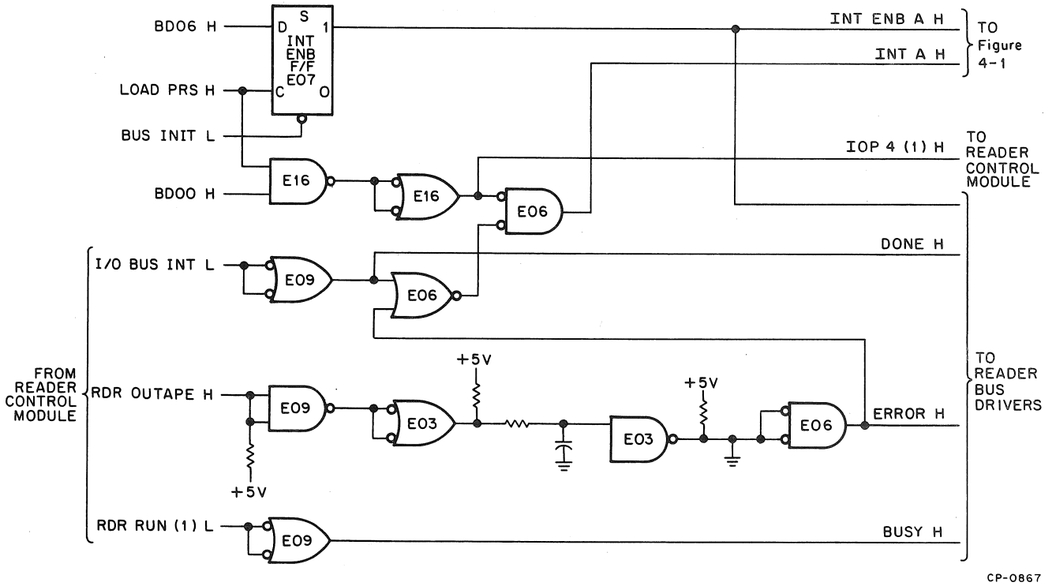


Figure 4-16 Paper-Tape Reader Status Register

The "A" input is connected to the reader control logic and provides a vector address of 70; the "B" input is connected to the punch control logic and provides a vector address of 74. The B input is not used in the PMK01.

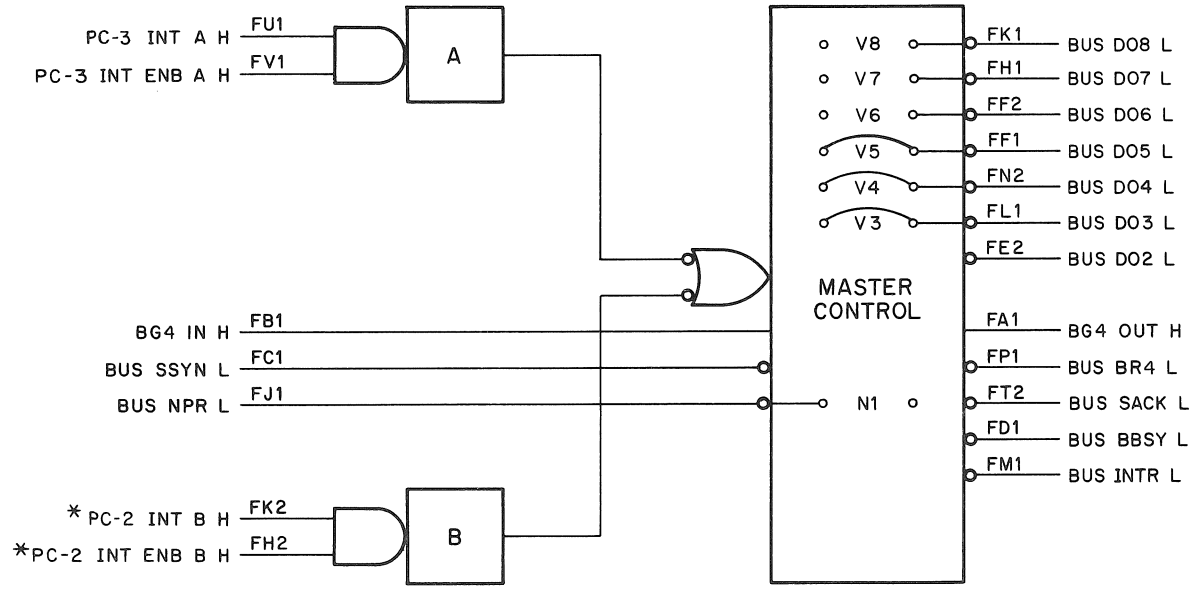
Before the "A" input interrupt logic can generate an interrupt request, two input signals must be high: INT A and INT ENB A. When a 1 is loaded into bit 06 of the reader status register (PRS), it sets the INT ENB flip-flop to produce INT ENB A H. This signal is applied to the interrupt control logic as an enabling signal. Whenever an ERROR condition (RDR OUTAPE H) or DONE condition (I/O BUS INT L) occurs in the reader, a series of gates are qualified to produce INT A H.

The "A" input section of the interrupt logic (Figure 4-17) is used to gain control of the bus. When both the INT A and INT ENB A requesting inputs are asserted, a bus request is made on the BR level corresponding to the level of the priority plug in the logic. The standard level for the PC11 interface is BR4, but this may be changed by changing the priority plug. When the priority arbitration logic in the processor recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. When the PC11 interface has fulfilled all requirements to become bus master (BBSY false, SSYN false, and BG false) the master control section asserts BBSY.

Once the PC11 interface has gained bus control by means of a BR request, an interrupt is generated. The interrupt vector address is selected by jumpers on the logic as shown on Figure 4-17.

Because the vector is a 2-word (4-byte) block, it is not necessary to assert the state of bits 0 and 1. The six selectable (jumpered) lines determine the two most significant octal digits of the vector address. The least significant octal digit is controlled by bit 02, so that all vector addresses end in either 0 or 4. The input to bit 02 is tied to the V2 flip-flop logic. Whenever an interrupt occurs on the "A" input logic, bus line D02 is not asserted, and the interrupt causes a vector at location 070. When an interrupt occurs on the "B" input logic, bus line D02 is asserted, and the interrupt causes a vector at location 074. The first two digits can be changed by jumpers but the last digit is always 0 or 4.

The BG IN signal is allowed to propagate through the logic to BUS BG OUT when the interface is not issuing a request. To request bus use, the AND condition of INT and INT ENB must be satisfied. These levels must be true until the interrupt service routine clears INT or INT ENB. Once bus control has been attained, it is released when the processor has strobed in the interrupt vector. After releasing bus control, the logic inhibits further bus requests from that



NOTES:
1. Bus request made on level 4.
2. Interrupt vector is 70 for "A" input; 74 for "B" input.
3. Jumpers are: jumpers for a 1, no jumpers for a 0.

* These signals not used in PMK01.

11-0939

Figure 4-17 Interrupt Control Simplified Logic Diagram

particular input ("A" or "B") even if INT and INT ENB remain asserted. In order to make another bus request, INT or INT ENB must be dropped and then reasserted to cause the logic to reassert the request line. This prevents multiple interrupts when the logic is used to generate interrupts. The interrupt control logic used in the PC11 interface is not capable of issuing NPR requests.

To improve NPR (Non-Processor Request) latency, the NPR input is sampled. When this input is asserted, the BG OUT output is inhibited, thereby inhibiting the granting of the bus (via the BG IN input) to any device on the same BR level as the PC11 interface and electrically further from the processor.

CAUTION

Only certain PDP-11 processors use the NPR circuit described. The jumper (N1) on the module, when cut, disables the NPR circuit.

CHAPTER 5
MAINTENANCE

5.1 INTRODUCTION

This chapter contains both preventive and corrective maintenance procedures. An optimum amount of preventive maintenance, performed on a routine schedule, can eliminate costly equipment breakdowns and detect impending failures.

The PMK01 is a dependable and relatively maintenance-free assembly. For example, the tape reader motor is electromagnetically driven; thus, it does not experience the mechanical failures normally inherent in systems using ratchets, detent, and clutch-brake mechanisms. If a specific item does fail, equipment design is such that replacement of modular elements can restore the equipment to service in a minimum amount of time.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance tasks should be performed at periodic intervals to ensure proper equipment operation and to minimize unscheduled downtime. These tasks consist of visual inspection, operational checks, cleaning, adjustment, and replacement of borderline, or partially defective parts. Table 5-1 provides a recommended preventive maintenance schedule for the paper-tape reader.

Preventive maintenance scheduling is contingent on environmental and operating conditions. Under normal conditions routine preventive maintenance should be performed after every 600 hours of operation (or every three months, whichever occurs first). This schedule should be modified when extreme temperature, humidity, dust, or work-load conditions exist.

Table 5-1
Preventive Maintenance Schedule

Performance Interval	Test or Procedure
Monthly	Visually inspect the unit for physical damage, correct if required.
Monthly	Check that all modules are properly seated in the wired assembly.
Quarterly (every 3 months)	Clean the interior and exterior of the unit, using a vacuum cleaner or a clean cloth that has been moistened with a nonflammable solvent.
Quarterly	Inspect the following components for mechanical security: Reader Feed switch, light source, phototransistor assembly, tape depressor, tape hold-down bracket, all connectors and circuit modules and reader motor. Run the Reader Diagnostics: PDP-8E/8F/8M – PRG2 PDP-11 – PRG0

5.3 CORRECTIVE MAINTENANCE

5.3.1 PMK01 Reader Adjustments

5.3.1.1 Introduction – The adjustment procedures for the PMK01 paper-tape reader are explained here. The procedures should be followed as closely as possible and should be performed in the order listed. Tools and equipment required are listed in Table 5-2. MAINDEC diagnostic programs are listed in Appendix B. If the unit can read programs, it is advisable to load the diagnostic in at this time. If not, the ONE-ZERO test tape can be used.

NOTE

This procedure was written for a completely misadjusted machine; adjustments that are already correct need not be redone. It is good policy, however, to check each adjustment to be sure it is correct.

5.3.1.2 Test Tape Registration – (Refer to Appendix B.) If the tapes are not in accurate registration (ten characters per inch), the reader may not be able to read them. To check registration, proceed as follows:

1. Obtain the prepunched ONE-ZERO tape and the tape registration gauge.
2. Use the pins on the gauge to check that the registration is not off by more than one-half feed hole per 6 inches of tape.
3. The gauge provides holes 1 inch apart. Check that every one of these holes is uncovered. If some holes are covered and the feed holes line up with the two pins 6 inches apart, registration is off by a multiple of one hole spacing.
4. It is also important that the feed holes be evenly spaced 0.1 inch from each other. This can be checked by sighting along the punched tape at a shallow angle.

Table 5-2
Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 547 or 453
Plug-in Unit	Tektronix	Type CA (for 547 scope)
X10 Probe	Tektronix	P6008
Module Extender	DEC	W980
Tape Registration Gauge	Teletype	156011 (DEC No. 29-15792)

5.3.1.3 Feed Wheel and Motor Adjustment – This adjustment properly positions the feed wheel on the motor shaft, placing the tape data holes in their proper relationship with the photo transistors.

1. Advance the feed wheel by momentarily pressing the Reader Feed switch. This will ensure that the motor stops *on* a character and not *between* characters.

2. Install a piece of ONE-ZERO test tape (about 6 inches long) over the photo transistors and hold it on the feed wheel by means of the tape depressor.

NOTE

Check data hole to photo transistor alignment. If alignment is correct, *do not* perform steps 3 through 7.

3. Loosen the two Allen screws that hold the feed wheel to the motor shaft.

4. Move the feed wheel in or out so the tape rubs lightly against the backplate. The tape must not be jammed against the backplate, nor should there be a gap between the tape and the eight level slide (right-hand side of the tape path guide). Jamming will cause paper handling problems and a gap can cause skew. At the same time, rotate the feed wheel on the shaft until the holes in the tape have approximately the relation to the photo transistors as shown in Figure 5-1. Tighten the Allen screws. Repeat Step 1 and check the alignment per Figure 5-1.

   If the Allen screws have dented the shaft, it may be difficult to make a small correction, since the screws tend to slide back into the original dents. To correct this, rotate the wheel on the shaft about one quarter turn and repeat this step. The important adjustment in this step is the in and out adjustment. Be sure the tape is not jammed.

5.3.1.4 Tape Depressor

1. Loosen the two Phillips screws holding the tape depressor to the shaft.

2. Place one thickness of unpunched paper tape (except for feed holes) on the feed wheel and lower the tape depressor.

3. Apply light finger pressure on the horizontal position of the tape depressor, centering the slot in the depressor around the feed wheel teeth (Figure 5-2).

4. Tighten the screws. The heel and toes of the depressor should now make a four-point contact with the paper, holding it evenly against the feed wheel.

5.3.1.5 Tape Hold-Down Bracket – The purpose of this adjustment is to limit the vertical motion of the tape as it passes the read station, yet allow room for passage of splices and folds.

1. Loosen the two Phillips screws holding the bracket to the backplate.

2. Insert three thicknesses of unpunched tape (no folds included) under the hold-down bracket and up against the eight level slide.

3. Press down carefully on the left-hand side of the hold-down bracket and tighten the screws (Figure 5-3).

4. The tape should have even tension as it is being pulled out. If not, the bracket is bent, and not parallel with the tape path guide. Remove the bracket and adjust it, checking it with a square or the right angle formed by the tape path guide and the backplate. Remount and readjust the bracket. When the tape hold-down bracket is properly adjusted, point A limits tape skew and point B keeps the paper close to the photo transistors (Figure 5-3). Maladjustment at either point can cause misreads.

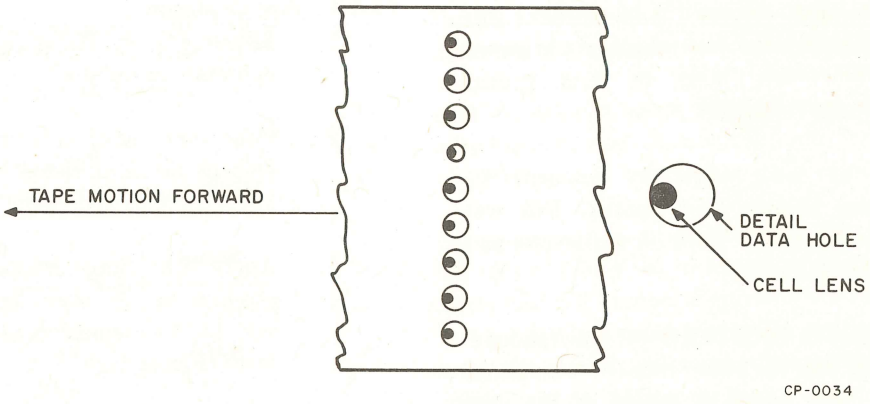


Figure 5-1 Feed Wheel and Motor Adjustment

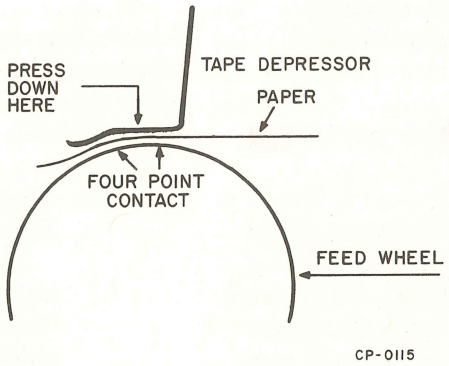


Figure 5-2 Tape Depressor

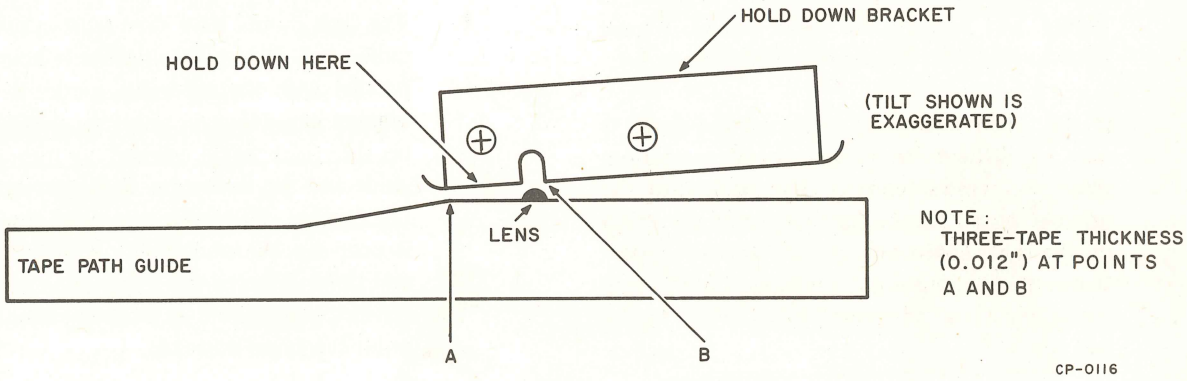


Figure 5-3 Tape Hold-Down Bracket

5.3.1.6 **Lamp, Lens, and Light Pattern**

1. Set the adjustable resistor in the lamp circuit for minimum resistance (maximum brightness). This will reduce the effects of stray outside light. Be sure that the photo transistors "turn off" when one thickness of the tape blocks the light.

2. Due to the offset filament in the lamp, the lamp should be placed in the reader so that the end with the lettering is nearest the backplate. This position will give a more uniform light at the phototransistor assembly. Rotate the lamp so the seam is not projected on the photo transistors.

3. Loosen the lens and rotate it so the light beam is concentrated and centered over the phototransistor assembly. A ONE-ZERO tape with the holes over the photo transistors will help define the light pattern. The pattern should appear as in Figure 5-4.

5.3.1.7 **Full-Speed Running Rate** – Proceed as follows to adjust the full-speed running rate to 110 ± 5 cps:

1. Connect an oscilloscope to the A (0) flip-flop (refer to Table 5-3 for pin locations).

2. Run the reader at full speed using either the Reader Feed switch or program control.

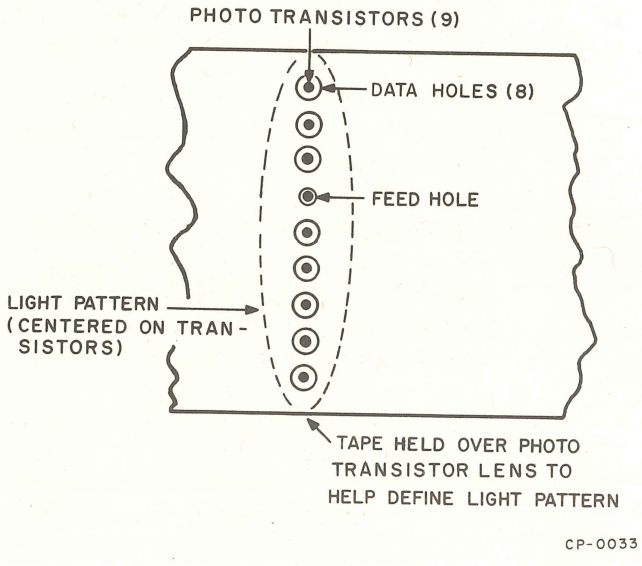


Figure 5-4 Light Pattern

3. Check the time between transitions of the A flip-flop. The time should be 4.55 ms. The time is adjusted by R6 on the M715 Module or R27 on the M840 Module.

Table 5-3
M060 Motor Driver Inputs and Outputs

Signal	In	Out
B (1)	A6T2	A3H2
B (0)	A6S2	A3K2
A (1)	A6R2	A3M2
A (0)	A6P2	A3P2

5.3.1.8 **Threshold and Skew** – Skew can be caused by feed wheel wobble. This wobble causes the tape to walk in and out across the phototransistor assembly, varying the outputs of the photo amplifiers. Skew can also be caused by phototransistor assembly placement in the tape path guide and placement of the individual transistors on assembly board. The relative sensitivity of each transistor will also cause skew.

1. Using a ONE-ZERO test loop, operate the reader at full speed by either program control or the FEED switch.

2. Set the oscilloscope to 1 ms/cm, 1 V/cm, triggering internal positive.

3. Connect the probe to the feed hole output of the G918 test point. See Table 5-4 for the pin location.

Table 5-4
G918 Photo Amplifier Pin Locations

Pin	PMK01
RH 1	A2E2
RH 2	A2F2
RH 3	A2J2
RH 4	B2D2
RH 5	A2L2
RH 6	A2N2
RH 7	A2P2
RH 8	A2R2
Feed Hole	A2T2
Sum (TP)	A2V2

PULSES

* CHECK RESPECTIVE INPUT FROM PHOTO SENSORS

4. Adjust the potentiometer on the G918 for a feed hole pulse width of approximately 4.5 ms (measured at the 10% point).

5. Observe the pulse stability. If the width varies more than 500 μs (1/2 ms), the feed wheel wobble is too great and the feed wheel must be replaced because it cannot be straightened. Do not mistake the passage of the tape loop splice for a variation. If the feed wheel must be replaced, repeat the procedure in Paragraph 5.3.1.3.

6. Observe the waveform at the SUM TP of the G918. It should appear as shown in Figure 5-5a. Measure the time "T" between the last data bit rise and the feed hole (slow rise signal). The time should be greater than 0.1 ms. If not, adjust by rotating the phototransistor assembly in its mounting hole as follows: Loosen the mounting screw of the assembly enough to allow light, finger-pressure movement. Gently rotate the assembly to maximize the time "T". Tighten the screw.

7. Turn the potentiometer on the G918 counterclockwise until a data bit is picked up on the all 0's section of the waveform. (Do not mistake the feed hole signal for a picked up bit when reading all 0's.) Then while counting the turns, turn the potentiometer in the opposite direction until a data bit or the feed hole is dropped in the 1's section of the waveform and set the potentiometer to the middle of these two extremes.

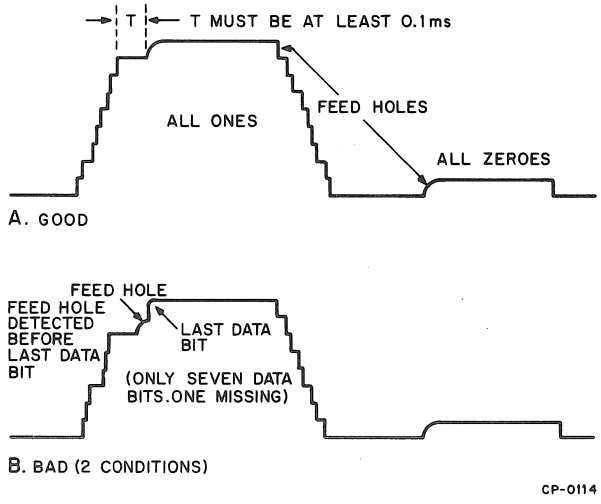


Figure 5-5 Summation Waveform, G918 Test Point

NOTE

These adjustments should be made using the tape with the highest transmissivity to be used on the system. For instance, if the reader is to read oiled tape, the threshold adjustment should be made while using oiled tape.

8. Recheck for a minimum of 0.1 ms time "T" as described in Step 6.

5.3.2 Testing and Error Correction

When the adjustment procedure is completed, test the reader for proper operation by reading a tape for which there is an error checking routine. The Special Binary count is recommended. If a test loop is used, be careful that the splice does not generate a false error indication.

5.3.2.1 Data Bits Picked Up – Data Bits are picked up if:

- Photo amplifier is not turning off. Return to threshold adjustment (refer to Paragraph 5.3.1.8).
- Photo transistor is exposed to stray light (determine if sunlight is falling on the reader).
- Data is picked up during transmission to processor due to faulty reader control module, cable, or processor.

5.3.2.2 Data Bits Dropped – Data Bits are dropped if:

- The photo transistor failed or the photo amplifier is not turning on. Return to threshold adjustment, Paragraphs 5.3.1.6 and 5.3.1.8.
- Skew. Return to Paragraphs 5.3.1.4, 5.3.1.5 and 5.3.1.8.
- Data is dropped during transmission to processor due to faulty reader control module, cable, or processor.

5.3.2.3 **Skipping Characters** – Skipping characters is caused by dropping the feed hole, which can be caused by:

- Skew. Return to Paragraphs 5.3.1.3, 5.3.1.5, 5.3.1.7 and 5.3.1.8.
- Threshold set incorrectly (refer to Paragraph 5.3.1.8).

5.3.2.4 **Double Reading** – If the reader reads a character twice, ensure that the adjustments in Paragraphs 5.3.1.4 through 5.3.1.8 are properly made.

5.3.2.5 **Dropping Flags** – The processor may lose the reader flag because of an out of tape indication. This may occur because of missing reader strobes (refer to Paragraphs 5.3.1.8 and 5.3.2.6).

5.3.2.6 **Out Of Tape Circuit Malfunction** – Failure of one of the M060 solenoid drivers may cause the reader motor to start so slowly that the out of tape 28 ms one-shot times out before it is re-triggered by the subsequent negative transition of the FEED HOLE line.

CHAPTER 6
PMK01 UTILIZATION

6.1 INTRODUCTION

The primary purpose of the PMK01 is to provide the technician with a rapid means of loading diagnostic programs (stored on paper tape) into the PDP-8E/8F/8M and PDP-11 computers. Before the diagnostic programs can be loaded, the computer must be programmed to accept them. The PDP-8E/8F/8M computers require that the RIM (Read-in-Mode) Loader and the BIN (Binary) Loader be loaded prior to loading the diagnostic programs. The PDP-11 Computers require that the Bootstrap Loader and Absolute Loader be loaded prior to loading the diagnostic programs.

Normally when a computer is taken off-line for maintenance, the actual content of its memory is not known. Therefore, it usually saves time to assume the computer memory has been wiped clean and start from scratch. Starting from scratch requires that the respective loader programs be loaded into the computer before an attempt is made to load the diagnostic programs.

The RIM and Bootstrap Loaders are the first programs to be loaded and therefore must be toggled into core memory. These programs instruct the respective computer to accept any data punched on paper tape in RIM/Bootstrap format and store it in core memory.

The BIN and Absolute Loaders are the second programs to be loaded into core memory and are loaded using the paper-tape reader. The BIN and Absolute Loaders are system programs punched in RIM/Bootstrap format that enable data punched on paper tape in BIN/absolute binary format to be loaded into any available memory bank. The Maintenance Loader program provides an alternate means of loading diagnostic programs when the PDP-11 Absolute Loader fails to function due to hardware failure. Figure 6-1 is a flowchart of the computer loading sequence.

The RIM/Bootstrap Loader and BIN/Absolute Loader programs are loaded into the upper most area of available memory so that they tend to survive most system program operations. Therefore, it is usually not necessary to reload them each time a new system program is to be loaded. The following paragraphs provide step by step procedures for loading the PDP-8E/8F/8M and PDP-11 loader and diagnostic programs.

6.2 PDP-8E/8F/8M COMPUTER PROGRAM LOADING

6.2.1 Loading the RIM Loader

1. Depress the HALT switch to give bus control to the console when powering up.

2. Turn OFF/POWER/PANEL LOCK switch to POWER position. This energizes the programmer's console.

3. If extended memory option is installed (extended memory option must be installed when memory size is 8K or larger), set Switch Register (SR) switches 6–8 and 9–11 to desired IF field and DF field respectively and depress ADDR Load.

   NOTE
   DECtape users should load RIM into field 0.

4. Set SR to starting address of RIM loader (Table 6-1) and depress ADDR LOAD. The address set in SR is shown in the MEMORY ADDRESS display.

5. Enter first instruction in SR and lift the DEP switch. The instruction set in SR is shown in data display.

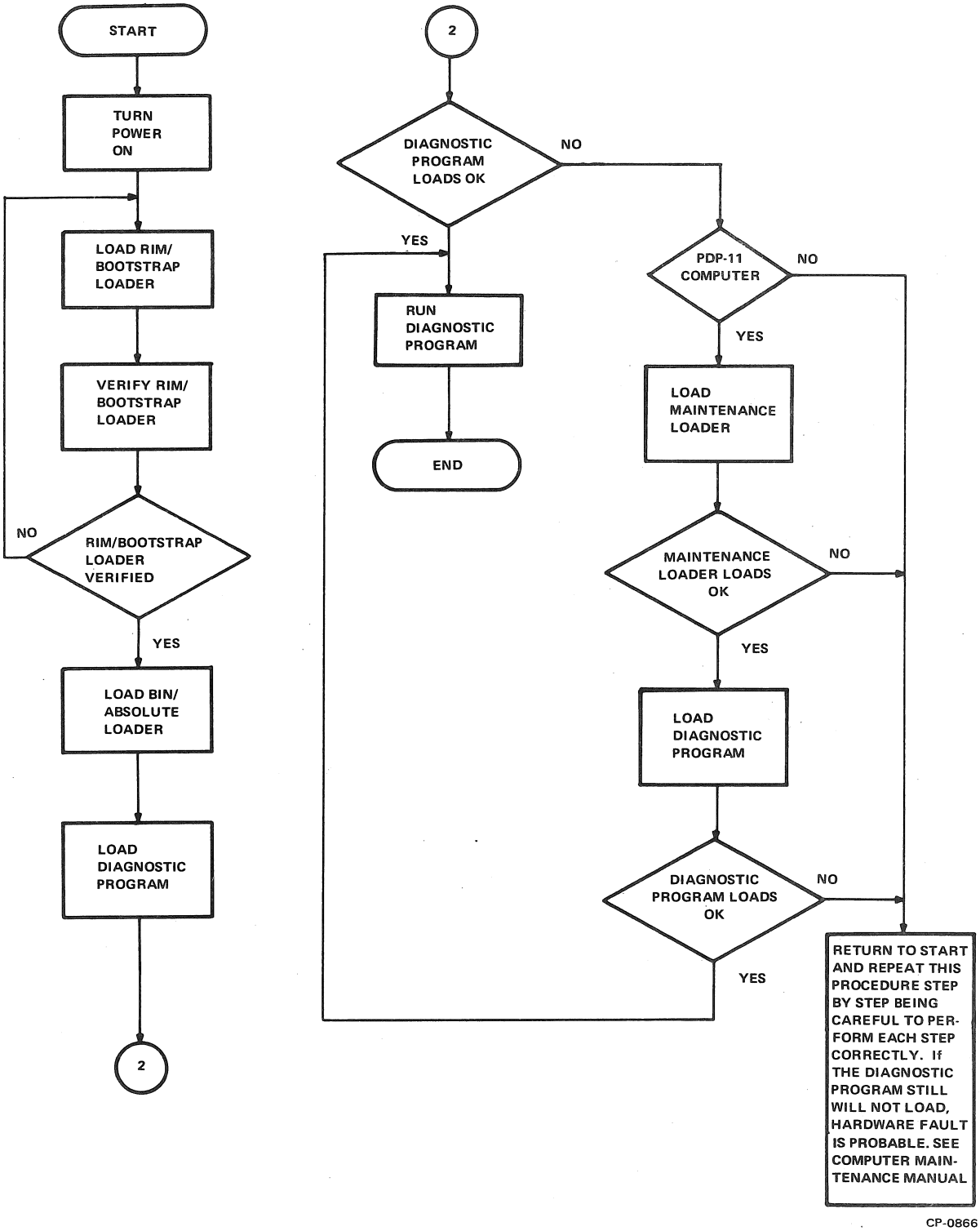


Figure 6-1 Computer Program Loading Flowchart

6. Enter next instruction into SR and lift the DEP switch.

NOTE

It is not necessary to load addresses after the starting address (7756) has been loaded because the address is automatically incremented by one each time DEP is used consecutively.

Table 6-1
RIM Loader Programs

Location	Instruction	
	Low-Speed Reader	High-Speed Reader*
7756	6032	6014
7757	6031	6011
7760	5357	5357
7761	6036	6016
7762	7106	7106
7763	7006	7006
7764	7510	7510
7765	5357	5374
7766	7006	7006
7767	6031	6011
7770	5367	5367
7771	6034	6016
7772	7420	7420
7773	3776	3776
7774	3376	3376
7775	5356	5357
7776	0000	0000

*The PMK01 is a high speed reader.

7. Repeat step 6 for each location of the RIM Loader.

8. The RIM Loader program is now loaded in memory locations and can be used to automatically load other programs into memory.

9. Correct program entry can be verified by examining the addresses between 7756 and 7776. This is accomplished by setting the starting address into the switch register, depressing the ADDR LOAD switch and depressing the EXAM switch. The contents of the starting address is shown in the data display. Each time the EXAM is again depressed, the address is automatically incremented by one and the corresponding contents displayed.

NOTE

Step 9 alone (verification) may be sufficient if the RIM Loader program has already been loaded into the system. The program is stored in the last portion of available memory so that it tends to survive program operation and is available for reloading programs. If the program is not intact, load RIM according to this procedure, beginning with step 1.

6.2.2 Loading the BIN Loader

1. Depress the HALT switch.

2. Be sure that the RIM Loader has been stored in core memory (Paragraph 6.2.1 step 9).

3. Enter starting address of RIM Loader (7756) into SR.

4. Depress ADDR LOAD switch. The address set in the SR is displayed in MEMORY ADDRESS display.

5. Place the PMK01 on-line (connected to the computer).

6. Place the BIN Loader tape in the reader. Be sure that the leader (level 8 hole) is under the reader station.

7. Lift the HALT switch.

8. Depress and release the START-CLEAR switch and START CONT. The tape is now read into the computer.

9. When the tape is completely loaded, depress the HALT switch. The data display lights may be in any configuration because no checksum capability exists in the RIM Loader.

6.2.3 Loading Binary Tapes

1. Be sure that the BIN Loader program is stored in core memory (Paragraph 6.2.2).

2. Depress HALT.

3. If the extended memory option is installed, set SR switches 6–8 and 9–11 to desired IF field and DF field respectively and depress ADDR LOAD.

4. Set SR to 7777 and depress ADDR LOAD. The address set in SR is shown on MEMORY ADDRESS display.

5. Set SR to 3777 and load binary tape into reader by placing leader under reader station.

6. Be sure that PMK01 is on-line.

7. Lift the HALT switch and depress and release START-CLEAR and START-CONT.

8. The computer starts reading the tape in and stops when either loading is complete or there is a checksum error.

   - Loading Complete – the AC register displays all zeros and Link = 1. Additional binary tapes may be loaded by repeating steps 5 and 6 and depressing START-CONT.

   - Checksum Error – the AC register is not all zeros, indicating a checksum error has occurred in the previous block of data. In this case re-read the tape.

6.3 PDP-11 COMPUTER PROGRAM LOADING

6.3.1 Loading the Bootstrap Loader (DEC-11-L1PA-LA)

1. Set ENABLE/HALT switch to HALT to give bus control to the console when powering up.

2. Turn OFF/POWER/LOCK switch to POWER position. This energizes the programmer's console.

3. Enter starting address of Bootstrap Loader (Table 6-2) into switch register. Be sure that the correct xx value is used.

4. Set address display select switch to CONS PHY. (This step is performed only on PDP-11/45, 50 Computers.)

5. Depress LOAD ADRS switch. The address set in the switch register is shown on the ADDRESS display.

6. Enter starting address contents (016701) into switch register.

7. Lift DEP switch. The contents just entered in the switch register is displayed in the DATA display.

8. Enter contents of next address into switch register.

NOTE

It is not necessary to load addresses after the starting address has been loaded because the address is automatically incremented by two each time DEP is used consecutively.

9. Lift DEP switch.

10. Repeat steps 8 and 9 for each location of the Bootstrap Loader. When loading the contents of address xx7766, be sure that the correct device address (yyyyyy) is used.

11. The Bootstrap Loader program is now loaded in memory locations xx7744 through xx7776 and can be used to automatically load other programs into memory.

12. Correct program entry can be verified by examining the addresses between xx7744 and xx7776. This is accomplished by setting the starting address into the SR, depressing the LOAD ADRS switch and depressing the EXAM switch. The contents of the starting address are shown in the DATA display. Each time the EXAM is depressed again, the address is automatically incremented by two and the corresponding contents displayed.

NOTE

Step 12 alone (verification) may be sufficient if the Bootstrap Loader has already been loaded into the system. The program is stored in the uppermost portion of available memory so that it tends to survive program operation and is available for reloading programs. If the program is not intact, load according to this procedure, beginning with step 1.

Table 6-2
Bootstrap Loader
(DEC-11-L1PA-LA)

Address	Instruction
xx7744	016701
xx7746	000026
xx7750	012702
xx7752	000352
xx7754	005211
xx7756	105711
xx7760	100376
xx7762	116162
xx7764	000002
xx7766	xx7400
xx7770	005267
xx7772	177756
xx7774	000765
xx7776	yyyyyy*

*yyyyyy is determined by the type of paper-tape reader used to load the bootstrap formatted tapes

Teletype Paper-Tape Reader—177560
Higher Speed Paper-Tape Reader—177550

PMK01 is a high speed paper reader.

In Table 6-2, xx is determined by the address of the highest available memory bank and therefore varies with the memory size of the computer being programmed. See Table 6-3 below to determine xx for the Bootstrap Loader.

Table 6-3
xx Assignments

xx	Memory Size
01	4K
03	8K
05	12K
07	16K
11	20K
13	24K
15	28K

6.3.2 Loading the Absolute Loader (DEC-11-L2PC-LA)

1. Set ENABLE/HALT switch to HALT.
2. Be sure that the Bootstrap Loader has been stored in core memory (Paragraph 6.3.1, step 12).
3. Enter starting address of Bootstrap Loader into switch register. The starting address is xx7744.
4. Depress LOAD ADRS switch. The address set in the SR is displayed in ADDRESS display.
5. Place the PMK01 on-line.
6. Place the Absolute Loader tape in the reader. Be sure that the special leader (a sequence of 351 punches) is under the reader station. Blank leader does not work.
7. Set ENABLE/HALT to ENABLE.
8. Depress START switch. The tape is now read into the computer and halts when the entire program is loaded.
9. When the tape is completely loaded, the DATA display lights may be in any configuration as no checksum capability exists in the Bootstrap Loader.

Any PDP-11 program punched in binary format may be loaded automatically by using the Absolute Loader. The Absolute Loader can be set up to select either an absolute or relocatable code. If a relocatable code is selected, the user may specify that the relocatable code start at a specific address or that the code start loading at the point the previous load stopped. The Absolute Loader also provides a checksum test to ensure accurate loading. Although the computer normally stops when the binary tape is loaded, instructions on the tape itself may cause the computer to begin execution of the program immediately after loading is finished. This action is beyond the control of the user because it is a part of the program on certain binary tapes.

6.3.3 Loading Binary Tapes (using the Absolute Loader)

1. Be sure that the Absolute Loader program is stored in core memory (Paragraph 6.3.2).
2. Set ENABLE/HALT switch to HALT.
3. Enter starting address of Absolute Loader into SR. The starting address is xx7500.
4. Depress LOAD ADRS switch. The starting address of the Absolute Loader is now displayed in ADDRESS display.
5. Select the type of load desired by setting the SR as specified in Table 6-4.
6. Be sure that the PMK01 is on-line.

NOTE

The reading device may be changed at any time by the user without reloading the Absolute Loader. If a reader is to be changed, simply replace the contents of address xx7776 with the appropriate device status address (y value in Table 6-2).

7. Load desired binary tape into reader by placing leader under the reader station.
8. Set ENABLE/HALT switch to ENABLE.
9. Depress START switch. This begins the binary tape load.
10. If the binary tape contains a transfer address instruction, the computer begins execution of the program as soon as loading is complete.
11. The computer stops when either loading is complete or there is a checksum error.

    - Loading Complete – The low-order (right-hand) byte displayed in the DATA indicators is zero. Additional binary tapes may be loaded by repeating steps 5 through 7 and depressing the CONT switch.
    - Checksum Error – The low-order byte displayed in the DATA indicators is not zero, thereby indicating a checksum error has occurred in the previous block of data. In this case, reposition the tape in front of the error-producing block and depress the CONT switch.

6.3.4 Loading the Maintenance Loader

The Maintenance Loader (MAINDEC-11-D8EA) should only be used to load diagnostic programs if the Absolute Loader malfunctions due to a hardware failure. To load the Maintenance Loader:

1. Set ENABLE/HALT switch to HALT and depress START to clear the system.
2. Be sure that the Bootstrap Loader has been stored in memory.

NOTE

The Maintenance Loader operates in the lowest 8K of memory. If some other memory area must be used, several program locations must be changed as listed in Table 6-5 after the maintenance program is loaded.

Table 6-4
Binary Tape Load Selection
(using Absolute Loader)

Type of Load	Switch Register Settings	
	Bits 15–01	Bit 00
Normal (absolute)	Not applicable	0
Relocatable (continue where left off)	0	1
Relocatable (load at specified address)	Offset from tape origin	1

3. Set SR to xx7744 and depress LOAD ADRS.

4. Place the PMK01 on-line.

5. Place the Maintenance Loader tape in paper-tape reader.

6. Set ENABLE/HALT switch to ENABLE and depress START. The tape is read into memory and the processor halts when the entire program has been loaded.

NOTE

If the Maintenance Loader was not loaded into the lowest 8K of memory, make location changes at this time (Table 6-5).

Table 6-5
Relocation of Memory Contents

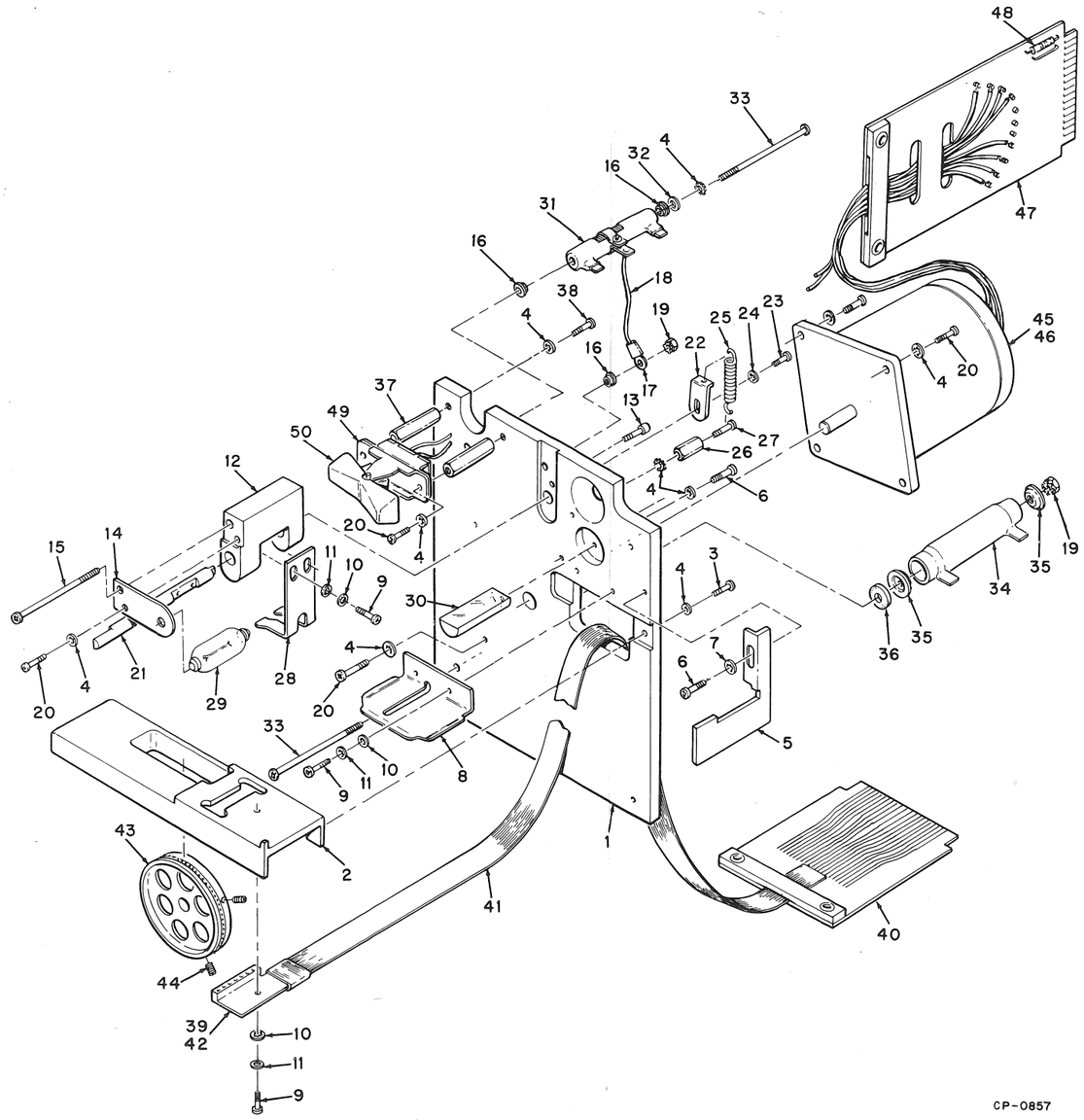
Move Contents of	To
xx7502	xx7470
xx7510	xx7474
xx7542	xx7475
xx7566	xx7475
xx7624	xx7776
xx7674	xx7474

Where xx equals:
01 for 4K memory
03 for 8K memory
05 for 12K memory
07 for 16K memory
11 for 20K memory
13 for 24K memory
15 for 28K memory

APPENDIX A
READER PLATE ASSEMBLY
ILLUSTRATED PARTS BREAKDOWN

Table A-1
Parts Identification

Item No.	Description	DEC Part No.
	READER PLATE ASSEMBLY	70-06573-03
1	Plate, Reader	74-07711-00
2	Guide, Tape Path	74-07690-00
3	Screw, Phl Hd Pan No. 6-32 x 1/2	90-06024-01
4	Washer, Int Tooth No. 6	90-06633-00
5	Slide, 8 Level	74-07826-00
6	Screw, Phl Hd Pan No. 6-32 x 1/4	90-06020-01
7	Washer, Ext Tooth No. 6	90-07649-00
8	Bracket, Tape Hold Down	74-07144-00
9	Screw, Phl Hd Pan No. 2-56 x 3/16	90-06000-01
10	Washer, Flat No. 2	90-08877-00
11	Washer, Int Tooth No. 2	90-06631-00
12	Block, Reader (Nylon)	74-07119-00
13	Screw, Soc Hd Cap No. 6-32 x 1/2	90-07937-00
14	Spring, Bulb	74-07116-00
15	Screw, Phl Hd Pan No. 6-32 x 1-3/4 Lg.	90-06031-01
16	Washer, Fiber No. 6	90-07632-00
17	Connector, Solderless	90-07929-00
18	Tracer, No. 18 AWG Strd. Tef. (Red/Gry)	91-07410-28
19	Nut, Keps No. 6	90-06560-00
20	Screw, Phl Hd Pan No. 6-32 x 3/8	90-06022-01
21	Shaft, Reader Plate	74-07120-00
22	Arm, Spring	74-07118-00
23	Screw, Phl Hd Pan No. 4-40 x 1/4	90-06009-01
24	Washer, Int Tooth No. 4	90-06632-00
25	Spring, Over Center	12-09863-00
26	Spacer, 1/4 AF x No. 6-32 x 5/16 Lg.	90-06842-00
27	Screw, Phl Hd Pan No. 6-32 x 3/4 Lg.	90-06026-01
28	Depressor, Tape	74-07719-00
29	Bulb, Osram No. 6475	12-04734-00
30	Lens	74-04989-01
31	Resistor, Ohmite 25 Ohm 12W (R1)	13-10134-00
32	Washer, Flat	90-06656-00
33	Screw, Phl Hd Pan No. 6-32 x 2-1/4 Lg.	90-07851-00
34	Resistor, 15 Ohm 25W (R2)	13-00181-00
35	Washer, Centering	90-06674-00
36	Washer, Fiber (Added)	90-08076-00
37	Spacer, Threaded 1/4 AF x No. 6-32 x 7/8 Lg.	90-06861-00
38	Screw, Phl Hd Pan No. 6-32 x 5/8 Lg.	90-06025-01
39	PHOTOTRANSISTOR ASSEMBLY	70-06267-00
40	Connector, Cable (W077)	W077
41	Flexprint (11 Conductor)	91-05692-02
42	Phototransistor Assembly	54-09227-00
43	Sprocket	74-04975-00
44	Screw, Soc Hd Set No. 6-32 x 1/4 Lg.	90-06291-00
45	MOTOR ASSEMBLY	70-06603-03
46	Motor	12-03530-01
47	Connector, Cable (W023)	W023
48	Resistor, 1K Ohms, 1/4W 5% (Added)	13-00365-00
49	Switch, RS-9, Momentary	12-05375-00
50	Button, Rocker Switch (Russet Orange)	12-05317-09



CP-0857

APPENDIX B
DIAGNOSTIC PROGRAMS

The following diagnostic programs are provided with the PMK01:

LIBKIT 8E-PC8E-01

High-Speed Reader/Punch Tests	
Document	MAINDEC-8E-D2CA-D
Binary Paper Tape	MAINDEC-8E-D2CA-PB

LIBKIT-11-PC11-0-6

PC11 Reader and Punch Tests	
Document	MAINDEC-11-DZPCA-C-D
Binary Paper Tape	MAINDEC-11-DZPCA-C-PB
Special Binary Count Tape	MAINDEC-00-D2G4-PT*
Alternate Ones and Zeros	MAINDEC-00-D2G2-PT*

*These tapes may also be used on the PDP-8E/8F/8M computer systems.

APPENDIX C
ENGINEERING DRAWING SET

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

THIS IS PRINT SET

SEQUENCE		SEQUENCE	
DRAWING DIRECTORY	B-DD-PMKØ1-Ø		
PORTABLE READER	D-UA-PMKØ1-Ø-Ø		
MODULE UTILIZATION	C-MU-PMKØ1-Ø-1		
MODULE UTILIZATION (P.L.)	A-PL-PMKØ1-Ø-1		
WIRE LIST	B-WL-PMKØ1-Ø-2		
WIRED ASSY	D-AD-7009669-0-0		
BOARD JUMPER	D-IA-9305647-0-0		
CABLE, D.C. POWER	C-IA-9305632-0-0		
+30 VOLT SUPPLY	B-CS-G835-Ø-1		
PHOTO TRANSISTOR AMP	C-CS-G918-Ø-1		
SOLENOID DRIVER	B-CS-MØ6Ø-Ø-1		
READER CLOCK	C-CS-M715-YA-1		
PC11 CONTROL	D-CS-M781Ø-Ø-1		
READER/PUNCH CONTROL	E-CS-M84Ø-YA-1		
READER CONTROL	D-CS-M7Ø5Ø-YA-1		
CONNECTOR WØ23	B-CS-WØ23-Ø-1		
ENGINEERING SPEC(MAINT.)	A-SP-PMKØ1-Ø-3		
OPERATING PROC.	A-SP-PMKØ1-Ø-4		

UNIT VARIATIONS

VAR	TITLE	PRINT SET PMKØ1-Ø
PMKØ1-AA	PDP 8/E CONTROL 115V	X
PMKØ1-AB	PDP 8/E CONTROL 230V	X
PMKØ1-BA	PDP 11/15-20 CONTROL 115V	X
PMKØ1-BB	PDP 11/15-20 CONTROL 230V	X
PMKØ1-CA	PDP 8/E & PDP/11/15-20 CONT.115V	X
PMKØ1-CB	PDP 8/E & PDP 11/15-20 CONT.230V	X

REVISIONS | REV | CHG. NO. | DATE

USED ON OPTION/MODEL: PMKØ1

		DATE
DRN.	D.SCHMIDT	10/16/72
CHK'D.	J.DEVIN	12/11/72
PROJ ENG.	[signature]	5/6/74
PROD.	[signature]	050374
FIELD SERV.		

TITLE: PORTABLE READER (PMKØ1)

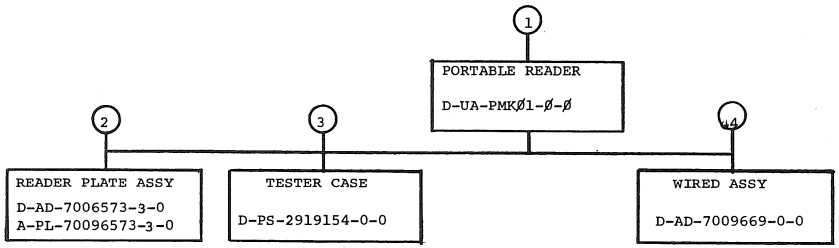
SIZE: B | CODE: DD | NUMBER: PMKØ1-Ø | REV:

DIST:

SHEET 1 OF 3

DRB 106

DEC 14-12251-1062-1A-R972



TITLE		SIZE	CODE	NUMBER	REV
PORTABLE READER	SHEET 2 OF 3	B	DD	PMKØ1-Ø	

DRB 107
DEC 16—(325)—1062—3—N871

ELECTRICAL

CUSTOMER PRINT SET PMKØ1-Ø	MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
X		1	B-DD-PMKØ1-Ø		3	DRAWING DIRECTORY	
X			C-MU-PMKØ1-Ø-1		1	MODULE UTILIZATION	
X			A-PL-PMKØ1-Ø-1		1	MODULE UTILIZATION (P.L.)	
X			E-WL-PMKØ1-Ø-2		1	WIRE LIST	
X			B-CS-G835-Ø-1		1	+30 VOLT SUPPLY AMPLIFIER	
X			C-CS-G918-Ø-1		1	PHOTO TRANSISTOR	
X			B-CS-MØ6Ø-Ø-1		1	SOLENOID DRIVER	
X			C-CS-M715-YA-1		1	READER CLOCK	
X			D-CS-M781Ø-Ø-1		3	PC11 CONTROL	
X			E-CS-M840-YA-1		3	READER/PUNCH CONTROL	
X			D-CS-M7Ø5Ø-YA-1		1	READER CONTROL	
X			B-CS-WØ23-Ø-1		1	CONNECTOR WØ23	
X			D-IA-9305647-0-0		1	BOARD,JUMPER	
X			A-SP-PMKØ1-Ø-3		18	ENG. SPEC. MAINT.	
X			A-SP-PMKØ1-Ø-4		17	OPERATING PROC.	
X		4	D-AD-7009669-0-0		1	WIRED ASSY	

MECHANICAL

CUSTOMER PRINT SET PMKØ1-Ø	MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
X		1	D-UA-PMKØ1-Ø-Ø		2	PORTABLE READER	
			D-MD-9605883-0-0		1	PLATE,BASE	
X			C-IA-9305632-0-0		1	CABLE,DC,POWER	
			C-IA-9605712-0-0		1	BRKT,TESTER CHASSIS	
			C-MD-9605889-0-0		1	ACCESSORY SEPERATOR	
			B-UA-H851-Ø-Ø		1	CONN.EDGE H851	
			D-UA-BCØ8J-Ø-Ø		1	I/O CABLE(BCØ8J)	
			D-UA-BCØ8K-Ø-Ø		1	I/O CABLE (BCØ8K)	
		2	D-AD-7006573-3-0		1	READER PLATE ASSY	
X			A-PL-7006573-3-0		3	READER PLATE ASSY(P.L.)	
		3	D-PS-2919154-0-0		2	CASE TESTER	
			D-MD-9605886-0-0		1	HINGE,BASE PLATE	
			B-IA-9605885-0-0		1	SUPPORT BASE PLATE	
		4	D-AD-7009669-000		1	WIRED ASSY	
			D-SC-1205348-0-0		1	CONN,BLOCK 288 PIN	
			C-MD-9605884-0-0		1	FRAME CASTING 1943(REWORK)	
			C-MD-9605979-0-0		1	BLOCK RETAINER UNIV.(REWORK)	

CUSTOMER PRINT SET CODES

X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE	SHEET 3 OF 3	SIZE	CODE	NUMBER	REV
PORTABLE READER		B	DD	PMKØ1-Ø	

DRB 108

DEC 16-(325)-1062-2B-R972

WIRE TABLE

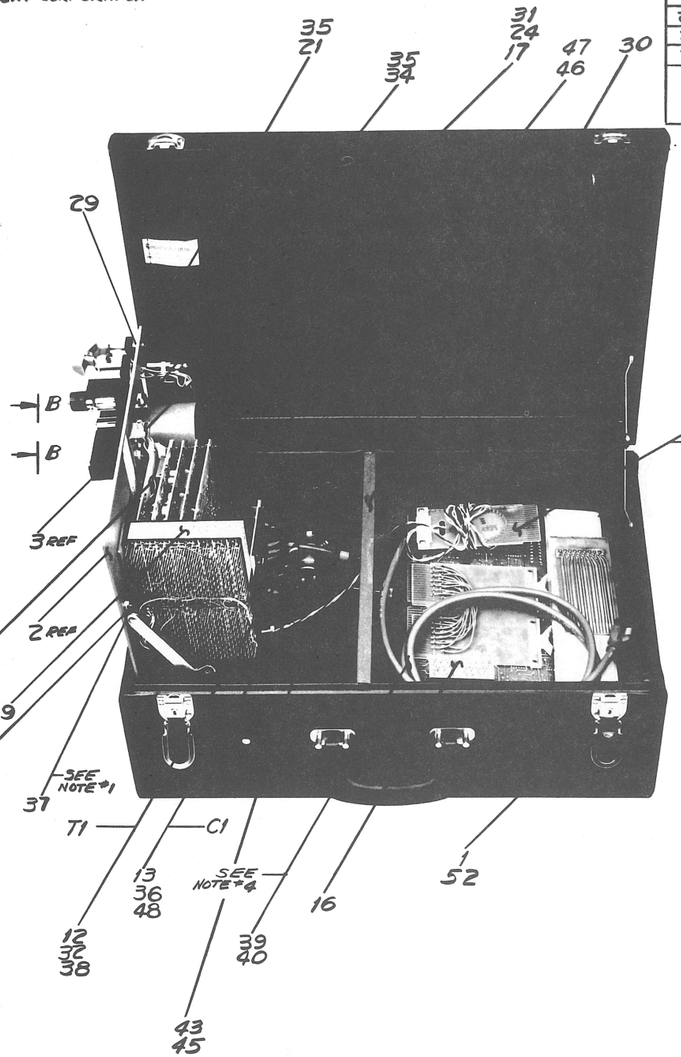
ITEM NO	DESCRIPTION COLOR	AWG	FROM CONN	WITH	TO CONN	WITH	REMARKS
27	BLK	22	T1-8	ITEM 32	B08V2	SOLDER	TRANS. OUTPUT
28	BLU	↓	T1-11	↓	B08R2	↓	↓
27	BLK	↓	C1(-)	↓	B08C2	↓	↓
29	GRY	22	C1(+)	ITEM 32	B08F2	↓	↓
8	BLK	LEAD	P1-C		A01C2	↓	GND
	WHT	LEAD	P1-B		A01B2	↓	-15VDC
	GRN/WHT	LEAD	P1-A		A01A2	SOLDER	+5VDC

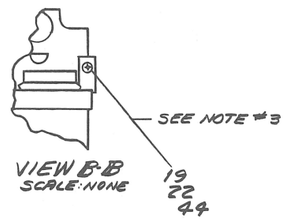
LEGEND

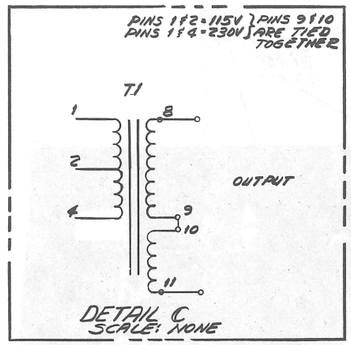
NUMBER	VARIATION	
PMKØ1-AA	PDP8/E CONTROL	115V
-AB	PDP8/E CONTROL	230V
-BA	PDP11/15-20 CONTROL	115V
-BB	PDP11/15-20 CONTROL	230V
-CA	PDP8/E & PDP11/15-20 CONTROL	115V
PMKØ1-CB	PDP8/E & PDP11/15-20 CONTROL	230V

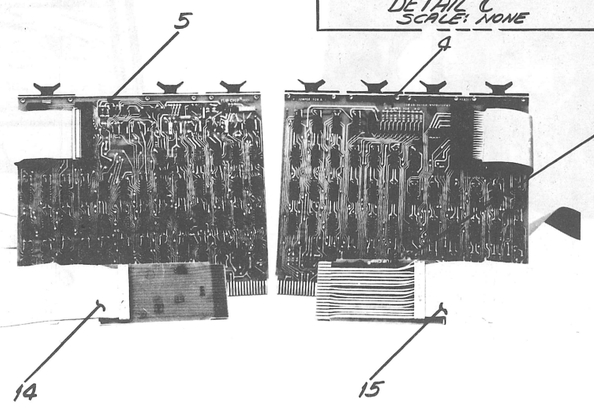
NOTES:

1. BASE PLATE AND READER PLATE ASSY WHEN IN OPEN LOCK POSITION, MUST BE PARALLEL TO THE SIDE OF THE CASE TO ACCOMPLISH THIS A SPACER MAY BE REQUIRED BETWEEN THE COLLAPSABLE HINGE AND BASE PLATE. USE ITEM 37 FOR SPACER.
2. ATTACH POWER CORD (ITEM 39 OR 40) TO TRANS. (ITEM 12) AND JUMPER TRANS. PER DETAIL 'C' FOR 115V AND 230V.
3. REMOVE .25 LG SCREW, REPLACE WITH .75 LG SCREW (ITEM 44)
4. GREEN WIRE OF POWER CORD TO GO TO TRANSFORMER GROUND AND BLK WIRE FROM TRANS. TO GO TO CHASSIS GROUND.









REVISIONS			REV.
DWR	CHANGE NO.	Re Rev #2 3-29-74 DJL	

DEC FORM NO. DRD 100-A

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PMKØI		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS: .XXX = .005, .XX = .02, .X = .1 — ANGLES: ±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL: SEE PARTS LIST

FINISH: —

DRN.		DATE 3-29-74
CH'D.		DATE
ENG.	R.D. Wetherbee	DATE 3-29-74
PROJ. ENG.	Harold Long	DATE 5/6/74
PROD.	Gadaire	DATE 050374

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PORTABLE READER (PMKØI)

NEXT HIGHER ASSY.: B-DD-PMKØI-Ø

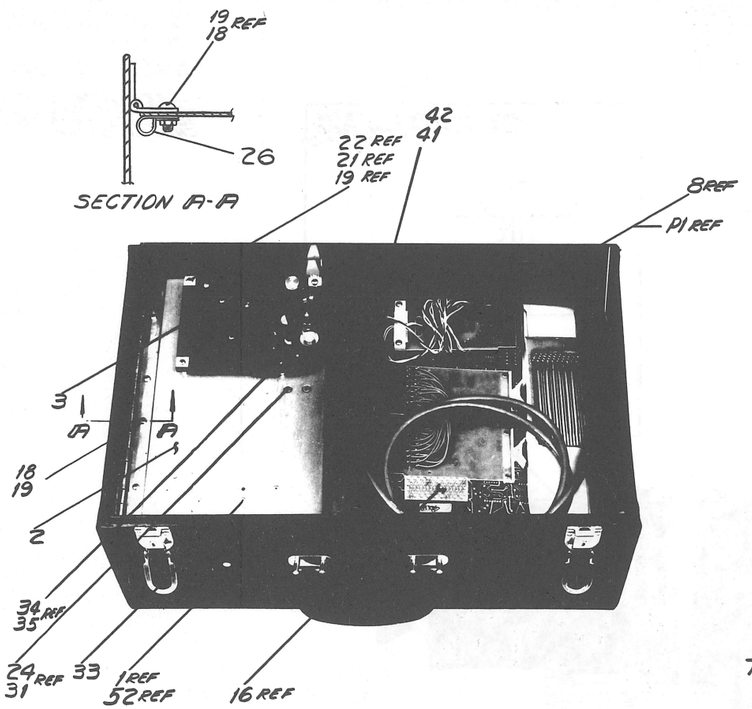
SCALE: —

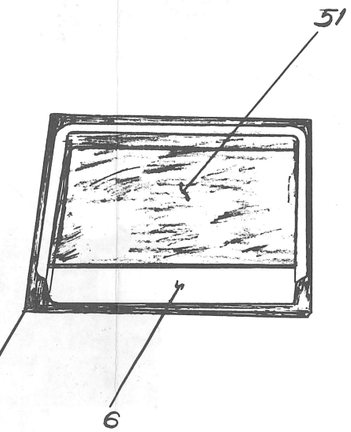
SHEET 1 OF 2

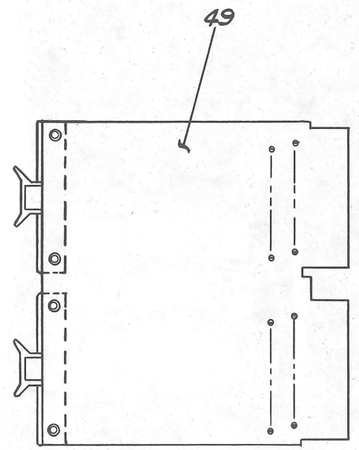
SIZE	CODE	NUMBER	REV.
D	UA	PMKØI-Ø-Ø	P03

DIST.

SIZE D CODE UA NUMBER PMKØI-Ø-Ø REV.







REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
PORTABLE READER	D	UA	PMKØ1-Ø-Ø	
SCALE —H— SHEET 2 OF 2	DIST.			

DEC FORM NO. DRD 138

LEGEND	
NUMBER	VARIATION
PMKØI- A	SEE PARTS LIST
PMKØI- B	SEE PARTS LIST

NOTES:
1. ASTERISK (*) INDICATES MODULES USED ON PMKØI-B, NOT USED ON PMKØI-A.

	1	2	3	4	5	6	7	8
	WØ23	G918	MØ6Ø	M7Ø5Ø-YA*	M715-YA*	9305647*		
	CABLE							
A	CONN BOARD	PHOTO TRANSISTOR AMPLIFIER	SOLENOID DRIVER	READER CONTROL	READER CLOCK	JUMPER BOARD		
	WØ77							G835
	CABLE							
B	CONN BOARD							+30 VOLT SUPPLY

REVISIONS			
	CHANGE NO.		REV.
CHK			PØ2
	4/20/73		

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PMKØI		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS: .xxx = .005, .xx = .02, .x = .1 | ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY √

MATERIAL
FINISH

		DATE
DRN.	B. Manchester	1-2-73
CHK'D	H. Chester	1-8-73
ENG.	Badaire	02-73
PROJ. ENG.	Badaire	02-73
PROD.	Badaire	02-73

NEXT HIGHER ASSY. D-UA-PMKØI-Ø-Ø
SCALE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
MODULE UTILIZATION

SIZE	CODE	NUMBER	REV.
C	MU	PMKØI-Ø-1	PØ2

DIST.

DEC FORM NO. DRF 1***-B

C-7

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY R. HUTNAK	CHECKED R. Hutnak	SECTION
DATE 11/28/72	DATE 11/28/72	1
ENG	PROD	ISSUED SECT.
DATE	DATE	1

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION PMKØ1-A	PMKØ1-B
1	G835	+3O VOLT SUPPLY	1	1
2	G918	PHOTO TRANSISTOR AMP	1	1
3	MØ6Ø	SOLENOID DRIVER	1	1
4	M715-YA	READER CLOCK	-	1
5	M7Ø5Ø-YA	READER CONTROL	-	1
6	D-IA-9305647-0-0	JUMPER BOARD (WØ25)	-	1

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
MODULE UTILIZATION	C-MU-PMKØ1-Ø-1	A	PL	PMKØ1-Ø-1		
	SHEET 1 OF 1	DIST.				

DEC FORM DEC 16-(325)-1031-N870
DRA 110

FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PMKØ1		PARTS LIST		

REVISIONS	REV.	CHANGE NO.	CHK

DRN. J. Devin	DATE 4-4-74	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. J. Devin	DATE 4-4-74	
ENG. Ron Pelletier	DATE 4/27/74	TITLE: WIRE LIST (PMKØ1)
PROJ. ENG. Harold Long	DATE 5/6/74	
PROD. Ron Pelletier	DATE 4/27/74	
NEXT HIGHER ASSEMBLY: B-DD-PMKØ1-Ø		SIZE K / CODE WL / NUMBER PMKØ1-Ø-2 / REV.
SCALE None		
SHEET 1 OF 1		DIST.

DEC FORM NO. DRB 109

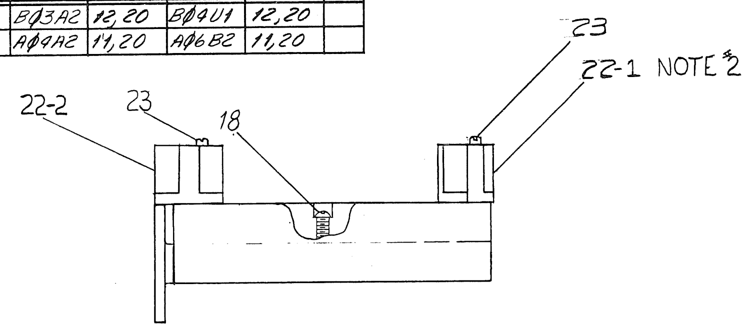
C-9

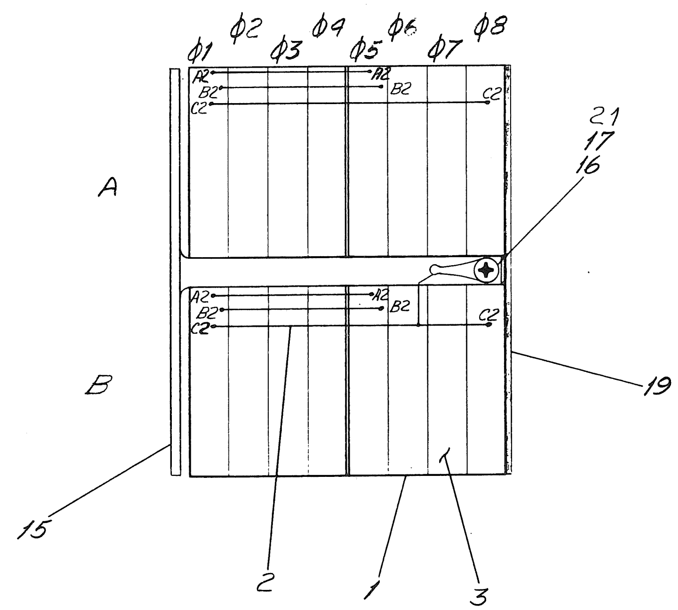
EXTERNAL COMP. LIST

ITEM	COMP	POL	FROM	WITH	TO	WITH	POL
13	RES		BØ3A2	12,20	BØ4U1	12,20	
14	RES		AØ4A2	11,20	AØ6B2	11,20	

NOTES:

1. CONNECTIONS ON ITEM #2 #13 & #14 TO BE LOCATED AT MINIMUM PRACTICAL HEIGHT ABOVE BLOCK
2. REFER TO C-MD-%05979-0-0





PARTS LIST

QTY.	DESCRIPTION	PART NO.	ITEM NO.
2	SCREW, PHL FILL HD #8-32X1½	9007799-5	23
1	BLOCK RETAINER (1 & 2)	C-MD-9605979	22
1	WIRE LIST (PMKØ1)	A-WL-PMK01-0-2	REF
1	WASHER INT TOOTH #8	9006034	21
4	CLIP TERMI PT. 85952-3	9007655	20
A/R	TAPE, FOAM GREY 1" X ⅛ THK	9008228	19
2	SCREW, PHL FILL HD #8-32 X ⅝ LG	900[illegible]10-[illegible]	18
1	SCREW, PHL PAN HD #8-32 X ¼ LG.	9006035-1	17
1	TERM #2104-08-04 SHAKE PROOF	9006766	16
1	FRAME CAST, 1943 (RE WORK)	C-MD-9605889-0-0	15
1	RES, 470 Ω ¼W 5%	1300316	14
1	RES, 100 Ω ¼W 5%	1300229	13
A/R	TUB, #22 AWG TEFFLON (BRN)	9107256-01	12
A/R	TUB, #22 AWG TEFFLON (BLU)	9107256-06	11
—	—	—	10
—	—	—	9
—	—	—	8
—	—	—	7
—	—	—	6
—	—	—	5
—	—	—	4
A/R	WIRE #30 SOLID KYNAR (BLU)	9105740-66	3
A/R	BUSS STRIP	1205541	2
2	CONN BLK, 288 PIN	1205398	1

REVISIONS		
CHK	CHANGE NO.	REV.
	12/20/72 ECN	PØ1
	2/12/73 ...	

FIRST USED ON OPTION/MODEL: PMKØ1

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL: SEE PARTS LIST

FINISH: —

DRN. D. Schmidt — DATE 9-18-72
CHK'D — DATE 12/2/73
ENG. R. Pillster — DATE 5-8-74
PROJ. ENG. — DATE 5/6/74
PROD. — DATE 050374

NEXT HIGHER ASSY. D-UA-PMKØ1-Ø-Ø

SCALE / SHEET OF

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: WIRED ASSY (PMKØ1)

SIZE	CODE	NUMBER	REV.
D	AD	7009669-0-0	PØ3

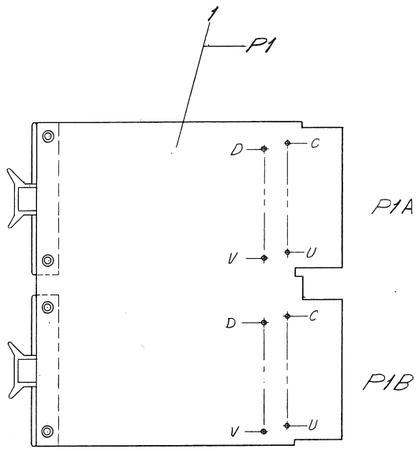
DIST.

BRUNING 40-107 15968

DEC FORM NO DRD 100-A

WIRE TABLE

ITEM NO	DESCRIPTION COLOR	AWG	FROM CONN	FROM WITH	TO CONN	TO WITH	REMARKS
2	BLU	#24	P1A-D	SOLD	P1B-D	SOLD	
			-E		-E		
			-F		-F		
			-H		-H		
			-J		-J		
			-K		-K		
			-L		-L		
			-M		-M		
			-N		-N		
			-P		-P		
			-R		-R		
			-S		-S		
			-T		-T		
2	BLU	#24	P1A-V	SOLD	P1B-V	SOLD	



QTY.	DESCRIPTION	PART NO.	ITEM NO.
A/R	WIRE #24 AWG TFE-K FLU	31-741-03	2
1	MODULE, WIRE (W. HANDLE)	V.S.E.	1

PARTS LIST

FIRST USED ON OPTION/MODEL: PMKØ'

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL: SEE PARTS LIST

FINISH: — —

		DATE
DRN	[illegible]	9-28-73
CHKD	[illegible]	10/17/73
ENG	[illegible]	5-2-74
PROJ. ENG.	[illegible]	5/6/74
PROD	[illegible]	5/28/74

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: BOARD, JUMPER

NEXT HIGHER ASSY.: D-UA-PMKØI-Ø-Ø

SCALE: 1/1

SHEET | OF |

SIZE	CODE	NUMBER	REV.
D	IA	9305647-0-0	PØ1

DIST.

REVISIONS			
CHK.	CHANGE NO.		REV.
RM	1421-73		P01

BRUNING 40-107 15868

DEC FORM NO DRD 100-A

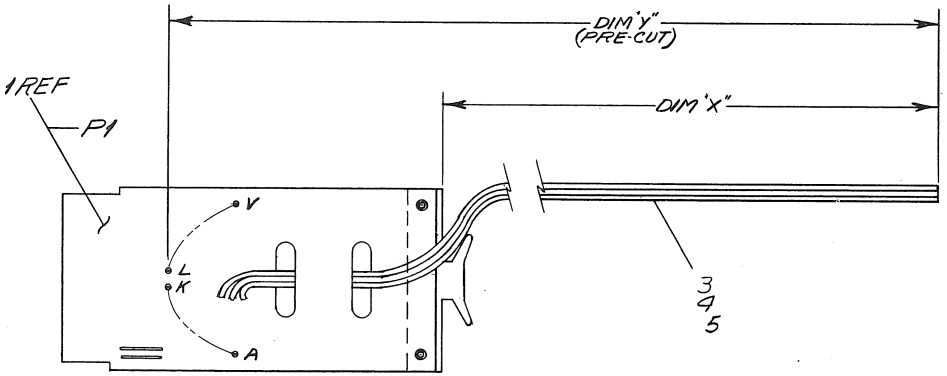
SIZE CODE D IA | NUMBER 9305647-0-0 | REV. P01

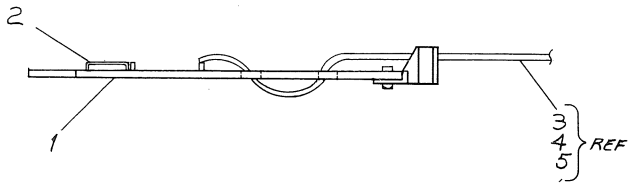
WIRE TABLE

ITEM NO.	DESCRIPTION COLOR	AWG	FROM CONN	WITH	TO CONN	WITH	REMARKS
4	ORN/WHT	#22	P1-A	SOLD.	—	—	
5	WHT	#22	P1-B	SOLD.	—	—	
3	BLK	#22	P1-C	SOLD.	—	—	

LEGEND

DWG. NO.	DIM 'X' VARIATION	DIM 'Y' (PRE-CUT)
9305632-9	9.0 FT.	9.0 FT.-4.0 IN.





PARTS LIST

ITEM NO.	QTY.	DESCRIPTION	PART NO.
5	A/R	WIRE, #22 AWG I.P.V.C (WHT)	9107350-99
4	A/R	WIRE, #22 AWG I.P.V.C (ORN/WHT)	9107400-93
3	A/R	WIRE #22 AWG IPVC (BLK)	9107350-00
2	A/R	WIRE BUSS #22 AWG	9107560-01
1	1	MODULE, W023 (W/HANDLE)	W023

FIRST USED ON OPTION/MODEL: PMKØI

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: .XXX = .005, .XX = .02, .X = .1
ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL: SEE PARTS LIST
FINISH: — / —

		DATE
DRN.	D. Schmidt	9-14-72
CHK'D.	D.E. Hatch	1-8-73
ENG.	Hadaii	4-21-73
PROJ. ENG.	[illegible]	5/4/73
PROD.	Hadaii	4-21-73

NEXT HIGHER ASSY.: D-UA-PMKØI-Ø-Ø
SCALE: NONE
SHEET: 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: CABLE, DC POWER (PMKØI)

SIZE	CODE	NUMBER	REV.
C	IA	9305632-0-0	PØ1

DIST.

REVISIONS

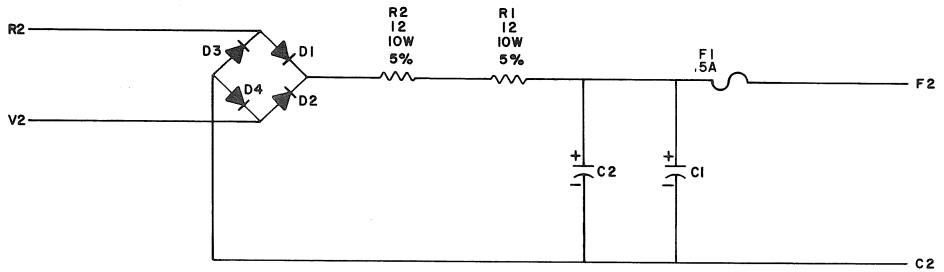
REV.	CHANGE NO.	CHK

BRUNING 40-107 15968

DEC FORM NO. DRC 100-A

C-13

SIZE	CODE	NUMBER	REV.
B	CS	G835-0-1	



UNLESS OTHERWISE INDICATED:
DIODES ARE IN4003
CAPACITORS ARE 50UF, 50V, -10+75%
F1 IS A 1209159 FUSE

REVISIONS	REV.	CHG NO.	CHK

DRN.	A. Cooper	DATE 10/19/70
CHKD	L. Waldis	DATE 11/20/70
ENG	A. Marku	DATE 12-4-70
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: +30 VOLT SUPPLY G835

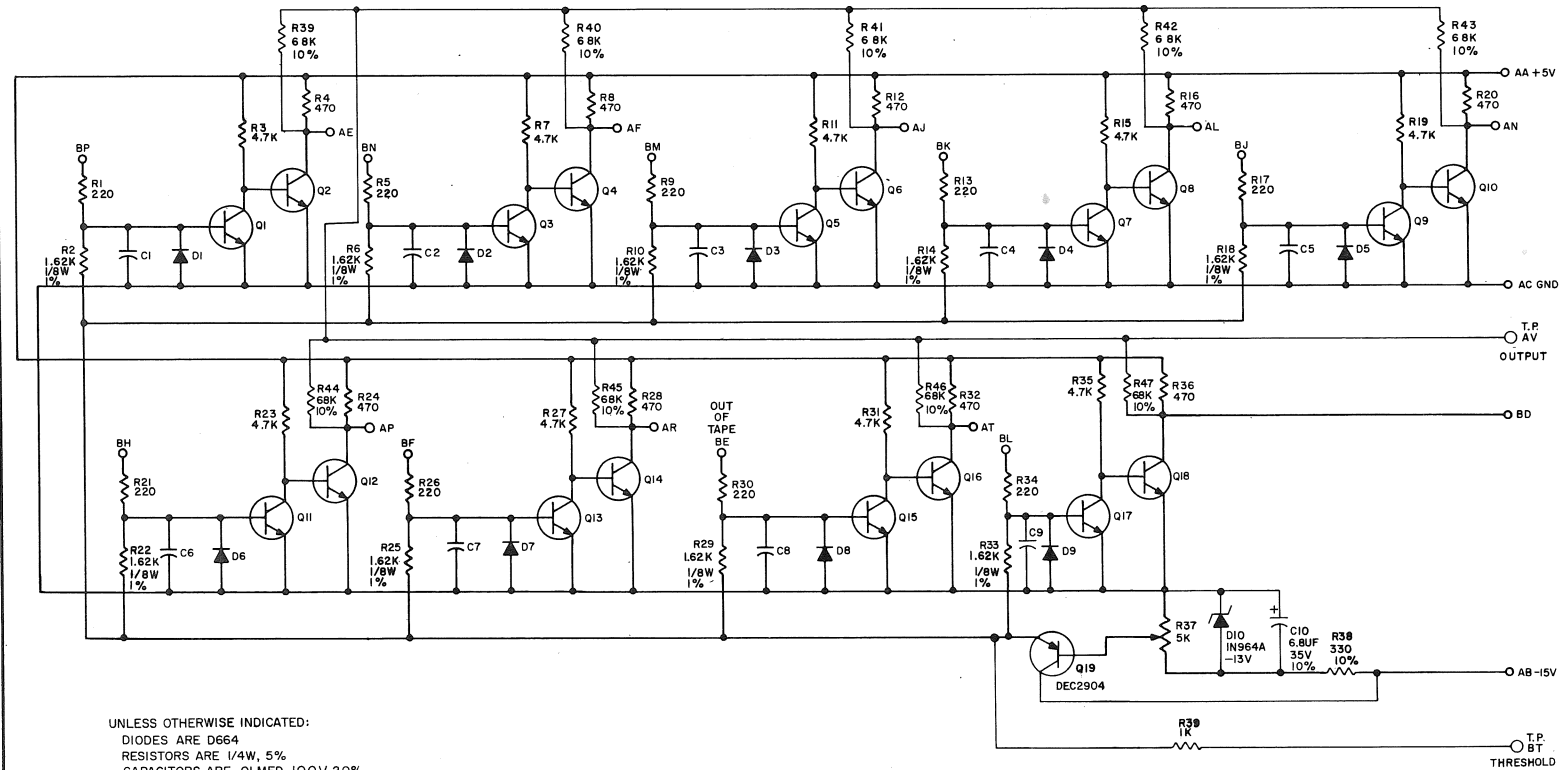
SIZE	CODE	NUMBER	REV.
B	CS	G835-0-1	

PRINTED CIRCUIT REV. A

DEC FORM NO. DRB 102

DIST. 324,434,435

5 Print



UNLESS OTHERWISE INDICATED:
DIODES ARE D664
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE .01 MFD, 100V, 20%
TRANSISTORS ARE 2N3646

○ INDICATES TEST POINT

REVISIONS			
CHK	CUSTOMER NO.	REV.	
	00000	A	
	00000	B	

DRN.	R.BUTLER	DATE 4/11/69
CHK'D	S. Young	DATE 4/29/69
ENG.	R. Abel	DATE 6/11/69
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
2N3646	2N3009	IN964A-13V	SAME
D664	IN3606	DEC2904	2N1132

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PHOTO TRANSISTOR AMPLIFIER G918

SIZE	CODE	NUMBER	REV.
C	CS	G918-0-1	B

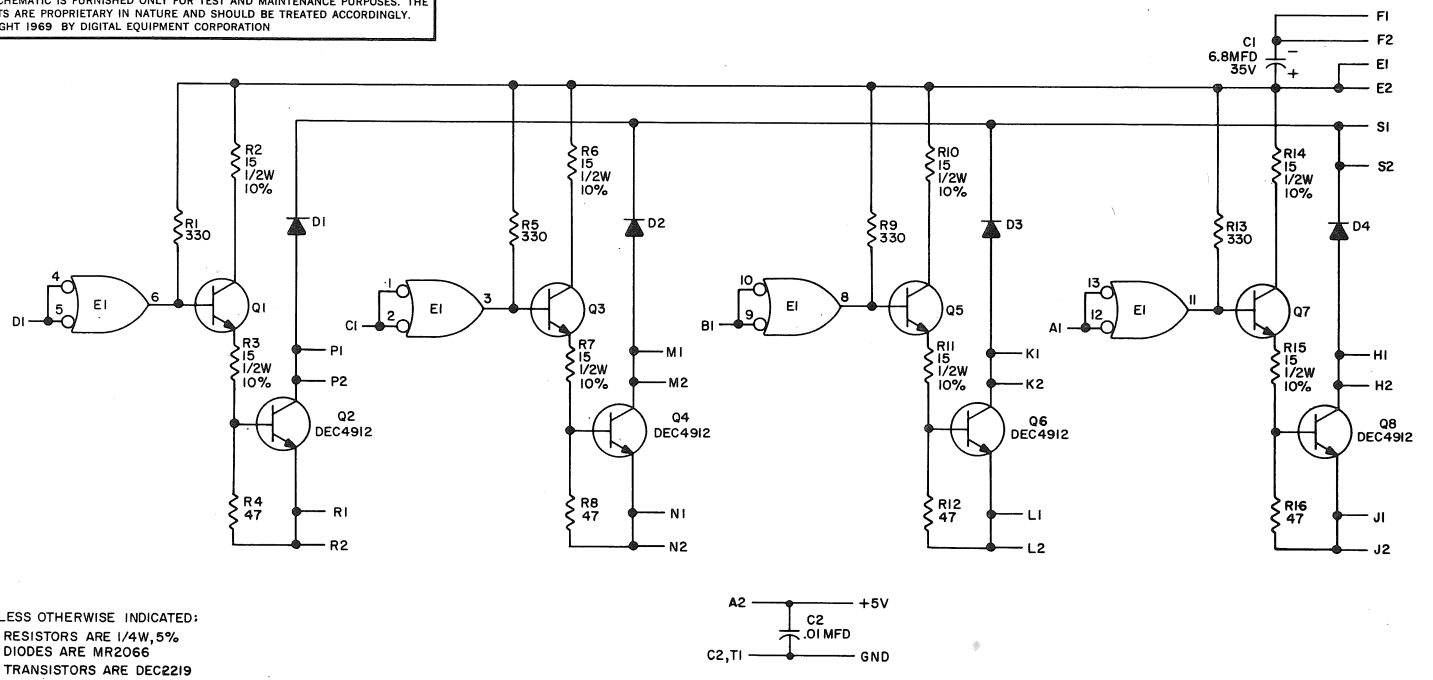
PRINTED CIRCUIT REV. D

DEC FORM NO. DRC 102

5 DIST. 324,434,435 PINK

SIZE C | CODE CS | NUMBER G918-0-1 | REV. B

SIZE	CODE	NUMBER	REV.
B	CS	M060-0-1	



UNLESS OTHERWISE INDICATED:
- RESISTORS ARE 1/4W, 5%
- DIODES ARE MR2066
- TRANSISTORS ARE DEC2219
- PIN 7 ON EACH IC = GND
- PIN 14 ON EACH IC = +5V
- E1 IS DEC7400N

REVISIONS	CHK	CHG NO.	REV.

		DATE
DRN.	BUTLER	9/12/69
CHK'D.	P.A. Holette	9/15/69
ENG.	D. Vogelsang	11/10/69
PROD.		

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
MR2206	IN4003		
DEC2219	SAME		
DEC4912	NONE		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: SOLENOID DRIVER M060

SIZE	CODE	NUMBER	REV.
B	CS	M060-0-1	

PRINTED CIRCUIT REV. A

DEC FORM NO. DRB 102

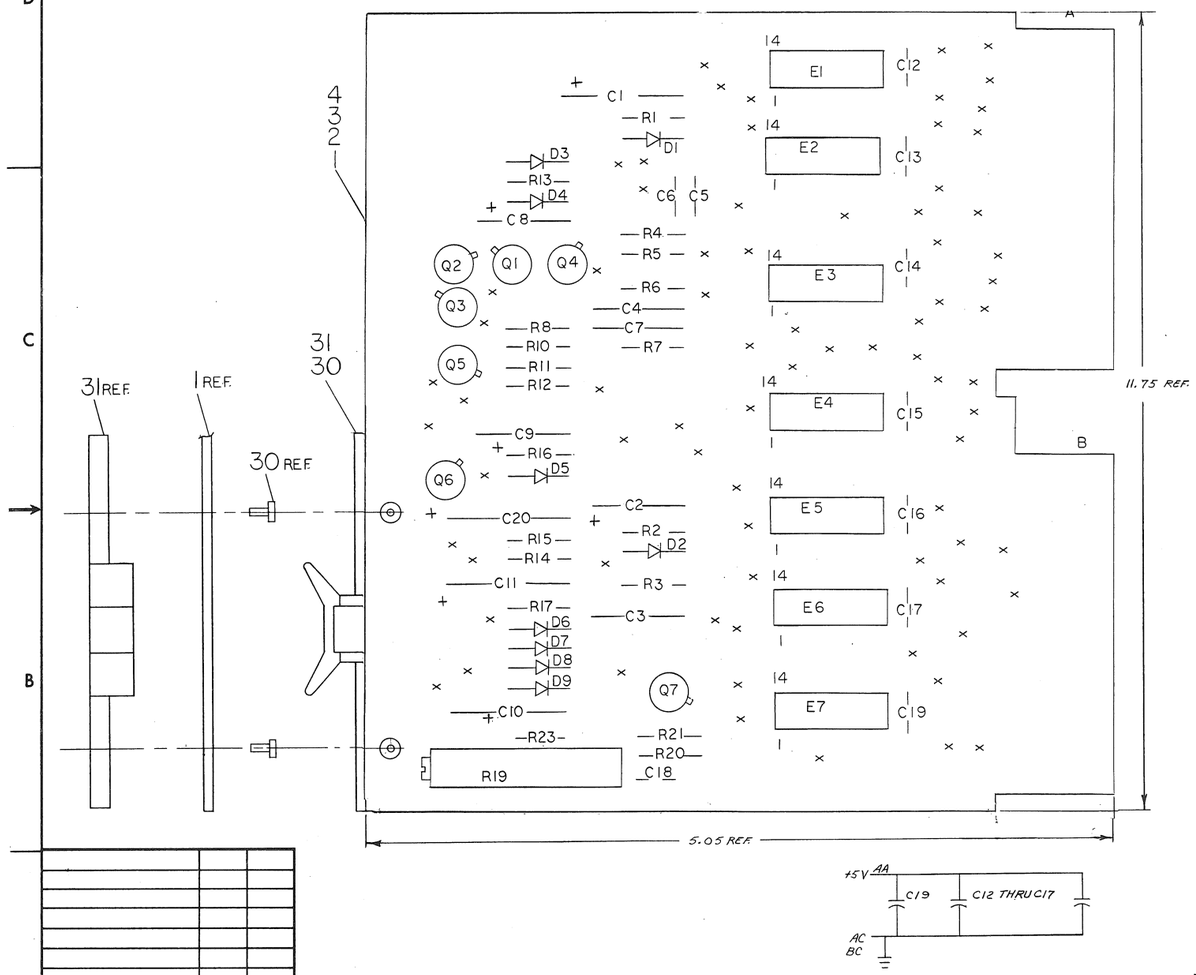
5

DIST: 324, 434, 435 3

PINK

NOTES:

1. UNLESS OTHERWISE NOTED:
   RESISTANCE IS IN OHMS,
   CAPACITANCE IS IN PICOFARADS



IC TYPE	GND	+ 5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE		

IC PIN LOCATIONS

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
2	R10,R11	RES. 2K 1/4W 5%	1302388	34
2	C8,C9	CAP. 1.5UF 35V 10% TANT	1009725	33
1	C6	CAP. .005UF	1001765	32
2		HANDLE FLIP CHIP - MAGENTA	9008397-06	31
4		EYELETS #GS4-7 STIMPSON	9006732	30
76		FEED THRU EYELETS	9006731	29
1	E9	IC. DEC. 7404	1909686	28
2	E2,E5	IC. DEC. 9601	1909373	27
1	E7	IC. DEC. 7402	1909004	26
3	E1,E6,E3	IC. DEC. 7400	1905575	25
1	Q7	TRANSISTOR MPS. 6531	1509338	24
6	Q1 THRU Q6	TRANSISTOR DEC 6534-D	1503409	23
1	R19	POTENTIOMETER 1K	1305450	22
1	R1	RES. 20K 1/4W 5%	1302391	21
1	R2	RES. 7.5K 1/4W 5%	1301422	20
1	R15	RES. 330 1/4W 5%	1300295	19
5	R8,R12,R13,R14,R16	RES. 3K 1/4W 5%	1300432	18
1	R23	RES. 15K 1/4W 5%	1300391	17
1	R21	RES. 1K 1/4W 5%	1300365	16
1	R20	RES. 470 1/4W 5%	1300316	15
5	R3 THRU R7	RES. 220 1/4W 5%	1300271	14
1	R17	RES. 47 1/4W 5%	1300202	13
9	D1 THRU D9	DIODE DG64	1100114	12
3	C1,C10,C20	CAP. 6.8UF 35V 10% STANT	1005306	11
2	C5,C18	CAP. 1000 PF 100V 5% D.M.	1002344	10
1	C2	CAP. 1.0UF 35V 10% S. TANT	1001776	9
7	C12 THRU C17,C19	CAP. .01UF 100V 20% DISC	1001610	8
1	C11	CAP. 33UF 10V 10% S.TANT	1000076	7
2	C3,C7	CAP. 680 PF 100V 5% D.M.	1000026	6
1	C4	CAP. 220 PF 100V 5% D.M.	1000021	5
REF		MODULE ECO HISTORY	B-MH-M715-YA-6	4
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M715-YA-5	3
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M715-YA-4	2
1		ETCHED CIRCUIT BOARD	5004521	1

PARTS LIST

FIRST USED ON OPTION MODEL: PMK Ø1

ETCH BOARD REV: F

DEC NO.	EIA NO.	DEC NO.	EIA NO.
DEC 6531	MPS 6531		
DEC DG64	IN3606		
DEC 6534D	MPS 6534		

SEMICONDUCTOR CONVERSION CHART

REVISIONS: CHANGE NO. / REV / CHK

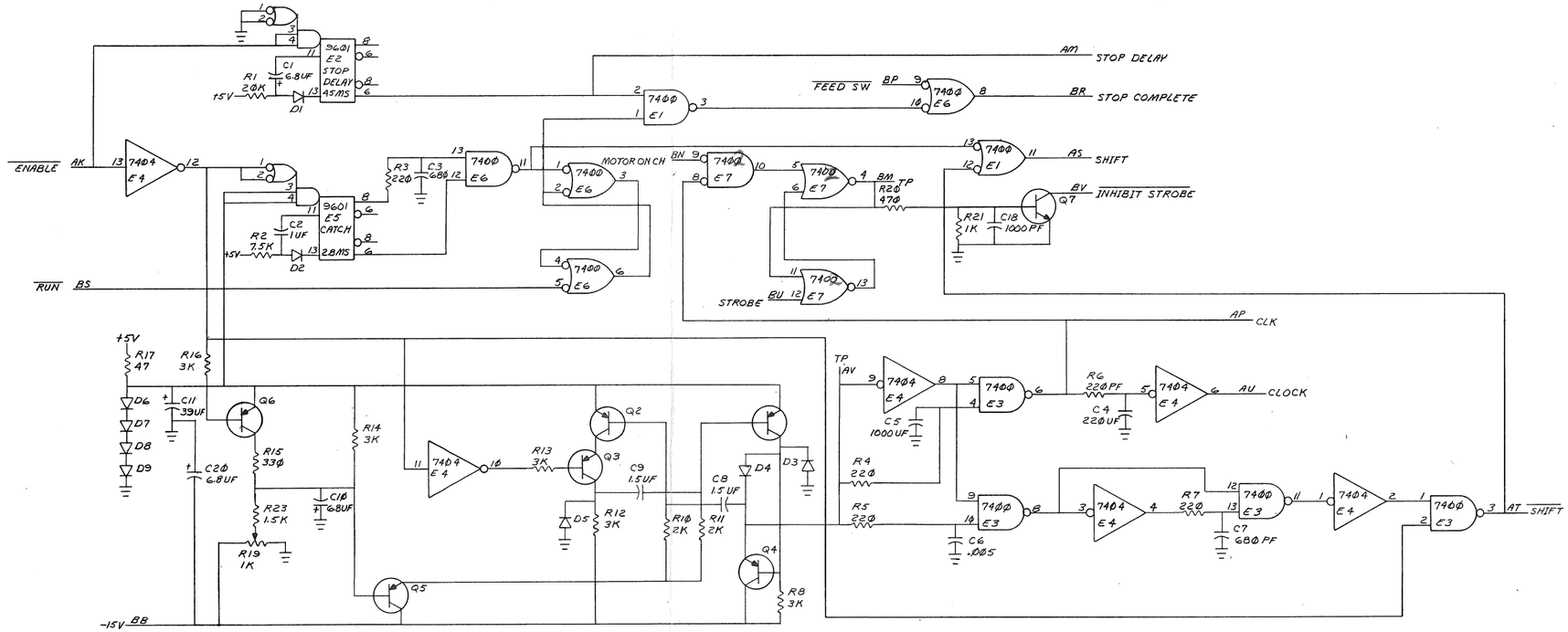
DRN. G. Manchester DATE 7-18-72
CHK'D. David Fales DATE 8/8/72
ENG. A. Cole DATE 10-2-72
PROJ. ENG. A. Cole DATE 10-9-72
PROD. Bob Lemay DATE 10-9-72
NEXT HIGHER ASSY: D-UA-PMKØ1-Ø-Ø
SCALE: 1/1
SHEET 1 OF 2

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: READER CLOCK M715-YA

SIZE D | CODE CS | NUMBER M715-YA-1 | REV.
DIST.

BRUNING 40-522 16699
DEC FORM NO. FRD-135A



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —

FINISH —

DRN	B Manchester	DATE 9-15-72
CHK'D		DATE 9-19-72
ENG.		DATE 10-1-72
PROJ ENG.		DATE 10-1-72
PROJ.		DATE 10-9-72

NEXT HIGHER ASSY. —

SCALE —

SHEET 2 OF 2

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: READER CLOCK M715-YA

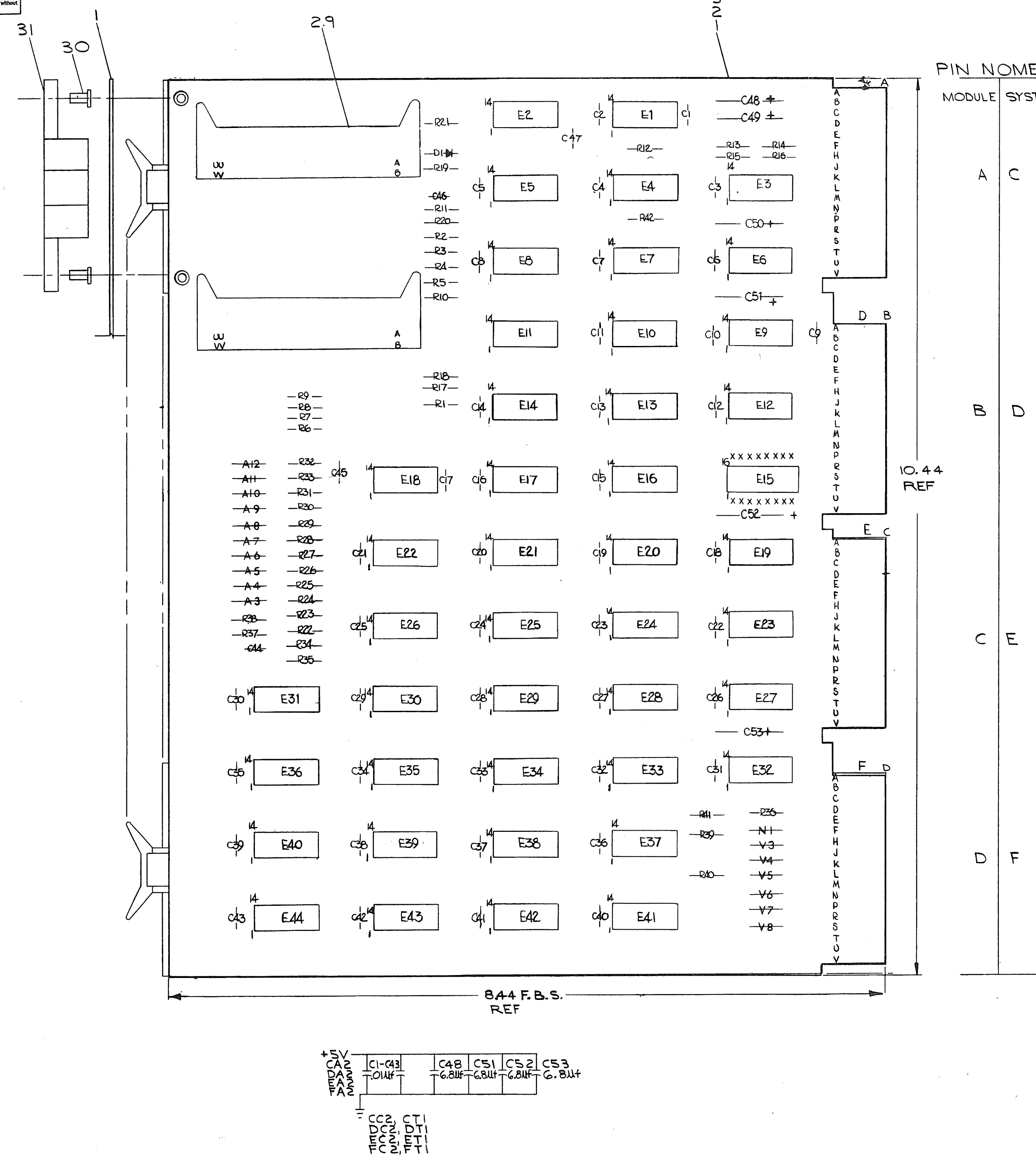
SIZE	CODE	NUMBER	REV.
D	CS	M715-YA-1	

DIST.

REV.	REVISIONS	CHANGE NO.	CHK

BRUNING 40-522 15840

DEC FORM NO DRD 102-B



PIN NOMENCLATURE

MODULE	SYSTEM UNIT
A	C
B	D
C	E
D	F

NOTES:

1.) PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE SYSTEM UNIT. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE LEFT.

2.) JUMPERS TO BE USED AT CONNECTIONS A3-A12, N1, AND V3-V8.

3.) ON ITEM NO. 19 ALL 10 CHIPS MUST BE EITHER DEC 380's OR ITS' SUBSTITUTE 11380 IC's. COMBINATIONS ARE NOT ALLOWED ON THE SAME OPTION.

ALLOWABLE SUBSTITUTION LIST

ORIG. PART NO.	SUBSTITUTE DESCRIPTION	PART PART NO.	ITEM NO.
1903485	IC. 11380	1911113	19

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
25	R1, R11, R12, R14, R16, R18-R2Ø, R22-R34, R37, R39, R41, R42	RES 1K 1/4W 5%	1300365	33
1		I.C. SOCKET	1209838	32
4		HANDLE, FLIP CHIP MAGENTA	9008337-06	31
8		EYELET #GS-4-7 . STIMPSON	9006732	30
2		BERG 40 PIN CONNECTOR	1209941	29
2	E38, E42	I.C. DEC 74H74	1909667	28
2	E35, E44	I.C. DEC 7408	1910155	27
2	E28, E36	I.C. DEC 7402	1909004	26
1	E25	I.C. DEC 74HØØ	1909056	25
3	E22, E26, E3Ø	I.C. DEC 8242	1909712	24
2	E21, E29	I.C. DEC 8815	1909713	23
9	E8-E1Ø, E13, E16-E18, E39, E43	I.C. DEC 7400	1905575	22
2	E7, E34,	I.C. DEC 7474	1905547	21
9	E3-E5, E12, E14, E31, E33, E37, E41	I.C. DEC 8881	1909705	20
10	E1, E2, E6, E11, E19, E2Ø, E23, E24, E27, E32	I.C. DEC 380	1909405 *	19
1	E4Ø	I.C. DEC 74HØ4	1909931	18
1	R38	RES 47 1/4W 5%	1300202	17
1	R36	RES 390 1/4W 5%	1300309	16
1	R21	RES 4.7K 1/4W 5%	1300447	15
1	R17	RES 220 1/4W 5%	1300271	14
3	R13, R15, R35	RES 100 1/4W 5%	1300229	13
9	R2-R1Ø	RES 470 1/4W 5%	1300316	12
1	R4Ø	RES 180 1/4W 5%	1301322	11
1	D1	DIODE D664	1100114	10
6	C48-C53	CAPACITOR 6.8 MFD 35V 20%	1000067	9
2	C46, C47	CAPACITOR 680 PF 1ØØV 5%	1000026	8
1	C45	CAPACITOR 470 PF 1ØØV 5%	1000024	7
1	C44	CAPACITOR 330 PF 1ØØV 5%	1000023	6
43	C1-C43	CAPACITOR .01 MFD 1ØØV 20%	1001610	5
REF		MODULE E.C.O. HISTORY	B-MH-M781Ø-Ø-6	4
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M781Ø-Ø-5	3
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M781Ø-Ø-4	2
1		ETCHED CIRCUIT BOARD	5009882	1

PARTS LIST

ETCH BOARD REV: C, D

* SEE ALLOWABLE SUBSTITUTION LIST & NOTE #3.

IC TYPE	GND	+5V
DEC 380	1	8

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

ITEM NO.	AWG	FROM PT	TO PT

JUMPER LIST

REV	CHANGE NO.	CHK
C	M7810-00001	S. Marcean 6-20-72
D	M7810-00002	H. Denamore 7-3-73

REVISIONS

DEC NO.	EIA NO.	DEC NO.	EIA NO.
D664	IN3606		

SEMICONDUCTOR CONVERSION CHART

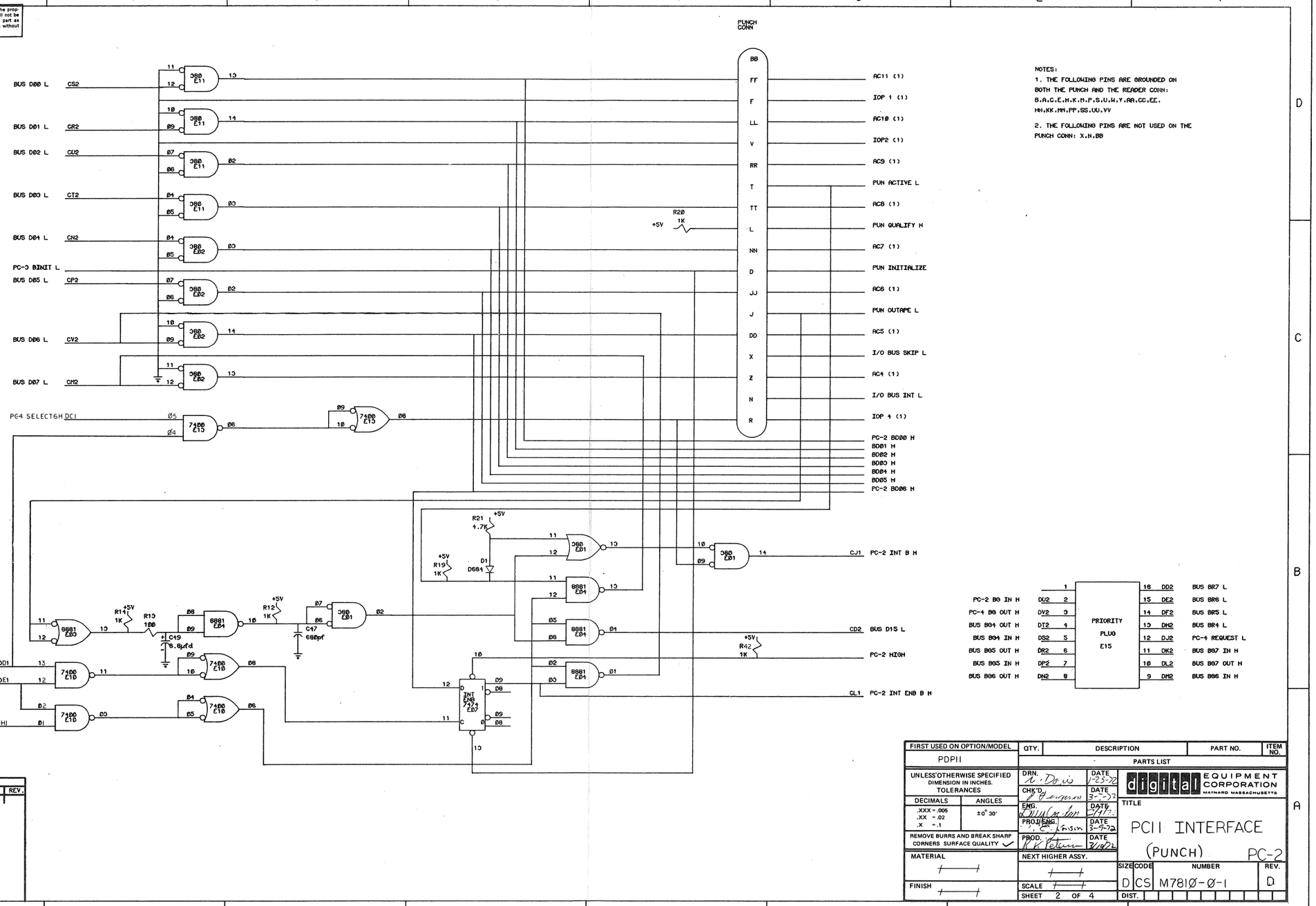
DRN. G. Marini DATE 1/31/72
CHK'D. J. Ferguson DATE 3-3-72
ENG. Larry Gordon DATE 3/9/72
PROJ. ENG. R. E. Janson DATE 3-9-72
PROD. R. K. Peterson DATE 3/10/72
NEXT HIGHER ASSY
SCALE NONE
SHEET 1 OF 4

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PC11 INTERFACE PC-1

SIZE E | CODE CS | NUMBER M781Ø-Ø-1 | REV. D

DEC FORM NO. DRE 104

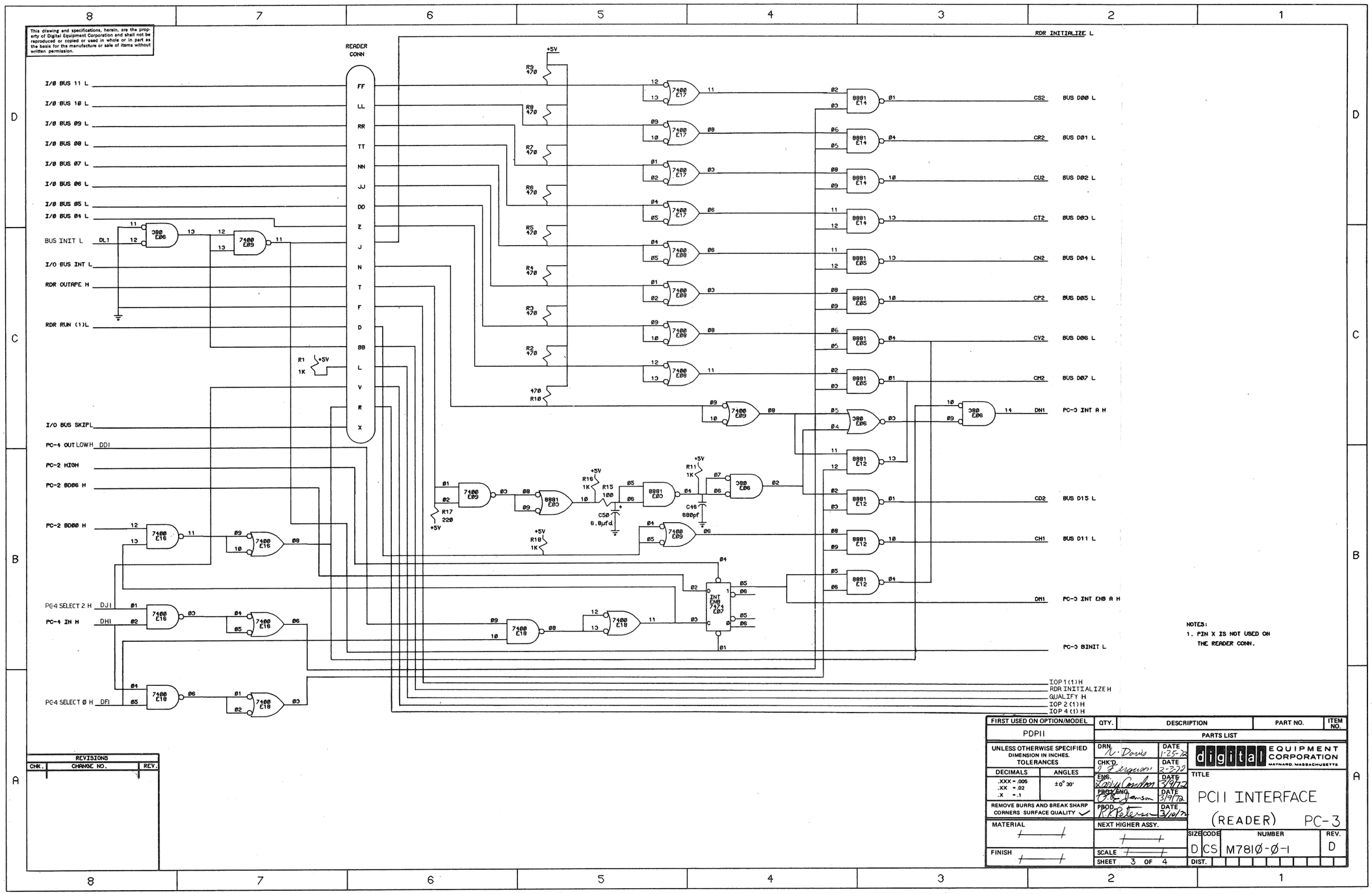


NOTES:
1. THE FOLLOWING PINS ARE GROUNDED ON BOTH THE PUNCH AND THE READER CONN: B,A,C,E,H,K,M,P,S,U,W,Y,AA,CC,EE, HH,KK,MM,PP,SS,UU,VV

2. THE FOLLOWING PINS ARE NOT USED ON THE PUNCH CONN: X,N,BB

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL: PDP11	QTY.	DESCRIPTION: PARTS LIST	PART NO. / ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES. DECIMALS: .XXX = .005, .XX = .02, .X = .1; ANGLES: ±0° 30'. REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	DRN. N. Davis 1-25-72; CHK'D G. Jorgensen 3-7-72; ENG. W. Wilcox 2/17/72; PROJ/ENG. C. Larson 3-9-72; PROD. K. Peters 3/10/72	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS	
MATERIAL: —	NEXT HIGHER ASSY.	TITLE: PCII INTERFACE (PUNCH) PC-2	
FINISH: —	SCALE: —	SIZE D; CODE CS; NUMBER M7810-0-1; REV. D	
	SHEET 2 OF 4	DIST.	



REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO. / ITEM NO.
PDPII	PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

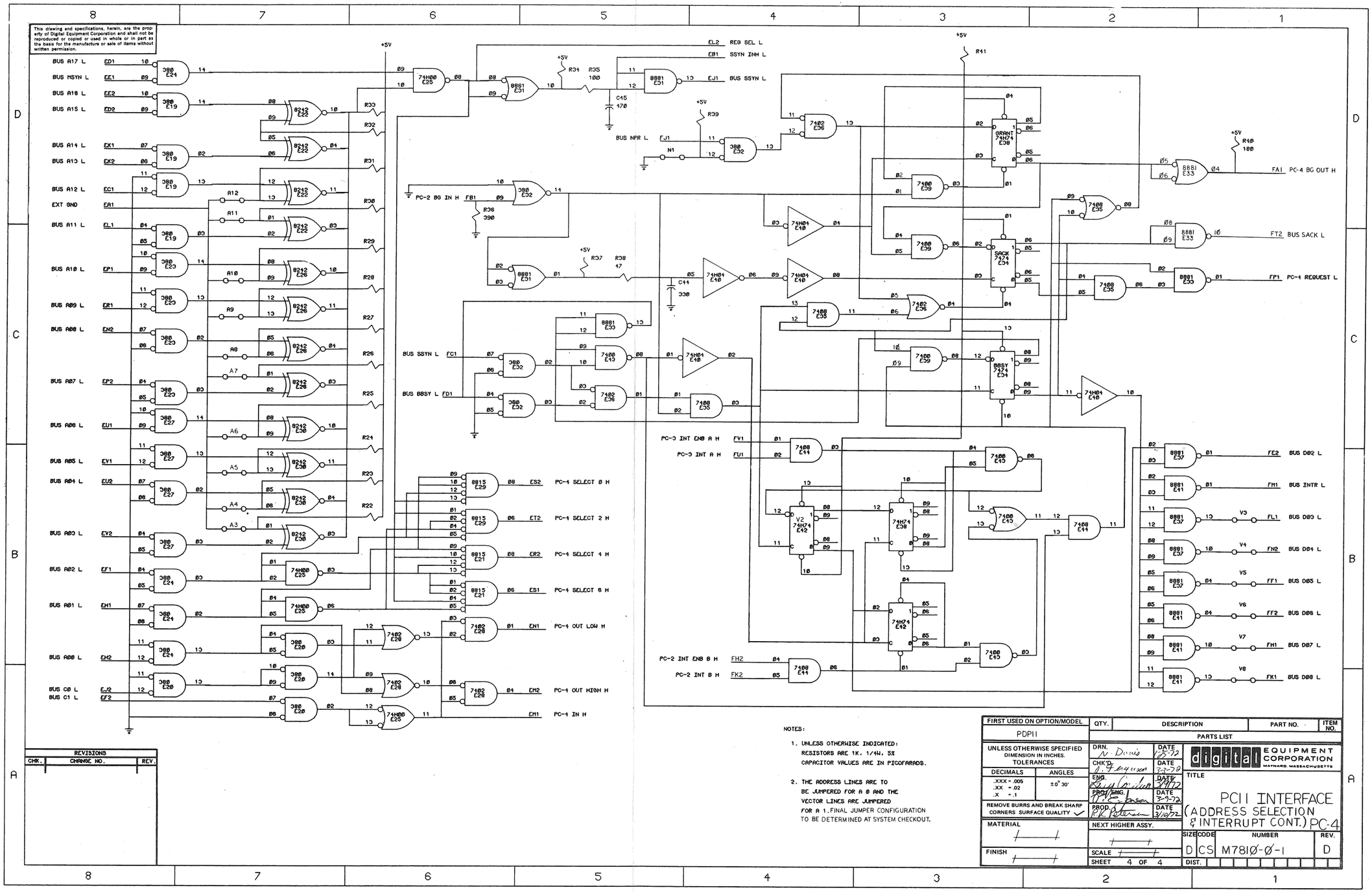
DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —/—

FINISH —/—

DRN. M. Davis	DATE 1-25-72	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D J. Ferguson	DATE 2-7-72	
ENG. Larry Condon	DATE 3/9/72	TITLE
PROJ. ENG. R. E. Hanson	DATE 3/9/72	PCII INTERFACE (READER) PC-3
PROD. R. K. Peterson	DATE 3/10/72	
NEXT HIGHER ASSY. —/—		SIZE D · CODE CS · NUMBER M781Ø-Ø-1 · REV. D
SCALE —/—		
SHEET 3 OF 4		DIST.



NOTES:

1. UNLESS OTHERWISE INDICATED:
   RESISTORS ARE 1K, 1/4W, 5%
   CAPACITOR VALUES ARE IN PICOFARADS.

2. THE ADDRESS LINES ARE TO BE JUMPERED FOR A 0 AND THE VECTOR LINES ARE JUMPERED FOR A 1. FINAL JUMPER CONFIGURATION TO BE DETERMINED AT SYSTEM CHECKOUT.

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP11		PARTS LIST		

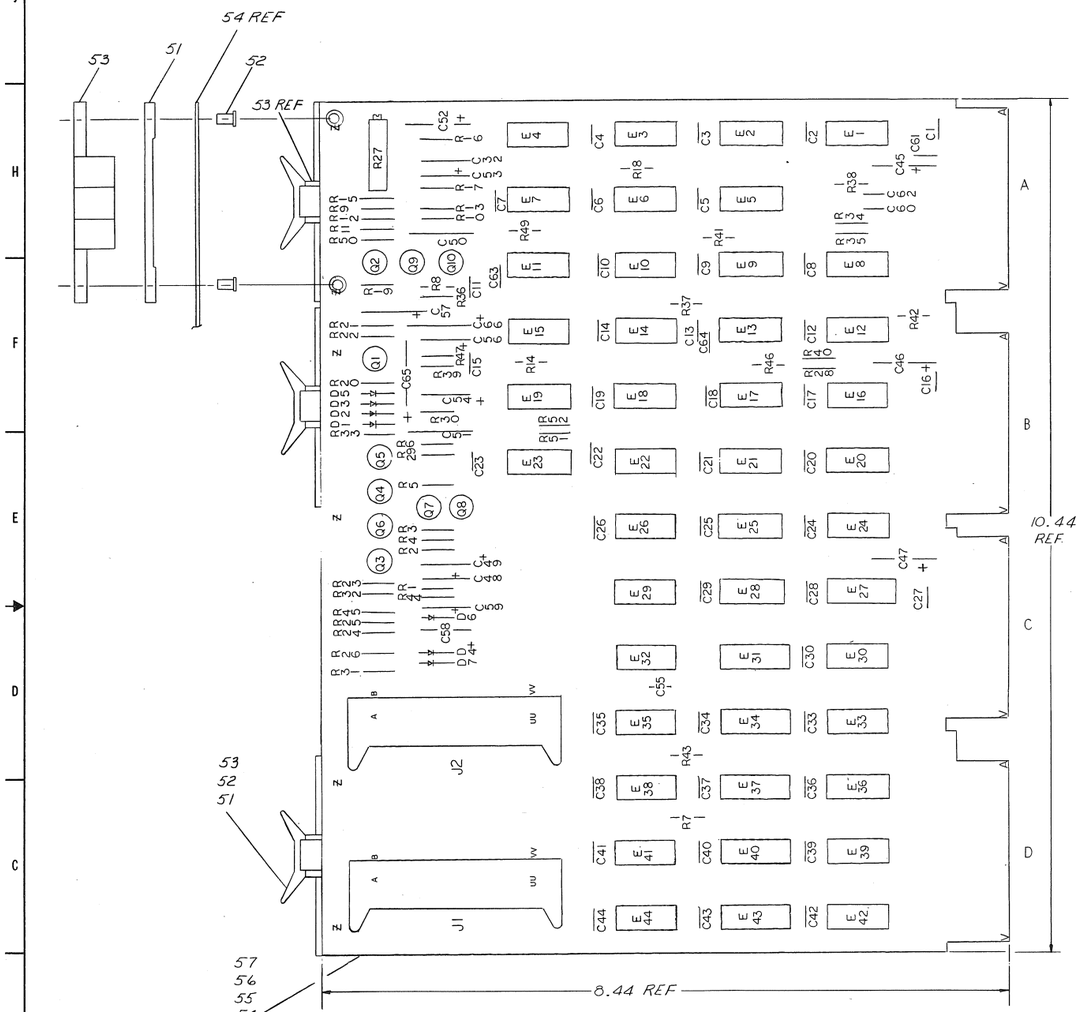
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES	DRN. N. Dennis	DATE 1/25/72
DECIMALS: .XXX = .005, .XX = .02, .X = .1 — ANGLES: ±0° 30'	CHK'D A. Ferguson	DATE 3-7-72
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	ENG. [illegible]	DATE 3/7/72
MATERIAL	PROJ. ENG. W. Cason	DATE 3-9-72
FINISH	PROD. R.K. Peterson	DATE 3/10/72
	NEXT HIGHER ASSY.	
	SCALE	
	SHEET 4 OF 4	

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PCII INTERFACE (ADDRESS SELECTION & INTERRUPT CONT.) PC-4

SIZE	CODE	NUMBER	REV.
D	CS	M7810-0-1	D

DIST.



QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	C55	CAP .005UF 100V 20% DISC	1001765	1
1	R44	RES 75 ¼W 5%	1302378	2
1	C61	CAP 1500 PF 250V 10% DISC	1000054	3
1	E35	IC DEC 7420	1905577	4
1	R49	RES 270 ¼W 5%	1301972	5
1	R9	RES 5.6K ¼W 5%	1301874	6
1	R13	RES 150 ¼W 5%	1300250	7
1	R8	RES 56 ¼W 5%	1302602	8
1	R21	RES 680 ¼W 5%	1301424	9
1	R47	RES 18K ¼W 10%	1300498	10
2	J1, J2	CONN 40 PIN RT ANGLE HEADER	1209941	11
4	E34,E37,E40,E43	IC DEC 8271	1909615	12
2	E27, E31	IC DEC 8251	1909594	13
4	E17,E18,E33,E39	IC DEC 8881	1909705	14
2	E21, E25	IC DEC 6314	1909972	15
5	E20,E24,E30,E36,E42	IC DEC 380	1909485	16
7	E3,E8,E26,E29,E38,E41,E44	IC DEC 7404	1909886	17
4	E4,E7,E15,E19	IC DEC 9601	1909373	18
1	E16	IC DEC 384	1909488	19
2	E1,E11	IC DEC 7410	1905576	20
7	E5,E6,E13,E22,E23,E28,E32	IC DEC 7400	1905575	21
5	E2,E9,E10,E12,E14	IC DEC 7474	1905547	22
2	Q7,Q8	TRANSISTOR DEC 6531	1509338	23
8	Q1-Q6,Q9,Q10	TRANSISTOR DEC 6534-D	1503409-00	24
7	R1,R4,R6,R18,R34,R38,R51	RES 220 ¼W 5%	1300271	25
20	R7,R28,R11,R12,R14,R15, R19,R20,R23,R24,R26,R31, R32,R37,R40-R43,R22,R52	RES 3K ¼W 5%	1300432	26
1	R27	RES 1K ¼W 10% 76PR	1300143-07	27
1	R17	RES 7.5K ¼W 5%	1301422	28
1	R16	RES 15K ¼W 5%	1300496	29
2	R39,R30	RES 12K ¼W 5%	1300488	30
2	R36,R46	RES 10K ¼W 5%	1300479	31
2	R2,R3	RES 4.7K ¼W 5%	1300447	32
1	R50	RES 1.5K ¼W 5%	1300391	33
1	R35	RES 330 ¼W 5%	1300295	34
2	R5, R10	RES 100 ¼W 5%	1300229	35
2	R29,R33	RES 47 ¼W 5%	1300202	36
3	D4,D6,D7	DIODE D664	1100114	37
4	D1,D2,D3,D5	DIODE D662	1100113	38
41	C1-C21,C33-C44,C23,C30	CAP .01UF 100V 20% DISC	1001610	39
6	C45-C47,C54,C57,C66	CAP 6.8UF 35V 10% TANT	1005306	40
2	C50,C51	CAP .01UF 100V 10% MILAR	1005784	41
2	C48,C49	CAP .33UF 20V 10% TANT	1005328	42
1	C52	CAP 15UF 20V 10% TANT	1004612	43
1	C56	CAP 2.2UF 20V 10% TANT	1002622	44
3	C53,C58,C59	CAP 1UF 35V 10% TANT	1001776	45
1	C65	CAP.39UF 10V 10% TANT	1000076	46
2	R25,R45	RES 2K ¼W 5%	1302388	47
1	C60	CAP 1000PF 100V 5% MICA	1000042	48
3	C22,C32,C62	CAP.68DPF 100V 5% DW	1000026	49
2	C63,C64	CAP 33DPF 100V 5% DW	1000023	50
3		SPACER (CABLE CLAMP)	1202704	51
6		EYELET GS4-11 STIMPSON	9006750	52
3		HANDLE FLIP CHIP-MAGENTA	9008337-06	53
1		ETCHED CIRCUIT BOARD	5008848	54
REF		MODULE HISTORY LIST	B-MH-M840-YA-6	55
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M840-YA-5	56
REF		X-Y COORDINATE HOLE LOC	K-CO-M840-YA-4	57

PARTS LIST
ETCH BOARD REV K

IC TYPE	GND	+5V
IC 384	1	8
IC 6314	1	8
IC 8271	8	16
IC 380	1	8

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

ITEM NO.	AWG	FROM PT	TO PT

JUMPER LIST

CHANGE NO.	REV	DEC NO.	EIA NO.
		DEC 6531	MPS 6531
		DEC 6534 D	MPS 6534
		D 664	IN3606
		D 662	IN645

SEMICONDUCTOR CONVERSION CHART

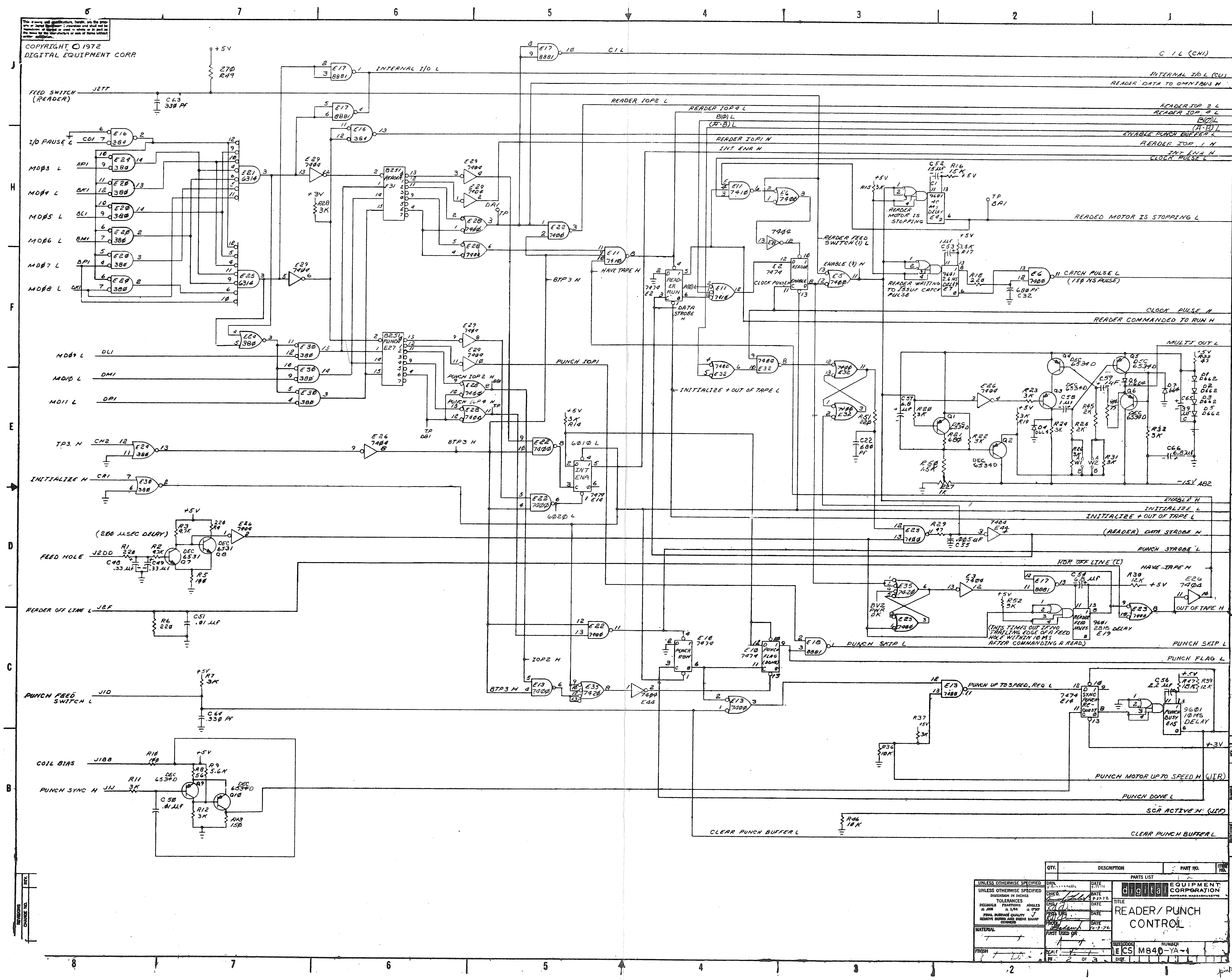
DRN. [illegible] DATE 9/21/72
CHK'D. [illegible] DATE 9/26/72
ENG. [illegible] DATE 10/3/72
PROJ. ENG. [illegible] DATE 10/3/72
PROG. [illegible] DATE 10/3/72
NEXT HIGHER ASSY B-DD-PMK01-T
SCALE 3/1
SHEET 1 OF 3

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE READER/PUNCH CONTROL

SIZE E | CODE CS | NUMBER M840-YA-1 | REV. | DIST.

MATERIAL E CS M840-YA-1 | SIZE | NUMBER | ITEM NO.


COPYRIGHT © 1972
DIGITAL EQUIPMENT CORP.
FEED SWITCH (READER)
I/O PAUSE L
INITIALIZE H
FEED HOLE
READER OFF LINE L
PUNCH FEED SWITCH L
COIL BIAS
PUNCH SYNC H
C I L (CHI)
INTERNAL I/O L (CU)
READER DATA TO OMNIBUS H
READER MOTOR IS STOPPING L
CATCH PULSE L
CLOCK PULSE H
READER COMMANDED TO RUN H
INITIALIZE + OUT OF TAPE L
PUNCH STROBE L
HAVE TAPE H
OUT OF TAPE H
PUNCH SKIP L
PUNCH FLAG L
PUNCH UP TO SPEED, REQ L
PUNCH MOTOR UP TO SPEED H
PUNCH DONE L
CLEAR PUNCH BUFFER L
DIGITAL EQUIPMENT CORPORATION
READER/ PUNCH CONTROL
CS M840-YA-1

C1L (CH1)
INTERNAL I/O L (CL1)
READER DATA TO OMNIBUS H
READER IOP 2 L
READER IOP 4 L
B(2) L
(A-B) L
ENABLE PUNCH BUFFER L
READER IOP 81 H
INT ENA H
BLOCK PULSE L
READER MOTOR IS STOPPING L
CATCH PULSE L
CLOCK PULSE H
READER COMMANDED TO RUN H
MULTI OUT L
CLOCK PULSE H
ENABLE H
INITIALIZE L
INITIALIZE & OUT OF TAPE L
(READER) DATA STROBE H
PUNCH STROBE L
OUT OF TAPE H
PUNCH SKIP L
PUNCH FLAG H
PUNCH DONE L #3
+3V
PUNCH MOTOR UP TO SPEED H (J1R)
SCR ACTIVE H (J1F)
CLEAR PUNCH BUFFER L

+5V R41 3K
A(2) L
B(2) L
B(2-8) L
BB(0)
BB(1)
BA(0)
BA(1)
+5V R42 3K
TP
SHIFT PULSE L
150 NS PULSE
ROTATE PULSE H
(150 NS PULSE)
R39 22Ω
C68 1000 H
R35 330
C61 1500 pF
R38 820
C62 680 H
R43 3K

HOLE 8 J1T
HOLE 7 J1V
HOLE 6 J1X
HOLE 5 J1Z
HOLE 4 J10D
HOLE 3 J1FF
HOLE 2 J1N
HOLE 1 J1LL

(PUNCH BUFFER)
(READER BUFFER)

BR1 DATA 84 L
BS1 DATA 85 L
BU1 DATA 86 L
BV1 DATA 87 L
DA1 DATA 88 L
DS1 DATA 89 L
DU1 DATA 10 L
DV1 DATA 11 L

RD HOLE 8 J2BB
RD HOLE 7 J2Z
RD HOLE 6 J2X
RD HOLE 5 J2V
RD HOLE 4 J2T
RD HOLE 3 J2R
RD HOLE 2 J2N
RD HOLE 1 J2L

(READER + PUNCH SKIP) CS1 SKIP L
(READER + PUNCH INT RQST) CP1 INT RQST L
PUNCH DONE H J1N
PUNCH MOTOR UP TO SPEED H J1R
SCR ACTIVE H J1F

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/16 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND SHARP EDGES
MATERIAL
FINISH

DRW V. DiDonato DATE 4-22-72
CHKD DATE 5-27-72
ENG DATE
PROJ DATE
MFG DATE

QTY. | DESCRIPTION | PART NO. | ITEM NO.
PARTS LIST

digital EQUIPMENT CORPORATION maynard, massachusetts

TITLE READER / PUNCH CONTROL

SIZE CODE E | NUMBER CS-M840-YA-1
SCALE | SHEET 3 OF 3 | DWG. | REV.

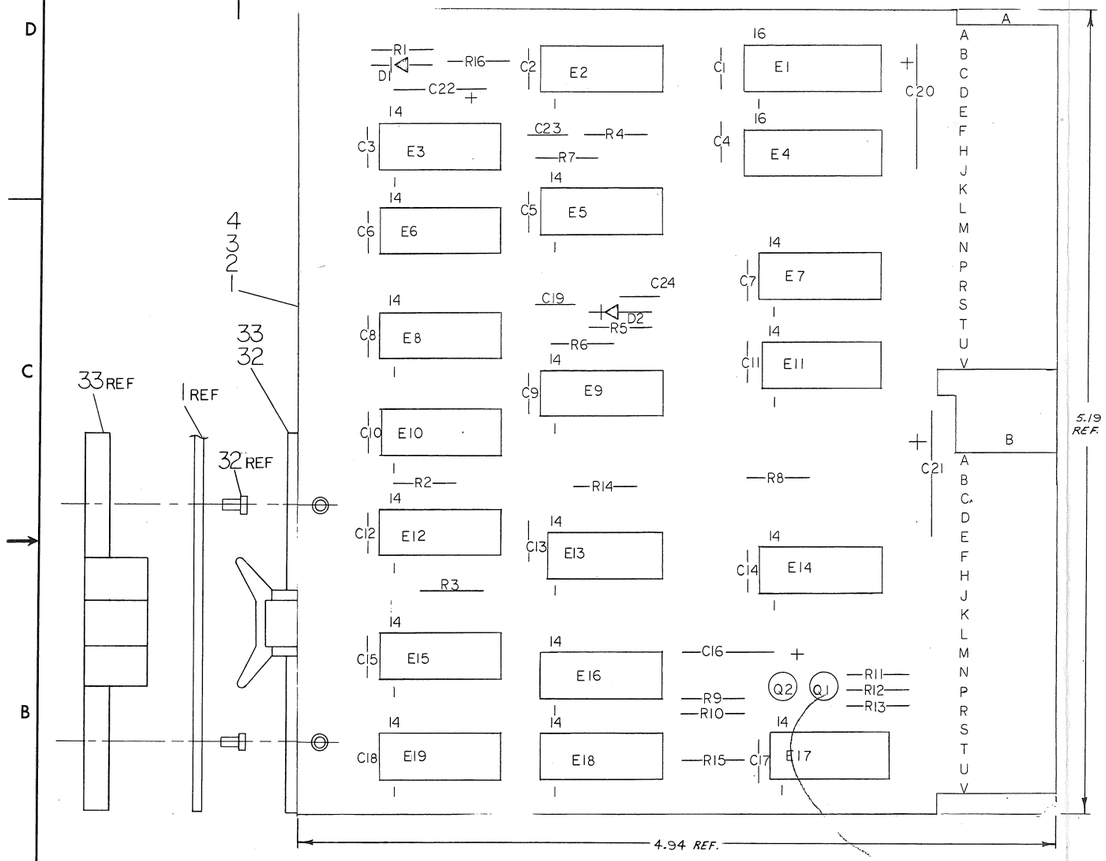
REVISIONS | REV. | CHANGE NO.

SEE FORM NO. BD 309

CS-M840-YA-1

NOTES:

1. UNLESS OTHERWISE NOTED:
   RESISTANCE IS IN OHMS
   CAPACITANCE IS IN PICOFARADS



IC DEC 4015P	8	16
IC TYPE	GND	+ 5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE		
IC PIN LOCATIONS		

BRUNING 40-522 16699
DEC FORM NO. DRD-135A

ITEM NO.	PART NO.	DESCRIPTION	REF DESIGNATION	QTY
33	9008337-06	HANDLE FLIP CHIP - MAGENTA		2
32	9006732	EYELET HGS4-7 STIMPSON		4
31	1910087	IC DEC. 4015P	E1,E4	2
30	1909686	IC DEC. 7404	E8,E13,E17	3
29	1909373	IC DEC. 9601	E3	1
23	1905590	IC DEC. 7401	E6,E7,E11	3
27	1905579	IC DEC. 7440	E12	1
26	1905578	IC DEC. 7430	E14	1
25	1905576	IC DEC. 7410	E10	1
24	1905575	IC DEC. 7400	E2,E9,E16,E19	4
23	1905547	IC DEC. 7474	E5,E15,E18	3
22	1509338	TRANSISTOR DEC 6531	Q1,Q2	2
21	1301972	RES 270 1/4W 5%	R15	1
20	1300488	RES. 12K 1/4W 5%	R1	1
19	1300447	RES. 4.7K 1/4W 5%	R9,R12	2
18	1300365	RES. 1K 1/4W 5%	R7,R14	2
17	1300316	RES. 470 1/4W 5%	R2,R6,R8	3
16	1300295	RES. 330 1/4W 5%	R11	1
15	1300271	RES. 220 1/4W 5%	R5,R13	2
14	1301890	RES. 560 1/4W 5%	R16	1
13	1300229	RES. 100 1/4W 5%	R4,R10	2
12	1300202	RES. 47 1/4W 5%	R3	1
11	1210244-0	GRIPLETS		
10	1100114	DIODE D664	D1,D2	2
9	1005965	CAP. .47UF 35V 10% S. TANT	C23	1
8	1001610	CAP. .01UF 100V 20% DISC.	C1 THRU C18	18
7	1000067	CAP. 6.8UF 35V 20% S. TANT	C20,C21,C22	3
6	1000025	CAP. 560PF 100V 5% D.M.	C19	1
5	1000020	CAP. 180PF 100V 5% D.M.	C24	1
4	B-MH-M7050-YA-6	MODULE ECO HISTORY		REF
3	D-AH-M7050-YA-5	ASSY/DRILLING HOLE LAYOUT		REF
2	K-CO-M7050-YA-4	X-Y COORDINATE HOLE LOCATION		REF
1	5009188	ETCHED CIRCUIT BOARD		1

PARTS LIST

ETCH BOARD REV D

FIRST USED ON OPTION MODEL: PMK01

REV	CHANGE NO.	DEC NO.	EIA NO.
		DEC D664	IN3606
		DEC 6531	MPS 6531

REVISIONS

SEMICONDUCTOR CONVERSION CHART

DRN.	DATE 9-14-72
CHK'D.	DATE 9-14-72
ENG.	DATE 10-9-72
PROJ. ENG.	DATE 10-9-72
PROD.	DATE 10-9-72

NEXT HIGHER ASSY: D-MU-PMK01-0-0

SCALE

SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: READER CONTROL

SIZE	CODE	NUMBER	REV.
D	CS	M7050-YA-1	

DIST.

REV. B
NUMBER M7050-YA-1
SIZE D CODE CS

C-26

SIZE D | CODE CS | NUMBER M7050-YA-1 | REV

UNLESS OTHERWISE INDICATED:
RESISTORS = 1/4W 5%
CAPACITORS = .01UF, 100V, 20%
DEC7401 = E6, E7, E11
DEC9601 = E3
DEC7404 = E8, E13, E17
DEC7475 = E1, E4
DEC7474 = E5, E15, E18
DEC7400 = E2, E9, E16, E19
DEC7410 = E10
DEC7430 = E14
DEC7440 = E12
PIN 12 = GND ON E1, E4
PIN 5 = +5V
PIN 7 = GND ON ALL OTHER IC'S
PIN 14 = +5V

SHEET 2 OF 2

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MPS6531	MPS6531	D664	IN3606

REVISIONS			
CHR	CHG NO	REV	
1	10001	C	

DRN Nancy Keefe DATE 2/2/71
CHKD DATE 4-29-71
ENGR DATE 4-29-71
PROJ Wadsworth DATE 6-7-72

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: READER CONTROL

SIZE D | CODE CS | NUMBER M7050-YA-1 | REV. D | PRINTED CIRCUIT REV.

DEC FORM 140 1188 115

M-1195

SIZE B
CODE CS
NUMBER W023-0-1
REV.
RIBBON CABLE
BLK
BRN
RED
ORN
YEL
GRN
BLU
VIO
GRY
WHT
BLK
BRN
RED
ORN
YEL
GRN
BLU
VIO
A
B
C
D
E
F
H
J
K
L
M
N
P
R
S
T
U
V
NOTE:
Ø ARE SPLIT LUGS
PARTS LIST IS A-PL-W023-0-0
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.
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REVISIONS
REV.
CHG NO.
CHK
DRN.
ENGR.
ENG.
PROD.
DATE 9-16-68
DATE 10-7-68
DATE 11-12-68
DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC
EIA
DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
CONNECTOR W023
SIZE B
CODE CS
NUMBER W023-0-1
REV.
PRINTED CIRCUIT REV.
A
PINK DIST. 434 435 359

READER'S COMMENTS

DEC-FS-HPMKA-A-D
PMK01 PROCESSOR
MAINTENANCE MANUAL

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Is there sufficient documentation on associated system programs required for use of the software described in this manual? If not, what material is missing and where should it be placed?

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Organization _____

Please describe your position _____

Street _____

City _____ State _____ Zip Code _____

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