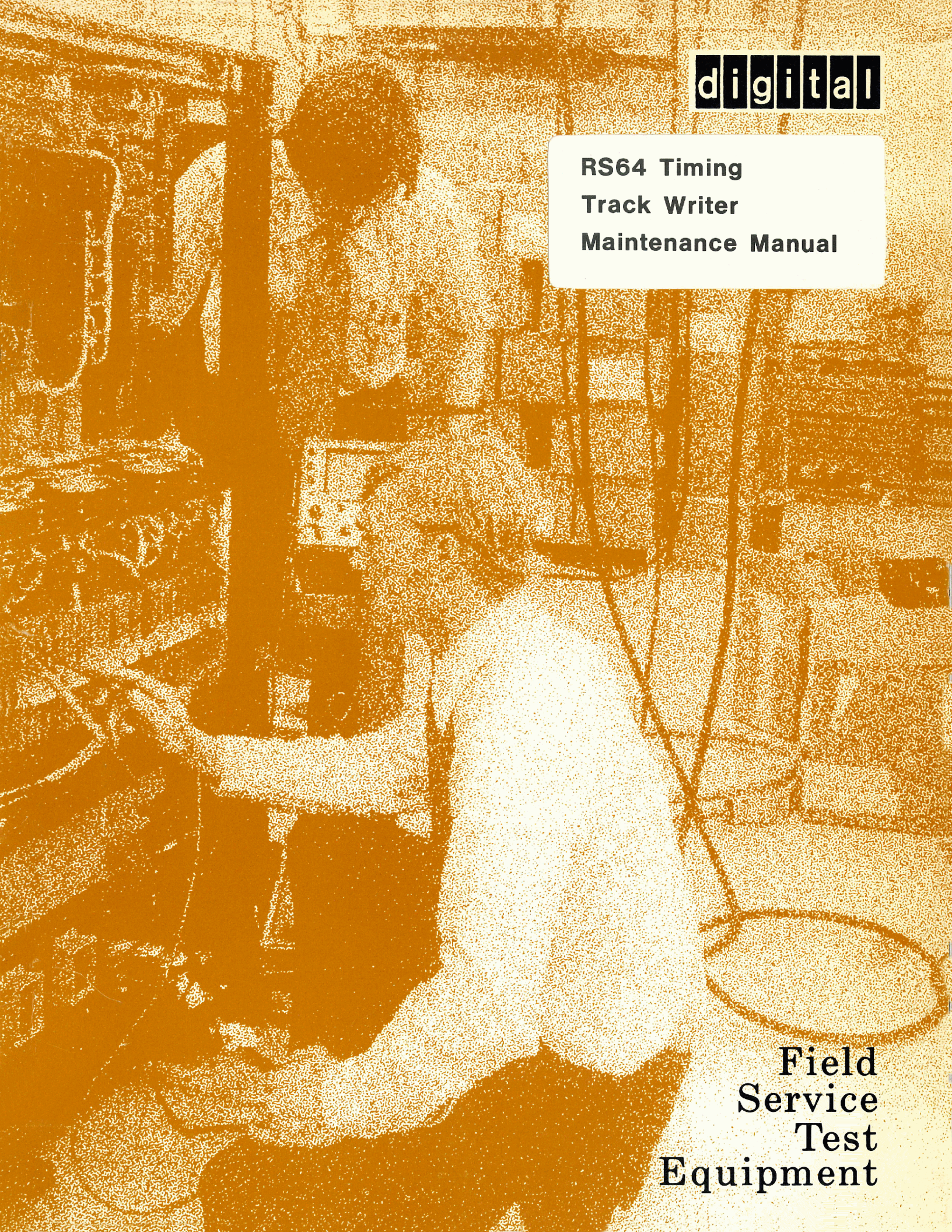


digital

RS64 Timing Track Writer Maintenance Manual

Field Service Test Equipment

DEC-FS-HRSMM-A-D

RS64 Timing Track Writer Maintenance Manual

digital equipment corporation · maynard, massachusetts

1st Edition, December 1974

Printed in U.S.A.

CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

TABLES

RS64 TIMING TRACK WRITER

RS64 Timing Track Writer (RS64-TA)

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides a complete description of the RS64 Timing Track Writer, including physical, functional, logic and flow diagram descriptions, specifications, and utilization and maintenance procedures.

1.2 GENERAL DESCRIPTION

The RS64 Timing Track Writer (RS64-TA) is a portable unit used to write timing tracks on disks in the RS64 Disk Drive. The timing tracks must be rewritten after installing new timing track heads or a new disk surface.

NOTE

If data errors occur immediately after the disk surface is cleaned, the first corrective action should be to rewrite the timing tracks. However, rewriting the timing tracks destroys all the data stored on the disk. This is because the data stored using the old timing tracks will be out of sync with the new timing tracks and therefore cannot be retrieved accurately.

The RS64-TA is completely contained in a carrying case and connects directly to the disk drive's timing track heads.

Operating power for the RS64-TA is provided by the disk drive via a power cable/tester cable combination which routes dc power from the disk drive's power supply directly to the writer.

1.3 PHYSICAL DESCRIPTION

The RS64-TA (Figure 1-1) consists of the following:

Carrying Case

Control Panel Assembly

Disk Plug Cable

Control Panel Cable

RS64 PS/Test Cable

Power Cable

Wired Assembly

Disk Preamplifier and Peak Detection Module (G088) (three)

Disk Writer with Power Fail Module (G291) (six)

50 mA Indicator Driver Module (M050)

Inverter Module (M111)

NOR Gate 2 Input Module (M112) (two)

NAND Gate 2 Input Module (M113) (two)

NAND Gate 3 Input Module (M115)

NAND Gate 4 Input Module (M117)

NAND Gate 8 Input Module (M119)

R/S Flip-Flop Module (M203)

D-Type Flip-Flop Module (M205) (two)

8-Bit Buffer Shift Register (M208)

Binary Up/Down Counter Module (M211) (two)

Dual Delay Multivibrator (M302)

Variable Clock Module (M401)

Pulse Amplifier Module (M602)

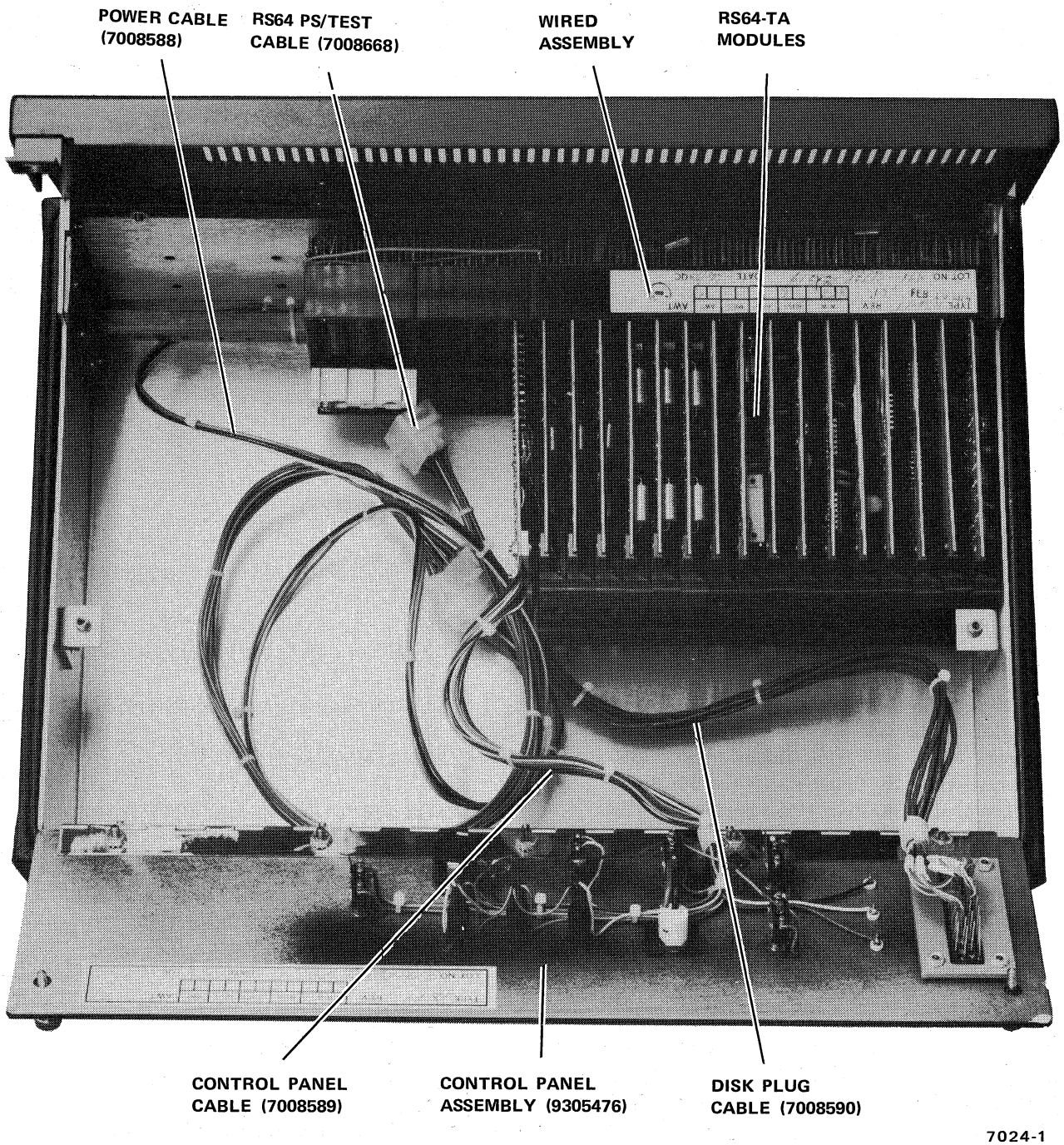


Figure 1-1 RS64-TA Components

1.3.1 Control Panel Assembly

The 9305476 control panel (Figure 1-1) contains a signal input connector slot and controls and indicators necessary to write timing on the surfaces of RS64 disks. Refer to engineering drawing D-AD-9305476-0-0 for wiring data, parts identification, and complete physical layout.

1.3.2 Disk Plug Cable

The 7008590 disk plug cable (Figure 1-1) consists of a module connector which mounts to the control panel assembly, a connector module (M908) which mounts in slot B17 of the wired assembly, and cabling which routes the timing track signals from the wired assembly to the control panel. Refer to engineering drawing D-IA-7008590-0-0 for wiring data, parts identification, and physical specifications.

1.3.3 Control Panel Cable

The 7008589 control panel cable (Figure 1-1) consists of a connector module (M908), which mounts in slot A17 of the wired assembly, and cabling. This cable assembly connects the control panel switches and indicators to the wired assembly. Refer to engineering drawing D-IA-7008589-0-0 for wiring data, parts identification, and physical specifications.

1.3.4 RS64 PS/Test Cable

The 7008668 test cable (Figure 1-1) consists of a 12-pin, male Mate-N-Lok connector, a 12-pin, female Mate-N-Lok connector, and a 12-wire cable harness. The cable routes dc power from the RS64 Disk Drive's power supply to the RS64-TA power cable. Refer to engineering drawing C-IA-7008668-0-0 for wiring data, parts identification, and physical specifications.

1.3.5 Power Cable

The 7008588 power cable (Figure 1-1) consists of a 4-wire cable harness with a male, 12-pin Mate-N-Lok connector attached to one end. The cable routes dc power from the RS64 PS/test cable to the wired assembly backpanel. Refer to engineering drawing D-IA-7008588-0-0 for wiring data, parts identification, and physical specifications.

1.3.6 RS64-TA Modules

For detailed information on the modules used in the RS64-TA, see Appendix A.

1.4 SPECIFICATIONS

1.4.1 Environmental

Ambient Temperature, ° C

0 to 50 operating

-10 to 65 storage

Relative Humidity, %

10 to 90 (without condensation, operating)

5 to 95 (storage)

1.4.2 Power Requirements

+20 V
+5 V
-15 V
} Power taken from disk drive's power supply

1.4.3 Packaging

Carrying Case Dimensions

12 in. H X 18 in. W X 6-1/2 in. D

Weight

27 lb

CHAPTER 2
UNPACKING, ACCEPTANCE TESTING, AND SETUP

2.1 UNPACKING PROCEDURE

To unpack the RS64-TA, proceed as follows:

1. Remove the carrying case from the shipping carton and inspect for exterior damage. Damage claims should be directed to the responsible shippers.

2. Open the carrying case and inspect the RS64-TA components for damage.

3. Verify that all components are present per Paragraph 1.3.

2.2 ACCEPTANCE TEST PROCEDURE

The RS64-TA is shipped ready to use. If the unit is not operating properly, refer to Chapter 5 (Maintenance) and diagnose and correct the problem. Service should be performed by qualified service personnel only.

NOTE

If faulty operation is detected at any point in the following procedure, refer to Chapter 5 and correct the fault before proceeding to the next step in the procedure.

NOTE

To make the RS64-TA wired assembly accessible, remove the RS64-TA chassis from the carrying case and unscrew and remove the rear portion of the chassis cover and the chassis backplate.

1. Check the wired assembly backpanel for bent pins.

2. Using the external components list (Table 2-1), check that all resistors and capacitors are properly connected to the wired assembly backpanel pins.

Table 2-1
External Components

	Parameters	Location	
		From	To
Resistors	1/4 W, 1K	A24E1	A24K1
		A24E2	A24K2
		A24L1	A24R1
	1 W, 300Ω	A14A2	A17S2
Capacitors	6.8 μF, +35 Vdc	A11B2(-)	A10C2(+)
		B1F1(-)	B1L2(+)
		B1R1(-)	B1S2(+)
		A12C2(-)	A14A2(+)
		A5C2(-)	A3A2(+)

3. Perform steps 1, 2, 4, and 5 of the setup procedure (Paragraph 2.3).

4. Check for proper dc voltages at the RS64-TA wired assembly pins listed below.

A16C2	GND
A1A2	+5 V
A14A2	+20 V
A16B2	-15 V

5. Set the RS64-TA MAINT toggle switch to MAINT.

6. Set the RS64-TA 50HZ/60HZ toggle switch to 60HZ.

7. Turn the RS64-TA GAP ADJUST knob fully counterclockwise and then turn it clockwise five complete turns.

NOTE

An oscilloscope (Tektronix 453 or equivalent) is required to perform the following steps.

8. Connect the channel 1 probe to pin A1D2 on the RS64-TA wired assembly.

9. The clock repetition rate should be 210 ns (positive pulse).

10. Rotate the GAP ADJUST knob clockwise and counterclockwise; observe that the clock repetition rate varies.

11. Connect the channel 1 probe to pin B1F2 (CLK RUN L) on the RS64-TA wired assembly; observe a 55 ± 5 ms positive-going pulse (adjustable).

12. Connect the channel 1 probe to pin B9F2 (DLY A H) on the RS64-TA wired assembly; observe a positive-going pulse of approximately 275 ± 25 μs in duration (fixed setting).

13. Connect the channel 2 probe to pin B9T2 (DLY B H) on the RS64-TA wired assembly; observe a positive-going pulse 100 μs longer than DLY A H (pin B9F2).

14. Set the scope controls as follows:

    - Vertical

      Mode = ALT
      Sensitivity = 0.2 V/div
      Coupling = dc

    - Horizontal

      A sweep time = 100 ns/div
      Trigger = Normal/internal
      Slope = Positive

15. Connect the channel 1 probe to pin A2J2 (CLK H) and the channel 2 probe to pin A2E1 (CLK A H) on the wired assembly; observe that A2E1 is 90 degrees out of phase with A2J2 and that the pulse width of both signals is 440 ns.

16. Change scope sweep time to 5 ms/div; observe a pulse train length of 33 ms.

17. Set the scope controls as follows:

    - Vertical

      Mode = Channel 1
      Sensitivity = 0.2 V/div
      Coupling = dc

    - Horizontal

      A sweep time = 10 ms
      Trigger = Normal

18. Connect the channel 1 probe to pin A4J2 (WREN H) on the wired assembly; observe a positive-going pulse of 90 ± 10 ms.

19. Set scope sweep time to 100 ns and connect the channel 1 probe to wired assembly pin A10U2 (WFA H); observe positive-going pulse of 840 ns.

20. Set scope sweep time to 5 ms; observe a pulse train length of approximately 33 ms.

21. Set scope sweep time to 2 μs and connect the channel 1 probe to wired assembly pin A10J2 (WFB H); observe positive-going pulses of 17 ± 0.5 μs.

22. Set scope sweep time to 0.5 ms; observe a pulse repetition rate of approximately 0.5 ms.

23. Set scope sweep time to 5 ms; observe a pulse train length of approximately 33 ms.

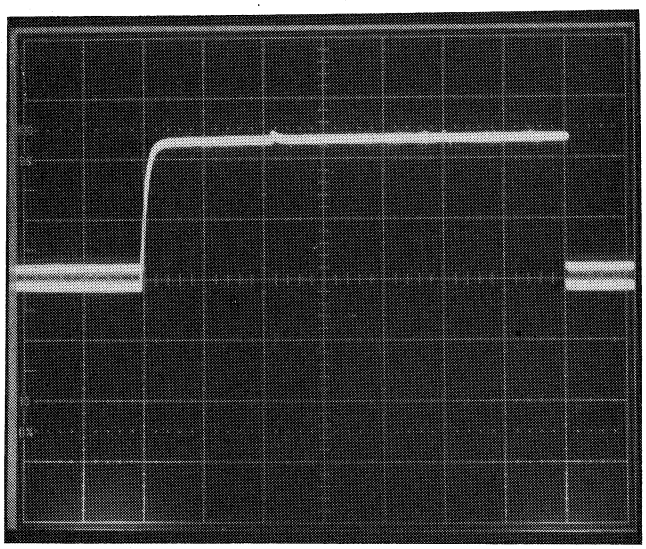
24. Connect the scope probe to wired assembly pin A10E1 (WFC H); observe a pulse train length of approximately 33 ms.

25. Set the scope to 5 V/div sensitivity and 10 ms sweep time and scope wired assembly pins E2 and F2 at locations A11, A12, A13, B12, B13, and B14; observe that write amplifier outputs are present at each pin (Figure 2-1).

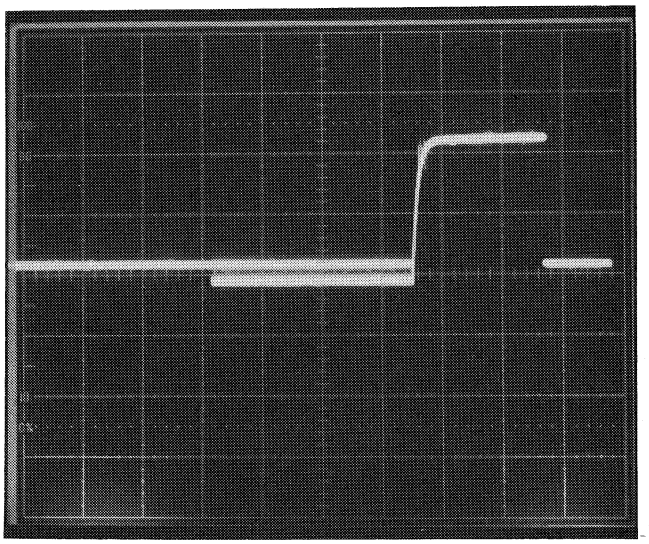
26. Check the slice voltage on the G088 modules, pin BU2 at slot positions 14, 15, and 16. Slice voltage should be -1.4 V.

27. Remove dc power from the RS64 Disk Drive by turning power off at the main computer console.

28. Set the RS64-TA MAINT toggle switch down.



a. Pin E2



b. Pin F2

Figure 2-1 Write Amplifier Output Waveforms

2.3 SETUP PROCEDURE

To connect the RS64-TA to the RS64 Disk Drive, proceed as follows:

1. Remove dc power from the RS64 Disk Drive by turning off the power at the main computer console.

   NOTE
   The ac power to the RS64 Disk Drive must remain on.

2. Disconnect the dc power connector on the top of the RS64's power supply and connect the RS64 PS/test cable (which connects to the RS64-TA power cable) to the power supply.

3. Disconnect the disk drive's timing cable assembly from module slot F09 and insert it into the module connector on the RS64-TA control panel (Figure 3-1).

4. At the RS64-TA, set the 50HZ/60HZ toggle switch to the ac input line frequency of the disk drive.

5. Turn power on at the main computer console to apply dc power to the RS64-TA.

CHAPTER 3
OPERATION AND UTILIZATION

3.1 SCOPE

This chapter covers complete operation of the RS64 Timing Track Writer, including a description of front panel controls and indicators and a utilization procedure.

3.2 CONTROLS AND INDICATORS

The RS64-TA control panel (Figure 3-1) is equipped with the controls and indicators necessary to:

- Adjust the gap (the elapsed time between the end and the beginning of the timing tracks).
- Initiate a timing track write operation.
- Select different clock repetition rates in accordance with the disk drive's ac input line frequency.

Table 3-1 identifies each control and indicator by name and function.

3.3 UTILIZATION PROCEDURE

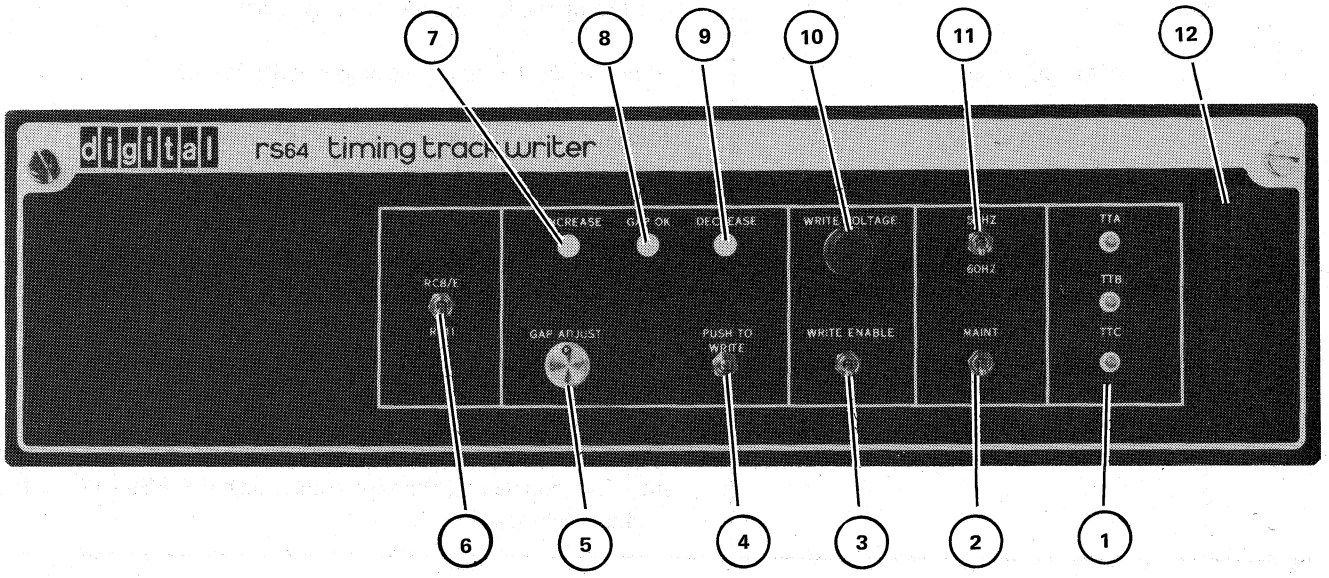
Timing tracks must be rewritten after installing new timing track heads or a new disk surface.

3.3.1 Procedure for Writing Timing Tracks

To write timing tracks, proceed as follows:

NOTE

If faulty operation is detected at any point in the following procedure, refer to Chapter 5 and correct the fault before proceeding to the next step in the procedure.



7024-4

Figure 3-1 RS64-TA Control Panel Controls and Indicators

Table 3-1
RS64-TA Control Panel Controls and Indicators

Item (Figure 3-1)	Name	Function
1	TTA/TTB/TTC test pins	These test pins enable the timing information written on the disk surface to be monitored at the control panel using an oscilloscope.
2	MAINT toggle switch	Selects maintenance mode for checkout and troubleshooting. Selecting MAINT causes the RS64-TA to perform write operations continuously.
3	WRITE ENABLE toggle switch	Setting this toggle switch to WRITE ENABLE enables the RS64-TA to write timing tracks and lights the WRITE VOLTAGE indicator.
4	PUSH TO WRITE pushbutton	If the WRITE ENABLE toggle switch is on, depressing this pushbutton causes the RS64-TA to perform one timing track write operation.
5	GAP ADJUST knob	Controls the width of the gap (a blank area on the disk surface which allows time for the disk drive to switch heads) by varying the clock repetition rate. Turning the knob clockwise increases the gap width.
6	RS8/E–RC11 toggle switch	This switch is not operational.
7	INCREASE neon	Blinks when the gap width is too narrow. The clock repetition rate must be increased using the GAP ADJUST knob before the timing tracks can be written properly.
8	GAP OK neon	Blinks when the timing track gap width is correct.
9	DECREASE neon	Blinks when the timing track gap width is too wide. The clock repetition rate must be reduced using the GAP ADJUST knob before the timing tracks can be written properly.
10	WRITE VOLTAGE indicator	Illuminates when power is applied to the timing track writer and the WRITE ENABLE toggle switch is on.
11	50HZ/60HZ toggle switch	Selects one of two clock repetition rates based on the disk drive's ac input line frequency.
12	Module Connector	The RS64 Disk Drive's timing track cable connector inserts into this connector, thereby connecting the RS64-TA to the timing track heads.

CAUTION

Timing tracks should be rewritten only when necessary. Continuous writing of the timing tracks may damage the disk drive's timing track heads.

1. Perform the RS64-TA setup procedure per Paragraph 2.3.

2. At the RS64-TA:

CAUTION

Ensure that the MAINT toggle switch (Figure 3-1) is down prior to setting the WRITE ENABLE toggle switch on. Otherwise, the disk drive's timing track heads may be damaged.

   a. Set the WRITE ENABLE toggle switch on; observe that the WRITE VOLTAGE indicator illuminates.

   b. Depress the PUSH TO WRITE pushbutton; observe the INCREASE, GAP OK, and DECREASE neons.

NOTE

The RS64-TA writes the timing tracks only once each time the PUSH TO WRITE pushbutton is depressed.

   c. If the GAP OK neon illuminates, the timing tracks have been written correctly; proceed to step 3.

   d. If the INCREASE neon illuminates, turn the GAP ADJUST knob clockwise and repeat steps b. and c.

   e. If the DECREASE neon illuminates, turn the GAP ADJUST knob counterclockwise and repeat steps b. and c.

NOTE

An oscilloscope (Tektronix 453 or equivalent) is required to perform the following steps.

3. Set the scope controls as follows:

   Vertical = 0.2 V/div (X10 probe)
   Mode = Channel 1
   Coupling = dc
   A sweep time = 5 ms/div
   Trigger = Line

4. Connect the channel 1 scope probe to test pin TTA on the RS64-TA control panel.

5. Depress the control panel PUSH TO WRITE pushbutton; observe timing track A on the oscilloscope display as shown in Figure 3-2.

6. Depress the RS64-TA PUSH TO WRITE pushbutton; observe that timing track A momentarily disappears and reappears each time the PUSH TO WRITE pushbutton is depressed. This is due to the erase operation performed by the RS64-TA just prior to rewriting timing tracks.

7. Connect the channel 1 probe to test pin TTB on the RS64-TA control panel and observe timing track B.

8. Connect the channel 1 scope probe to test pin TTC on the RS64-TA control panel and observe timing track C.

9. Set the RS64-TA WRITE ENABLE toggle switch off and observe that the WRITE VOLTAGE indicator extinguishes.

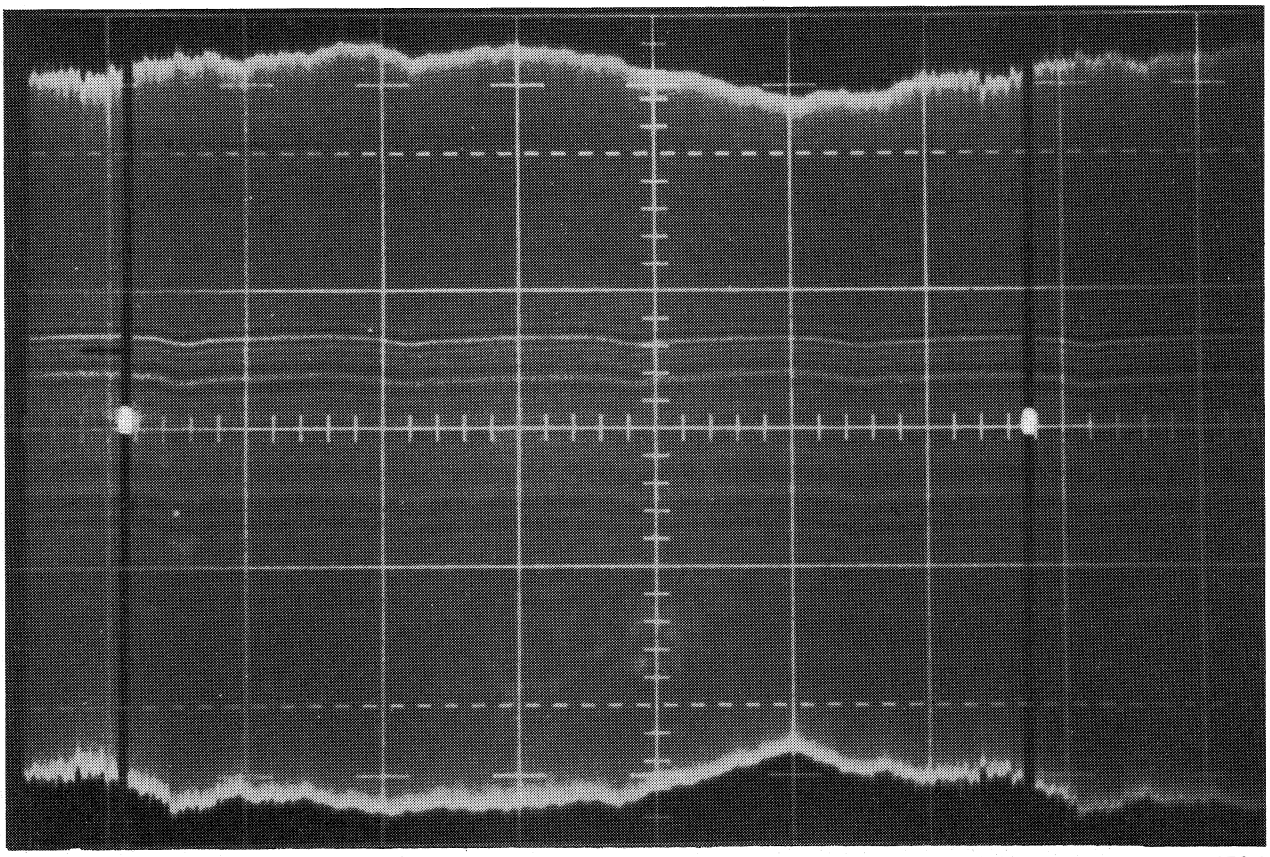
10. Remove dc power from the RS64 Disk Drive by turning off the power at the main computer console.

11. Disconnect the RS64-TA dc power cable from the disk drive's power supply.

12. Remove the timing track cable from the RS64-TA control panel connector and insert it into slot E09 of the RS64 Drive electronics.

13. Reconnect the dc power connector on top of the RS64's power supply.

14. Apply dc power to the disk drive.



5056-1

Figure 3-2 Timing Track A Waveform

3.3.2 Verification of Timing Track Writer Performance After writing new timing tracks, the RS64 Disk Drive's read amplifier-peak detectors must be readjusted and diagnostics must be run to verify that the timing tracks were correctly written.

3.3.2.1 Read Amplifier-Peak Detector Adjustments – Initially, the read amplifier-peak detectors are statically adjusted for a nominal operating point. Next, each is dynamically adjusted using a controller for bit patterns and for error detection. The dynamic adjustment entails locating a mean point between data peaks and noise peaks. To perform these adjustments:

1. Using an oscilloscope or VOM, adjust all four read amplifier-peak detectors for static threshold operating value of −1.2 V. Access points for the read amplifier-peak detectors are as follows:

Read Amplifier-Peak Detector	Access Point
Clock	F08-U2
Sector Mark	F07-U2
Address	F06-U2
Data	D07-U2

2. Write a pattern (all 1s, for example) on one complete data track, then begin a repetitive read and comparison operation for that track.

3. Connect an oscilloscope or VOM at the clock read amplifier-peak detector test point (F08-U2).

4. While monitoring for errors, slowly adjust the clock threshold potentiometer for a more positive indication. When an error occurs, record the threshold indication as V_{High}.

5. Adjust the potentiometer for a more negative threshold value and observe where the error occurs. Record this value as V_{Low}.

6. Calculate the mean threshold as follows and set the potentiometer for that value.

$$V_{mpt} = (V_{High} + V_{Low})/2$$

7. Using steps 2 through 6, set up the threshold for the sector mark and address read amplifier-peak detectors. Test points are as follows:

Sector Mark	F07-U2
Address	F06-U2

8. For the data read amplifier-peak detector adjustment, write an all-zero pattern in every track. Next, initiate a repetitive read and comparison for track 17_8. (The outermost data track normally has the greatest amount of noise and wobble.)

9. Connect the oscilloscope to the data read amplifier-peak detector test point (D07-U2). While observing the data comparison result, adjust the data threshold potentiometer (for a more positive scope indication) until an error occurs. Decrease the threshold setting slightly until no errors occur.

10. Read and compare data for all other tracks. If no errors are detected for the other tracks, proceed to step 11. If errors are detected (signifying tracks with greater amounts of noise than track 17_8), record the track numbers containing errors. Readjust the data threshold while reading and comparing data from these tracks and locate the noisiest track on the disk.

11. Record the threshold voltage (V_{High}) for track 17_8 or the noisiest track on the disk.

12. To define the lowest threshold (V_{Low}), write all ones for every track. Initiate a repetitive read and comparison operation for track 30_8. (The innermost track will normally have the lowest amplitude data peaks.) Adjust the data threshold potentiometer (for a more negative threshold) until an error occurs. Decrease the threshold setting slightly until no errors occur.

13. Read and compare data from all tracks. If no errors are detected for the other tracks, proceed to step 14. If errors are detected (signifying tracks having data peaks less than the threshold) record the track numbers. Readjust the data threshold while reading and comparing data from these tracks. Locate the lowest data peak track and set up the threshold for this track.

14. Record the threshold voltage (V_{Low}) for track 30_8 or the track having the lowest data peaks.

15. Calculate the mean threshold as shown in step 6 and set the potentiometer for that value.

3.3.2.2 Verification of Timing Tracks – To verify that the timing tracks were written properly, proceed as follows:

1. Load the disk data diagnostic (MAINDEC-11-DZRCB).

2. Set the switch register to 200_8 and depress LOAD ADRS.

3. Set the switch register to 000000_8 and depress START; observe diagnostic printout.

4. To check that the spare set of timing tracks was written correctly, reverse the timing track cable connector at RS64 electronics slot E09; recalibrate the gain settings for timing tracks A, B, and C read amplifier-peak detectors per Paragraph 3.3.2.1; and repeat steps 3 and 4.

5. Restore the timing track cable connector to its normal configuration; recalibrate the gain settings for timing track read amplifier-peak detectors per Paragraph 3.3.2.1; and run one additional pass of the disk data diagnostic (random mode).

CHAPTER 4
THEORY OF OPERATION

4.1 SCOPE

This chapter provides a detailed description of the RS64 Timing Track Writer. The description is provided in three parts: a functional description, a detailed logic description, and a flow diagram description.

4.2 FUNCTIONAL DESCRIPTION

4.2.1 Introduction

The RS64-TA is used to write timing tracks on the surfaces of disks used in RS64 Disk Drives. These tracks preformat the disk to satisfy synchronization, clocking, and data location requirements of the RC11/RS64 DECdisk system, and must be recorded before data can be stored on the disk.

As illustrated in Figure 4-1, the timing tracks are recorded so that the disk surface is divided into three distinct areas: a sync sector, 77_8 data sectors, and a gap.

- The *sync sector* (the first sector to be recorded) contains a clock signal which enables the DECdisk system to synchronize with the disk surface prior to storing or retrieving data.

- The 77_8 *data sectors* (which follow the sync sector) contain clocking, data location, and addressing information, which serve to locate the data sectors on the disk surface; the data sectors also provide a clock signal to be used by the DECdisk system to actually gate the data to and from the disk surface.

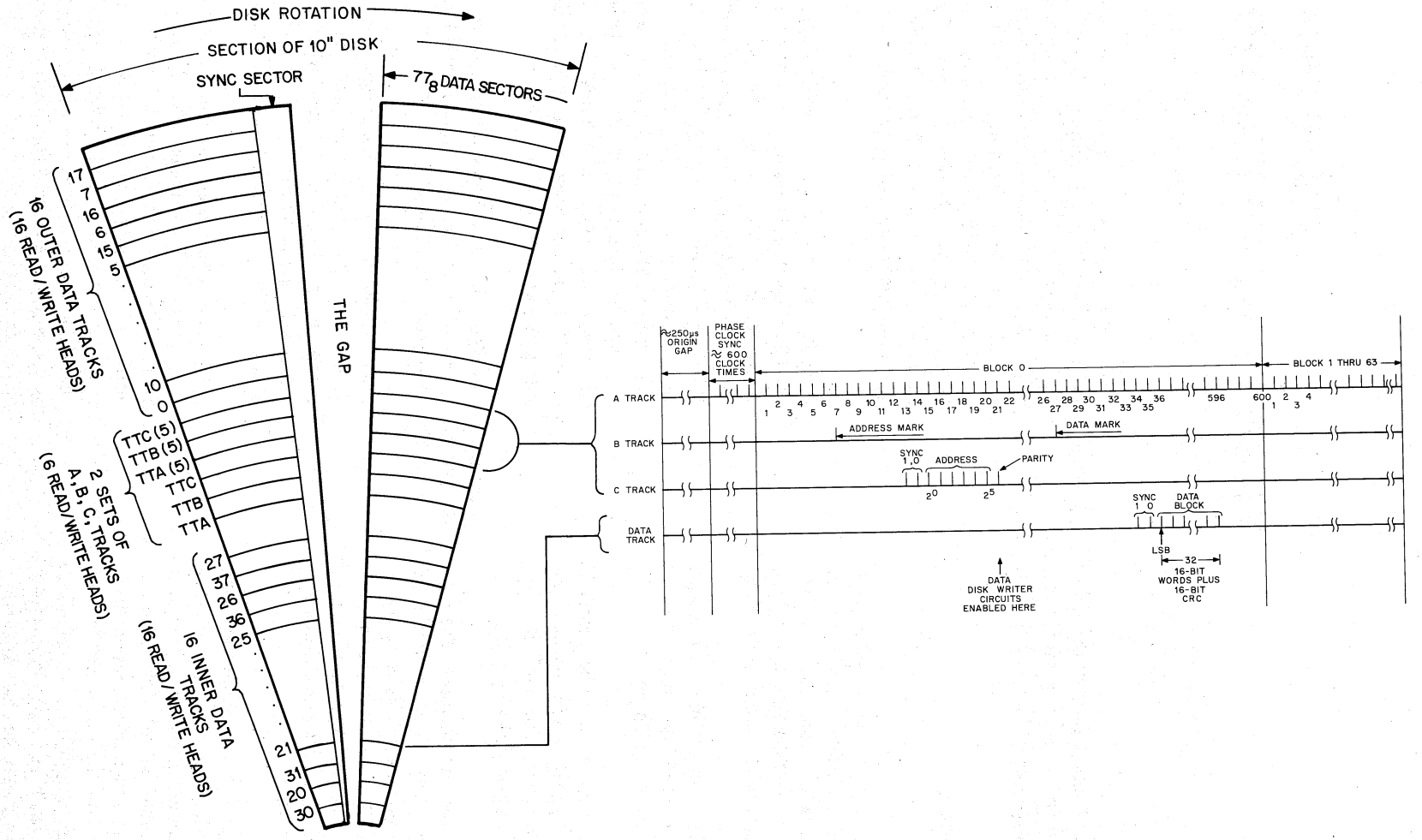
- The *gap* is nothing more than a uniform, blank area on the disk surface; i.e., no timing information or data is recorded in that area. The gap is not visibly discernible on the disk surface as there are no markings such as notches or slits in the disk surface or on the disk edge. The gap allows time for the DECdisk system to switch from one read/write head to another. If this time were not provided, the disk drive logic would have to wait one complete revolution of the disk to resynchronize whenever a different head was selected. The width of the gap area is critical to accurate data storage and retrieval. If the repetition rate of the clock internal to the RS64-TA is adjusted properly when the timing tracks are written, the gap is from 250 to 350 μs wide, i.e., it takes 250 to 350 μs for the gap to pass under the read/write heads.

  To verify that the gap meets specifications, the RS64-TA logic measures the gap after each timing track write operation. The logic measures the elapsed time between the end of track A and the beginning of track A, and illuminates the control panel INCREASE/GAP OK/DECREASE indicators accordingly. If the GAP OK indicator fails to illuminate, the operator must vary the clock rate using the GAP ADJUST knob and rewrite the timing tracks until a proper indication is obtained.

As illustrated in Figure 4-1, three types of timing tracks (A, B, and C) are recorded on the disk surface. Each timing track performs a specific function:

- Track A provides a clocking signal and is recorded in the sync sector and the data sectors. In the sync sector, it synchronizes the DECdisk system to the disk. In the data sectors, it gates the data to and from the disk surface.

- Track B provides address and data markers and is recorded only in the data sectors. The address marker is recorded once per data sector and marks the beginning of the block or sector address which is recorded on track C. The data marker is recorded once per data sector and marks the beginning of data which is recorded on the data tracks.



NOTE:

A = Timing track
B = Address and data marker track
C = Sector address track
AM = Address marker
DM = Data marker

CP-1005

Figure 4-1 RS64 Disk Surface Recording Format

- Track C provides block addresses and is recorded only in the data sectors. The block address is recorded once per data sector and identifies the data sector in which it is recorded. The block address is recorded at the beginning of the data sector so that the RS64 Disk Drive reads the address just before the data portion of the identified sector passes under the read/write heads.

  A synchronizing preamble and a parity bit are included with each block address. The synchronizing preamble (two bits) permits the DECdisk system to synchronize with block address information without having to compensate for skew between track A and track C. The parity bit maintains odd parity.

The RS64-TA writes two identical sets (total of six) of the timing tracks described above: primary timing tracks and spare timing tracks. The spare tracks are used only if the primary tracks are erased or damaged.

NOTE

To change over from the RS64 Disk Drive's primary timing tracks to the spares if the primary tracks are damaged, turn off dc power at the main computer console, disconnect the timing track cable connector from slot E09 of the disk drive electronics, rotate the connector 180 degrees, reconnect the connector, and recalibrate the disk drive's timing track read amplifiers per Paragraph 3.3.2.1.

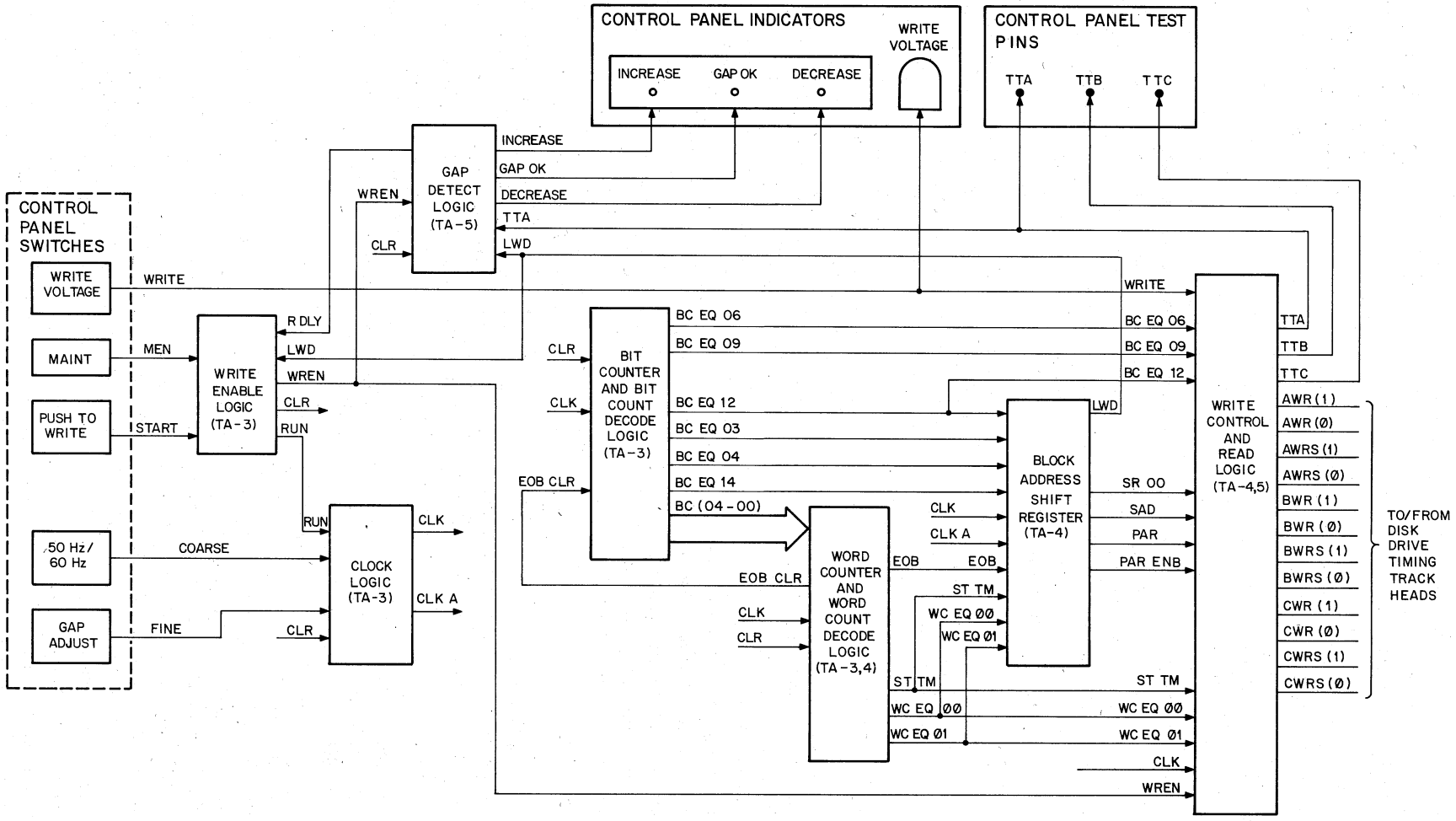
4.2.2 Functional Block Description

The functional block diagram (Figure 4-2) illustrates the major logic sections and the control panel switches, indicators, and test pins.

Assuming that the control panel WRITE ENABLE toggle switch is up, the RS64-TA begins to write timing tracks when the control panel PUSH TO WRITE pushbutton is depressed. This action asserts the START line, which triggers the write enable logic and causes CLR (clear) to assert. CLR initializes the RS64-TA logic, i.e., clears all counters, registers, and flip-flops with the exception of the WREN (write enable) flip-flop, which is set. Setting the WREN flip-flop asserts WREN, which turns on the timing track write amplifiers in the write control and read logic. The write amplifiers write all zeros on the timing tracks for 50 ms, thus erasing all timing information from the disk surface. After 50 ms, RUN asserts and enables the clock logic. The clock then activates CLK and CLK A. CLK is input to the write control and read logic and is used to write track A on the disk surface. CLK is also input to the bit counter, the word counter, and the block address shift register. CLK A is used by the block address shift register. Although the bit counter and word counter are active during the writing of the first sector (the sync sector), the bit count decoder outputs (BC EQ 03, BC EQ 04, etc.) and the word count decoder outputs (WC EQ 00 and WC EQ 01) are not used because the word counter ST TM output is cleared, thereby inhibiting the writing of tracks B and C. Therefore, during the sync sector, the bit counter and word counter complete a normal 600-bit count cycle (thirty-five 17-bit words, plus one 5-bit word); at the end of that count cycle, ST TM is asserted. The assertion of ST TM enables the block address shift register and the B and C portions of the write control and read logic.

After the first sector (the sync sector) count cycle is completed, the count cycle for the next sector (the first data sector) begins immediately. The CLK signal continues to write track A and increment the bit counter. When the bit counter reaches a count of 06, the bit count decode logic asserts BC EQ 06 (bit count equals 06), which is ANDed with WC EQ 00 (word count equals 00) at the write control and read logic, causing the address marker bit to be recorded on track B. The bit counter then continues to count and BC EQ 12 asserts and conditions the block address shift register incrementation logic. BC EQ 12 is also ANDed with WC EQ 00, causing a 1 to be written on track C as the first of two sync bits. (The sync bits make up the sync preamble of the block address.) On the next count, BC EQ 12 clears and a 0 is written on track C as the second sync bit. On the next count, BC EQ 14 asserts and is ANDed with WC EQ 00 at the block address shift register, causing the assertion of SAD (shift address) and activating the SR 00 (shift register 00) output. The assertion of SAD enables the C portion of the write control and read logic; each time the SR 00 line asserts, the CLK line causes a 1 to be written on track C. During the first data sector, for example, the block address shift register contains all zeros. Therefore, six zeros are written on track C as the block address.

While the block address is being written, the bit counter continues to increment and, at bit count 17, the bit counter is cleared, the word counter is incremented, and WC EQ 01 asserts. The bit counter continues and, when BC EQ 03 asserts, the block address shift register is incremented by 1, SAD is cleared, and PAR ENB (parity enable) asserts. PAR ENB is then ANDed with PAR (parity) at the write control and read logic, causing the parity bit to be written on track C. In this case, the address recorded (address 0) has an even number of 1s; therefore, PAR is asserted and a 1 is written for parity, thus maintaining odd parity.



NOTE:
TA numbers reference engineering drawings.

Figure 4-2 RS64-TA Functional Block Diagram

After parity is written, the bit counter is incremented and BC EQ 04 asserts and resets the parity logic in the block address shift register. The bit counter continues and, when BC EQ 09 asserts, it is ANDed with WC EQ 01 at the write control and read logic, causing the data marker bit to be recorded on track B. Thus, the recording of timing information on tracks B and C is completed for the first data sector.

For the remainder of the first data sector, timing information is recorded on track A only. The bit counter and word counter continue to count, however, and when the word count equals 35 and the bit equals 05, the word count decode logic asserts EOB CLR (end of block clear), which signals the end of the current sector count cycle. EOB CLR clears the bit counter and word counter to zero, thus preparing the counters to start the next count cycle. The next count cycle begins on the next clock pulse.

The logic operations performed during each successive data sector count cycle are identical to those for the first count cycle, except the block address recorded in each successive sector is increased by 1 due to incrementation of the block address shift register. Thus, the count cycle is repeated over and over until timing information is recorded on each of the 64 (0 through 63) data sectors. At the end of the 64th data sector count cycle, the block address shift register asserts LWD (last word), which clears the RUN line (disabling the clock) and enables the gap detect logic. The gap detect logic then asserts R DLY (read delay), which clears the WREN output from the write enable logic. When WREN clears, the write amplifiers are disabled (ending the record operation) and the gap detect time-out circuits are triggered.

The gap detect logic then measures the gap. As the gap detect circuits time out, the read amplifiers in the write control and read logic monitor the feedback from the disk drive's read/write heads. When timing information is detected on track A, TTA (timing track A) asserts and one of the indicator control lines (INCREASE/GAP OK/ DECREASE) asserts to indicate whether the gap meets specification. The RS64-TA then stops, having completed one write operation.

The control panel test pins are provided for checkout and maintenance. The test pins are connected to the outputs of the read amplifiers in the write control and read logic. The read amplifiers are connected directly to the disk drive's read/write heads via the write lines [AWR (1), AWR (0), AWRS (1), etc.] ; the read amplifiers read the actual A, B, and C timing tracks once they are recorded. The timing tracks can be monitored using an oscilloscope.

4.3 DETAILED LOGIC DESCRIPTION

The following paragraphs provide detailed logic descriptions of each of the functional blocks illustrated in Figure 4-2.

4.3.1 Write Enable Logic

The write enable logic initiates and terminates RS64-TA write operations (Figure 4-3). Each time the control panel PUSH TO WRITE pushbutton is depressed, the M203 flip-flop sets and triggers the CLK RUN, 50 ms one-shot and the M602, B02A, 110 ns one-shot; CLR L and CLR H assert immediately and the WREN flip-flop sets. After 50 ms, CLK RUN L asserts and triggers the MAINT ENABLE, 50 ms one-shot and the M602, B02B, 110 ns one-shot. STP L then asserts, setting the RUN flip-flop. The write enable logic remains in this state until the RS64-TA completes one write operation and the LWD L and R DLY H inputs assert. LWD L resets the RUN flip-flop, thereby inhibiting the clock; R DLY resets the WREN flip-flop, thus disabling the write amplifiers in the write control and read logic and enabling the gap detect time-out circuits.

The output of MAINT ENABLE one-shot is only effective if the control panel MAINT switch is set to MAINT.

CAUTION

The maintenance mode should only be selected when the RS64-TA is disconnected from the disk drive's timing track read/write heads. Otherwise, the timing track read/write heads may be damaged.

Setting the MAINT switch to MAINT asserts MEN L (maintenance enable) and initiates a write operation, just as depressing the PUSH TO WRITE pushbutton does. CLR RUN L asserts 50 ms later, triggering the MAINT ENABLE one-shot, which clears MEN L. After 50 ms (the 50 ms allows the RS64-TA to complete the write operation), the MAINT ENABLE one-shot resets and asserts MEN L, thereby initiating another write operation. Thus, in the maintenance mode, the RS64-TA performs write operations continuously.

4.3.2 Clock Logic

The clock logic generates timing for the RS64-TA (Figure 4-4). The assertion of RUN L enables the M401 variable clock. The control panel 50HZ/60HZ toggle switch selects different clock repetition rates in accordance with the disk drive's ac input line frequency. The control panel GAP ADJUST knob permits frequency variations of ±15% of the selected rate.

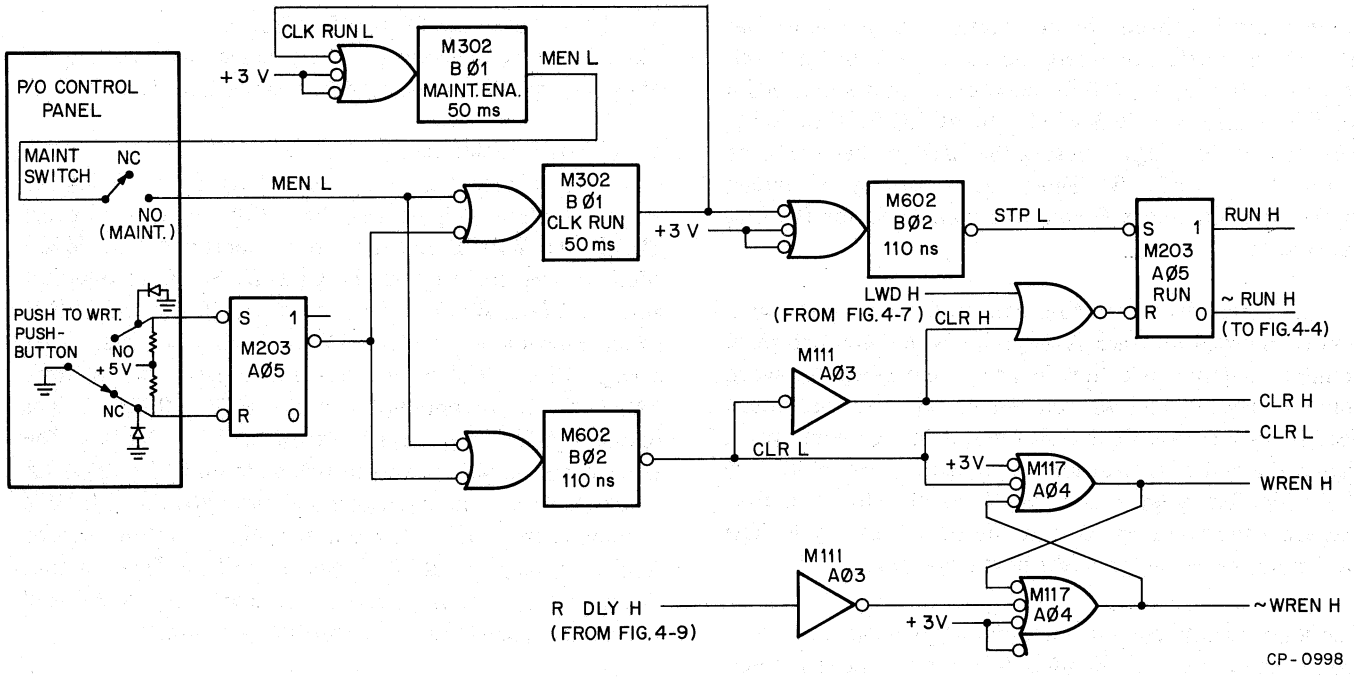


Figure 4-3 Write Enable Logic Diagram

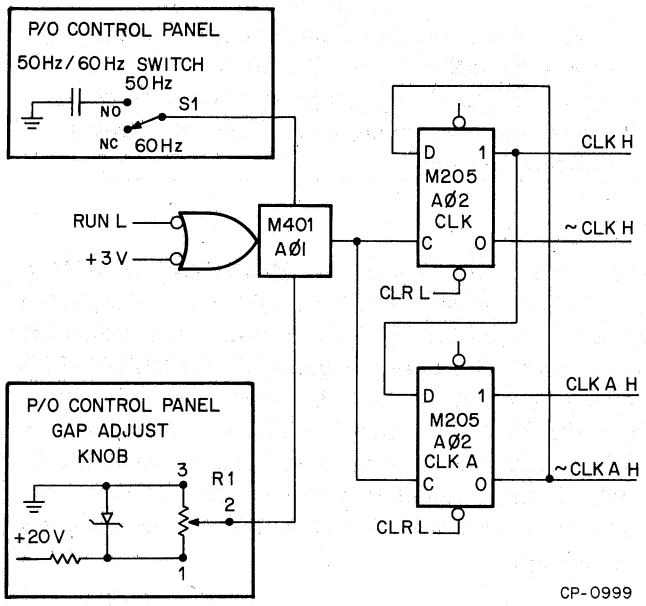


Figure 4-4 Clock Logic Diagram

The clock output flip-flops divide the clock repetition rate by two, and the output from the CLK A flip-flop lags the output from the CLK flip-flop by 90 degrees. The clock flip-flops are reset by CLR L each time a new write operation is initiated.

4.3.3 Bit Counter and Bit Count Decode Logic

The bit counter and bit count decode logic combines with the word counter to provide a timing reference within each data sector. This timing reference is used to write address and data marker bits (track B) and block addresses (track C) on the disk surface (Figure 4-5). The logic consists of an M211 binary counter and an AND gate decoder. The CLK H input steps the counter from 0 to 17_{10}. When a count of 17_{10} is reached, BC 04 H and BC 00 H are ANDed with ~ CLK H (not Clock H) to clear the counter to 0.

The counter is also cleared by other functions during a write operation. The CLR L line clears the counter each time a write operation is initiated. EOB CLR L clears the counter at the end of each block or sector.

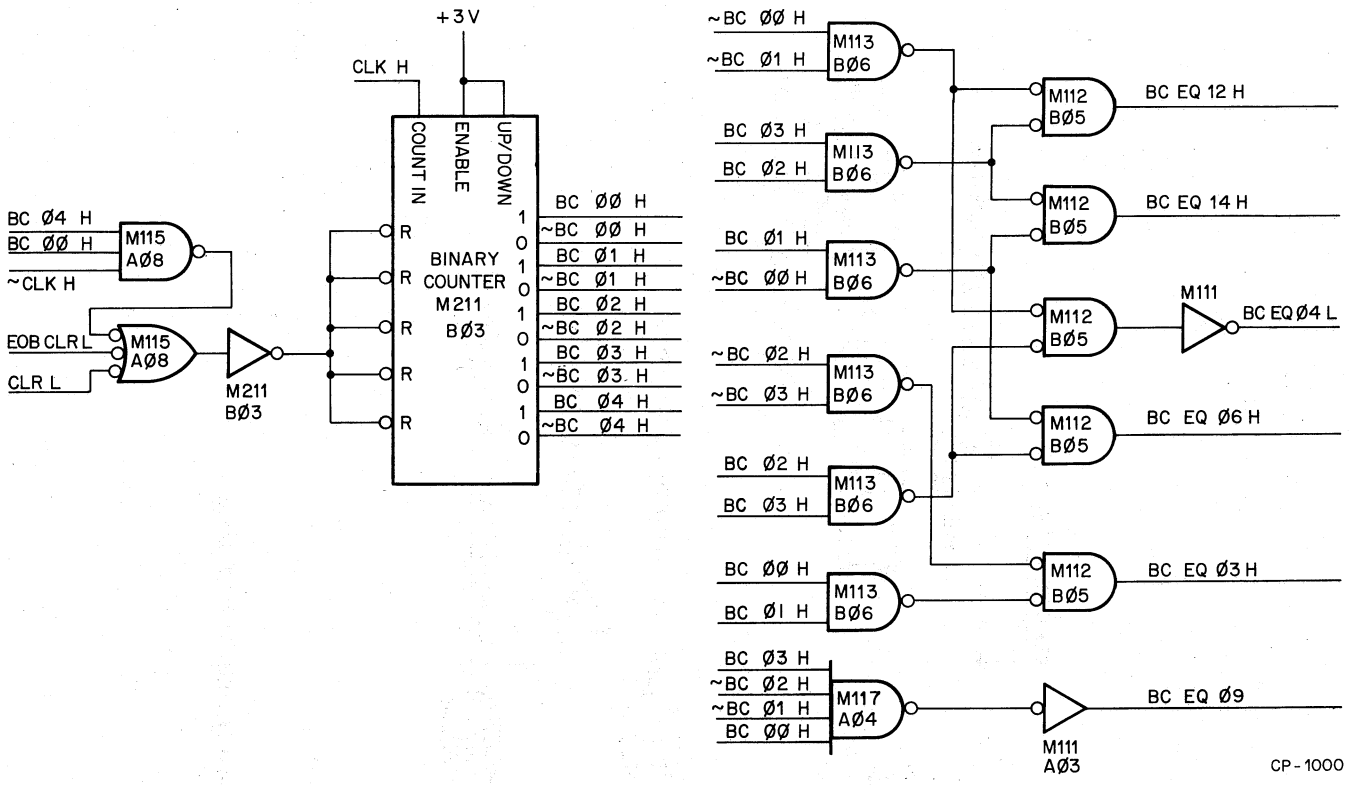


Figure 4-5 Bit Counter and Bit Count Decode Logic Diagram

4.3.4 Word Counter and Word Count Decode Logic

The word counter and word count decode logic combines with the bit counter to provide a timing reference within each data sector for writing the address and data marker bits (track B) and the block addresses (track C) on the disk surface (Figure 4-6). In addition, this logic monitors the bit count and word count to determine when to end one block count cycle and start the next.

The logic consists of an M211 binary counter, an AND gate decoder, and ST TM logic. When CLK H asserts and steps the bit counter to a count of 17_{10}, the BC EQ 00 and BC EQ 04 inputs assert, satisfying AND gate M113 and placing a low on the COUNT IN line. When CLK H clears (goes low), the COUNT IN line goes high and increments the counter by 1. In this manner, the counter is incremented from 0 to 35_{10}.

The word count decode logic monitors the bit counter and word counter outputs and generates outputs accordingly. When the word counter equals 0, WC EQ 00 asserts; when the word counter equals 1, WC EQ 01 asserts. When the word counter equals 35 and the bit counter equals 5, EOB H asserts, triggering the M502 one-shot and conditioning AND gate M113. The M502 one-shot sets the ST TM flip-flop. When ~CLK H asserts (CLK H goes low), the M113 AND gate is satisfied, EOB CLR L asserts, and the bit counter and word counter are cleared.

4.3.5 Block Address Shift Register Logic

The block address shift register generates and updates the block address and outputs that address to the write control and read logic (Figure 4-7). In addition, this logic monitors the parity of each block address recorded and provides outputs to the write control and read logic to maintain odd parity.

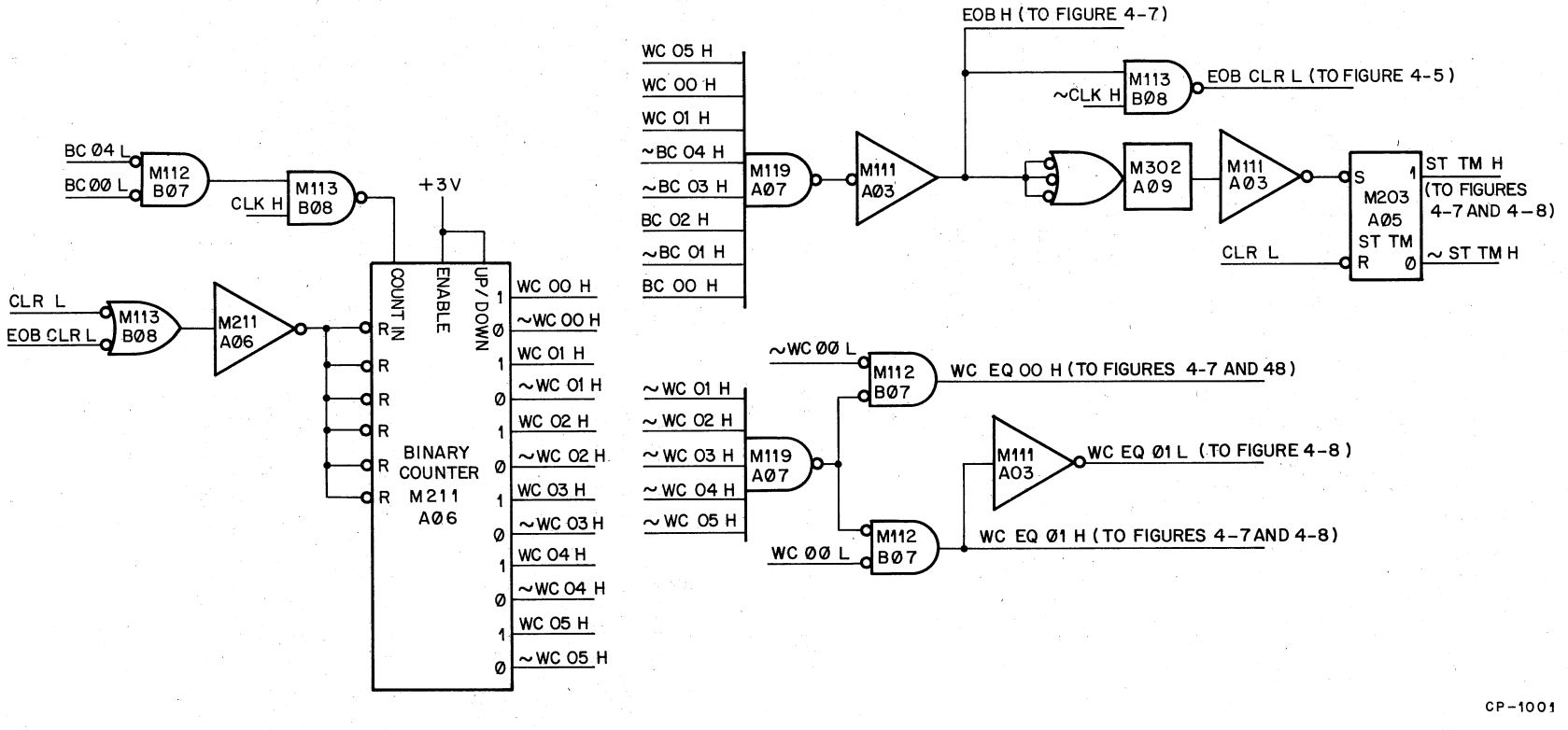


Figure 4-6 Word Counter and Word Count Decode Logic Diagram

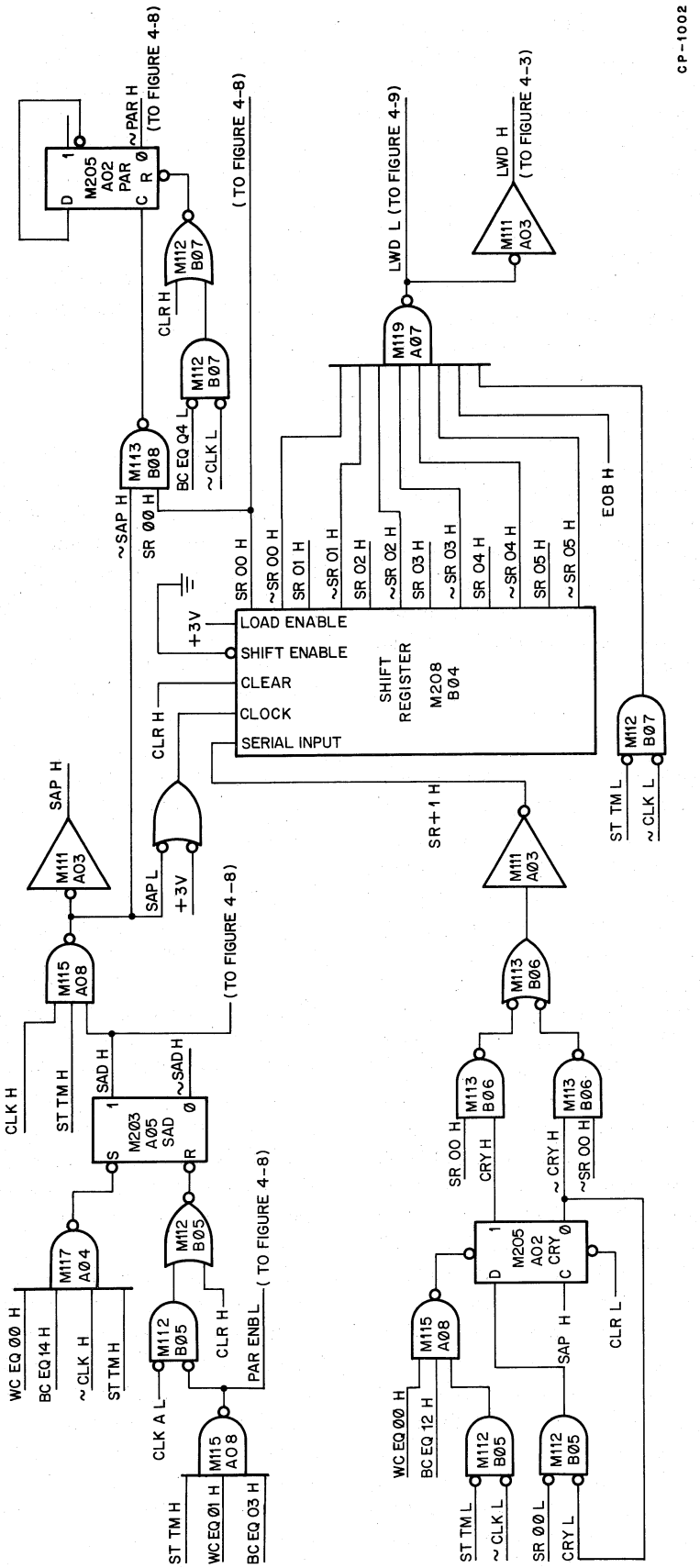


Figure 4-7 Block Address Shift Register Logic Diagram

This logic consists of a shift register, shift register incrementation logic, an AND gate decoder, and control flip-flops. When CLR H asserts at the beginning of a write operation, the shift register is cleared to zero. The logic then remains idle until the sync sector count cycle is completed. ST TM H then asserts and the bit counter counts to 12_{10}. At that point, BC EQ 12 H is ANDed with WC EQ 00 H, ST TM L, and ~CLK L to set the CRY (carry) flip-flop. The shift register is cleared at this point; therefore, SR 00 H is cleared (low). Thus the assertion of CRY H inhibits the M113 exclusive OR function and asserts SR + 1 H (shift register plus 1). The bit counter continues to count and, at a count of 14_{10}, the assertion of ~CLK H sets the SAD flip-flop, asserting SAD H. The CLK H line then asserts and is ANDed with SAD H and ST TM H to assert SAP L (shift address pulse) and SAP H. SAP L is applied to AND gate M113, B08, but has no affect because SR 00 H is cleared. If SR 00 H were asserted, the assertion of SAP L would cause the output of AND gate M113, B08 to go high and set the PAR flip-flop. SAP L is also applied to the shift register. At the shift register, the contents of each register are shifted down one bit position and due to the assertion of SR + 1 H, a 1 is loaded into bit position 05.

At the same time, SAP H clocks the CRY flip-flop, causing it to reset because AND gate M112 is inhibited by SR 00 L cleared (high), placing a low on the CRY flip-flop data input. Resetting the CRY flip-flop satisfies the M113 exclusive OR function and clears SR + 1 H. Note that every assertion of CLK H also increments the bit counter. CLK H then asserts again, the contents of the shift register are shifted down one bit position, a 0 is loaded into bit position 05, and the bit counter is stepped to a count of 16_{10}. The next assertion of CLK H shifts the register contents for a third time and steps the bit counter to 17_{10}. The word counter is then stepped to a count of 01 and the bit counter is cleared to 0. Three more clock pulses then occur, shifting the register for the fourth, fifth, and sixth lines (shifting the 1 into bit position 00) and incrementing the bit counter to a count of 03. BC EQ 03 then asserts and is ANDed with ST TM H and WC EQ 01 to assert PAR ENB L. PAR ENB L is output to the write control and read logic (Figure 4-8), where it is ANDed with ~PAR H to write the parity bit. In this case, PAR H is asserted (block address contains an even number of 1s); therefore, the parity bit will be recorded as a 1. In addition, PAR ENB L is ANDed with CLK A L (Figure 4-1) to reset the SAD flip-flop, thereby disabling the shift register output (SR 00) to the write control and read logic. The next assertion of CLK H steps the bit counter to a count of 04. ~CLK L then asserts and pulses the reset side of the PAR flip-flop. In this case, the flip-flop is already reset so this has no affect.

The block address shift register logic performs the operation described in the preceding paragraph 64_{10} times (once for each data sector). At the end of the 64th data sector, the shift register contains a block address of 0. Therefore, when the EOB H line asserts to end the block count cycle, the M119 AND gate is satisfied, asserting LWD L and LWD H. The assertion of the LWD lines terminates the write operation.

4.3.6 Write Control and Read Logic

The write control and read logic controls the current flow through the timing track read/write heads and monitors feedback from those heads for purposes of measuring the gap (Figure 4-8).

The logic is enabled when the control panel WRITE ENABLE toggle switch is set to the up position and the WREN H line asserts. With WREN H asserted and the write flip-flops (WFA, WFB, and WFC) reset (CLR L resets the flip-flops), the 0 outputs [AWR (0) H, AWRS (0) H, BWR (0) H, etc.] are asserted and all zeroes are written on the disk surface for approximately 50 ms. Thus, the disk is erased. After 50 ms, the clock is enabled and CLK H begins to set and reset the WFA flip-flop, causing current reversals in the track A read/write heads. Each current reversal records a 1 on the disk surface. Thus, track A is continuously recorded until the WREN H line clears or the control panel WRITE ENABLE toggle switch is set to the down position.

While track A records continuously, tracks B and C only record a few bits in each data sector. Track B only records two bits per data sector (address and data markers). Track C only records nine bits per data sector (block address). When the block count cycle for the sync sector is complete, the word counter and word count decode logic (Figure 4-6) asserts the ST TM lines, thereby enabling the track B and track C poritons of the write control and read logic. When the bit counter reaches a count of 06, BC EQ 06 H is ANDed with ST TM H and WC EQ 00 H, satisfying OR gate M113 and placing a high on AND gate M113. ~CLK H then asserts, satisfying AND gate M113 and placing a low on the WFB flip-flop clock input. On the next clock pulse, ~CLK H clears, placing a high on the flip-flop clock input and thereby setting the flip-flop. A current reversal results in the track B read/write heads and a 1 is written for the address marker bit. The bit counter continues and, at a count of 12, BC EQ 12 H is ANDed with ST TM H and WC EQ 00 H to enable the clock to the WFC flip-flop; ~CLK H clears and sets the WFC flip-flop, causing a 1 to be written for the first of the two sync bits preceding the block address. On the same clock pulse, the bit counter is stepped to a count of 13_{10}, BC EQ12 H is cleared, and the M113 AND gate connected to the WFC flip-flop is disabled.

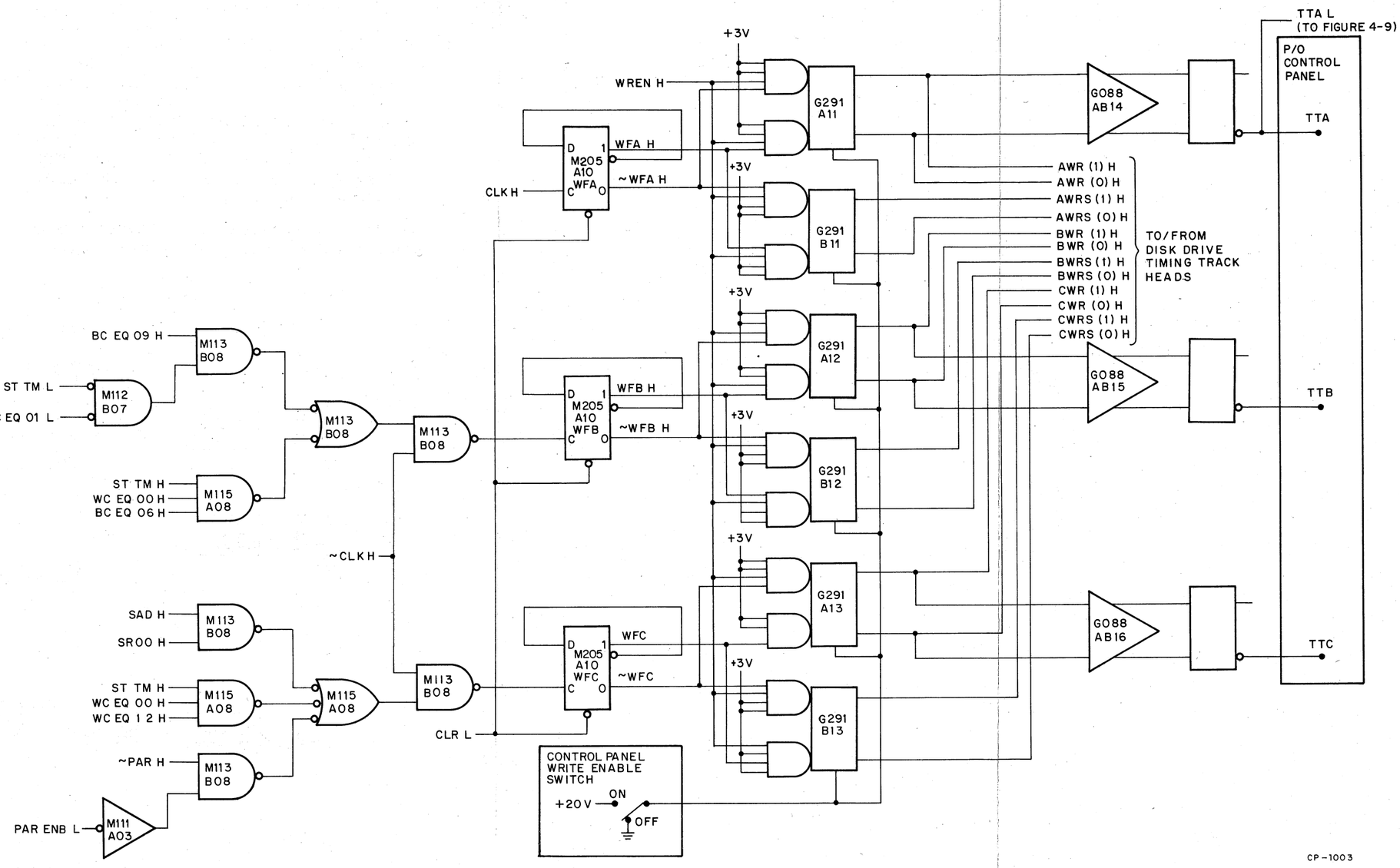


Figure 4-8 Write Control and Read Logic Diagram

Therefore, on the next clock pulse, the WFC flip-flop remains set (no current reversal occurs) and a 0 is written as the second sync bit. Note that the bit counter was stepped to a count of 14_{10} by the same clock pulse to record a 0 for the second sync bit. Therefore, SAD H is asserted and ANDed with SR 00 H. The next six clock pulses then alternately reset and set the WFC flip-flop each time the SR 00 H line asserts. On the sixth clock pulse, the PAR ENB L line asserts and is ANDed with ~PAR H. If the block address just recorded had an even number of 1s, ~PAR H is asserted and the next clock pulse resets the WFC flip-flop, thereby recording a 1 for the parity bit. Thus the block address recording is complete.

When the bit counter reaches a count of 09, BC EQ 09 is ANDed with WC EQ 01 and ST TM and the WFB flip-flop is reset by the next clock pulse, causing a 1 to be recorded for the data marker. This completes B and C track recording for one data sector.

The G088 read amplifiers monitor the timing tracks. After the write operation has been performed, the track A read amplifier detects the timing information and outputs TTA L to the gap detect logic, thus signaling the end of the gap.

4.3.7 Gap Detect Logic

The gap detect logic measures the width of the gap and drives control panel indicators to indicate whether the gap meets specifications. The logic consists of time-out circuitry, lamp driver circuitry, and a read delay one-shot to prevent false triggering (Figure 4-9).

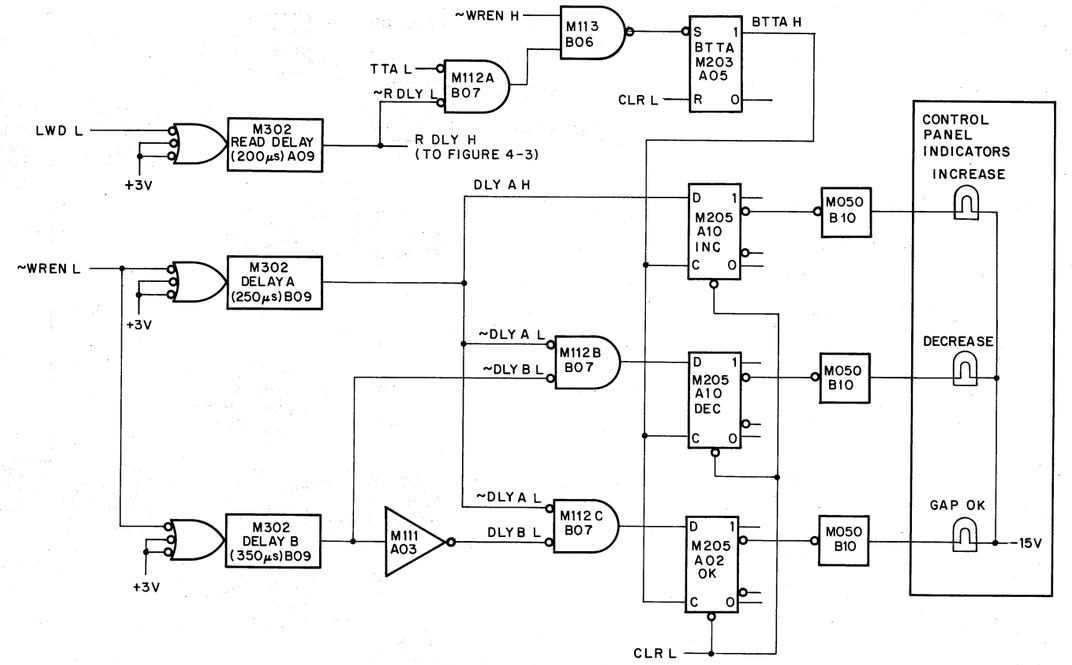
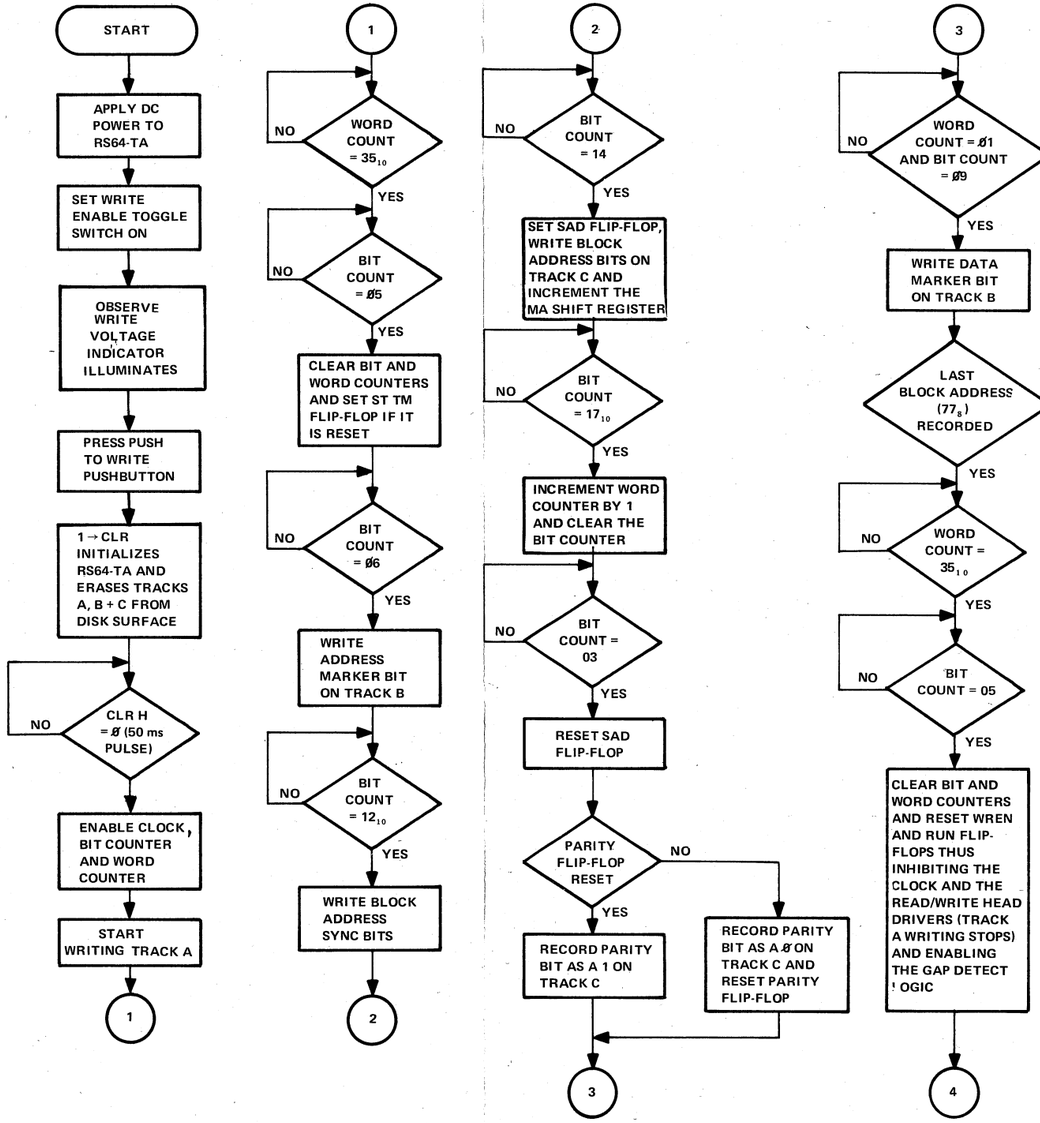


Figure 4-9 Gap Detect Logic Diagram

When the write operation is terminated, the gap detect logic is enabled. At the end of the last data sector, the block address shift register logic asserts LWD L, which triggers the 200 μs, read delay one-shot, thereby clearing ~R DLY L. With ~R DLY L cleared, AND gate M112A is inhibited (to prevent false triggering by noise caused by the write heads turning off) and the write enable logic WREN flip-flop (Figure 4-3) is reset, asserting the ~WREN inputs to the gap detect logic. The assertion of the ~WREN lines triggers the time-out one-shots (delay A and delay B) and also enables the M113 AND gate. After 200 μs, ~R DLY L asserts, enabling the M112A AND gate. When TTA L asserts (indicating the end of the gap), the BTTA (timing track A) flip-flop sets, BTTA H asserts, and the three lamp driver circuit flip-flops are clocked. If the gap is less than 250 μs wide, the DLY A H (delay A) line is asserted, the INC (increase) flip-flop is set, and the control panel INCREASE indicator illuminates. If the gap is more than 350 μs wide, the ~DLY A L and ~DLY B L lines are asserted, and the DEC (decrease) flip-flop sets. If the gap is wider than 250 μs but less than 350 μs, the OK flip-flop sets.

4.4 FLOW DIAGRAM DESCRIPTION

The following flow diagram (Figure 4-10) provides a step-by-step explanation of the RS64-TA sequence of operation.



NOTES:

1. During the sync sector only Track A is recorded on the disk surface.
2. If the INCREASE or DECREASE indicator illuminated at the end of the write operation, the GAP ADJUST KNOB should be adjusted and the PUSH TO WRITE pushbutton depressed to perform another write operation.

CP-1006

Figure 4-10 RS64-TA Operation Flow Diagram

CHAPTER 5
MAINTENANCE

5.1 SCOPE

This chapter lists the test equipment required and provides a complete description of RS64-TA maintenance procedures, including a preventive maintenance schedule and a corrective maintenance troubleshooting flow diagram.

5.2 MAINTENANCE PHILOSOPHY

Basically, RS64-TA maintenance consists of preventive and corrective maintenance procedures and a maintenance log. The preventive maintenance procedures are performed regularly in an attempt to detect any damage caused by improper handling of the unit. The corrective maintenance troubleshooting flow diagram is provided to aid service personnel in isolating and repairing faults in the circuitry. The maintenance log (included in the back of this manual) is used to record all maintenance action and aid in detecting any component failure pattern that may develop.

5.3 TEST EQUIPMENT REQUIRED

RS64-TA maintenance procedures require the test equipment, tools, and materials listed in Table 5-1, in addition to standard hand tools, cleaners, test cables, and probes.

5.4 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed at periodic intervals or whenever the timing track writer is shipped to ensure proper equipment operation and minimum unscheduled maintenance. These tasks include visual inspection and operational checks. Table 5-2 provides a recommended preventive maintenance schedule.

5.5 CORRECTIVE MAINTENANCE

The following information will aid the service technician in isolating failing RS64-TA components. The information is presented in flow diagram form so that correctly functioning RS64-TA circuitry is systematically eliminated. Using the flow diagram (Figure 5-1) and logical deductive reasoning, faulty components can be located.

Table 5-1
Test Equipment Required

Equipment	Manufacturer	Designation
DECdisk System	Digital	RC11/RS64
Oscilloscope	Tektronix	Type 453 or equivalent
X10 Probe (2)	Tektronix	P6008
Multimeter	Triplett/Simpson	Model 310/Model 260
Module Extender	Digital	W974 (Dual Height)

Table 5-2
Preventive Maintenance Schedule

Performance Interval	Test or Procedure
Monthly	Visually inspect for physical damage; correct if required.
Monthly	Clean externally.
Monthly	Check that all modules are properly seated in the wired assembly.
Quarterly	Clean internally with vacuum cleaner or a soft brush.
Quarterly	Check for looseness of the knobs, switches, and indicators.
Quarterly	Perform RS64-TA Acceptance Test Procedure (Paragraph 2.2).

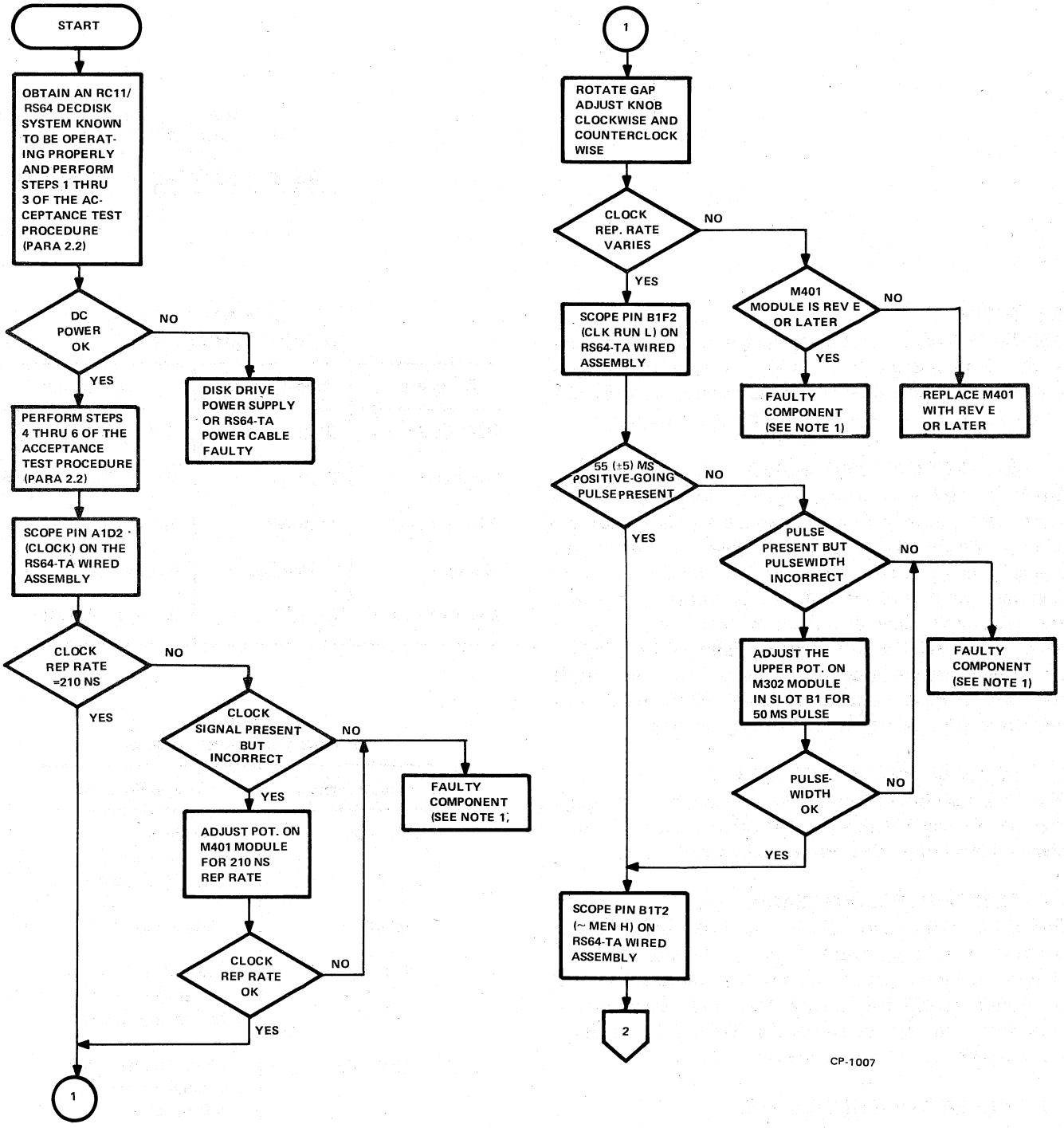


Figure 5-1 RS64-TA Troubleshooting Flow Diagram (Sheet 1 of 6)

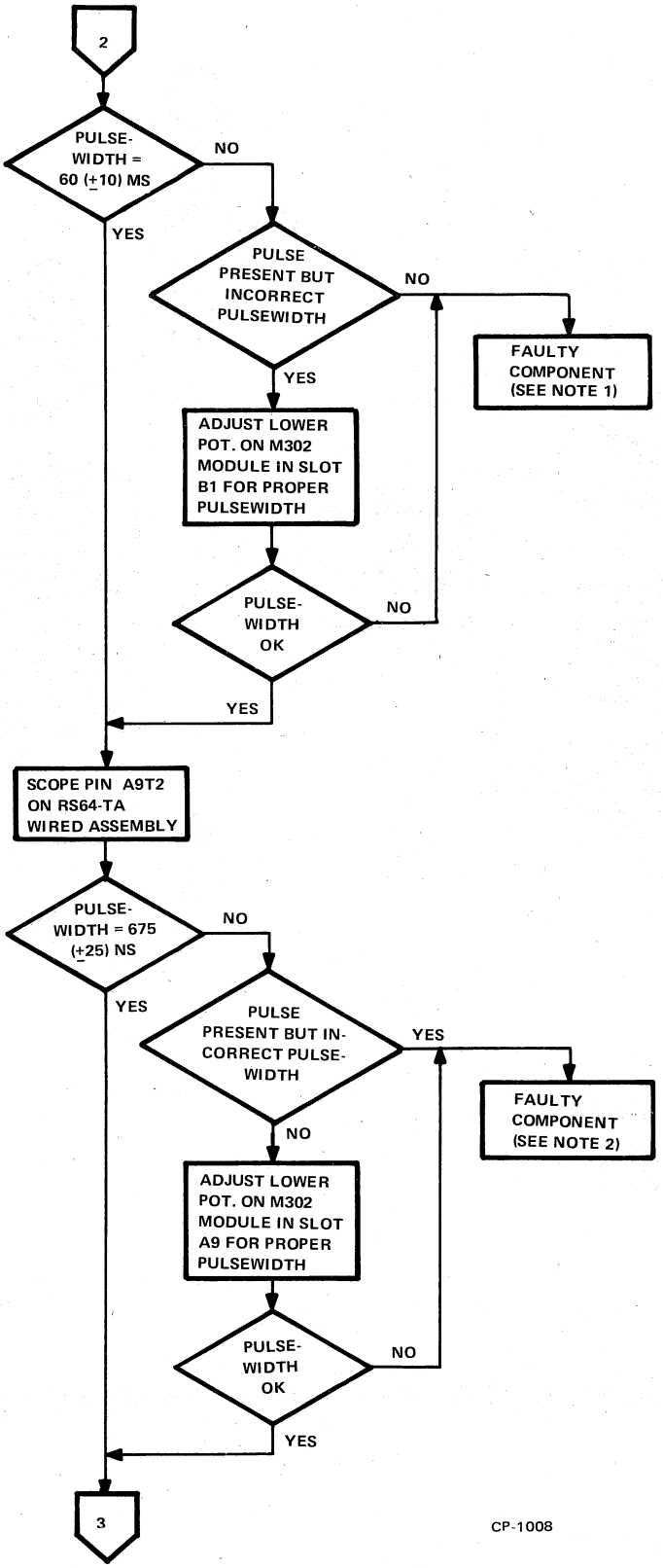


Figure 5-1 RS64-TA Troubleshooting Flow Diagram (Sheet 2 of 6)

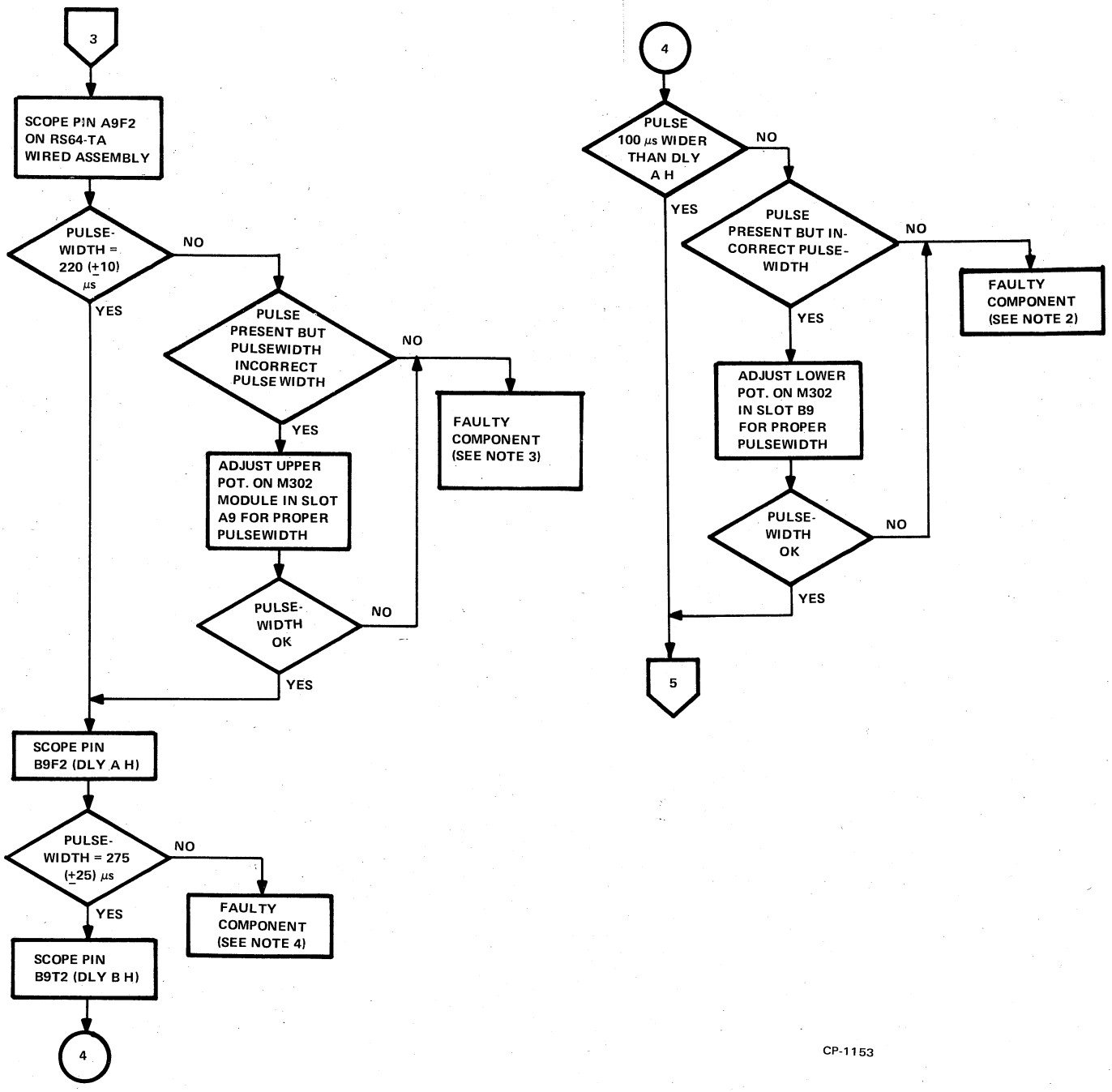


Figure 5-1 RS64-TA Troubleshooting Flow Diagram (Sheet 3 of 6)

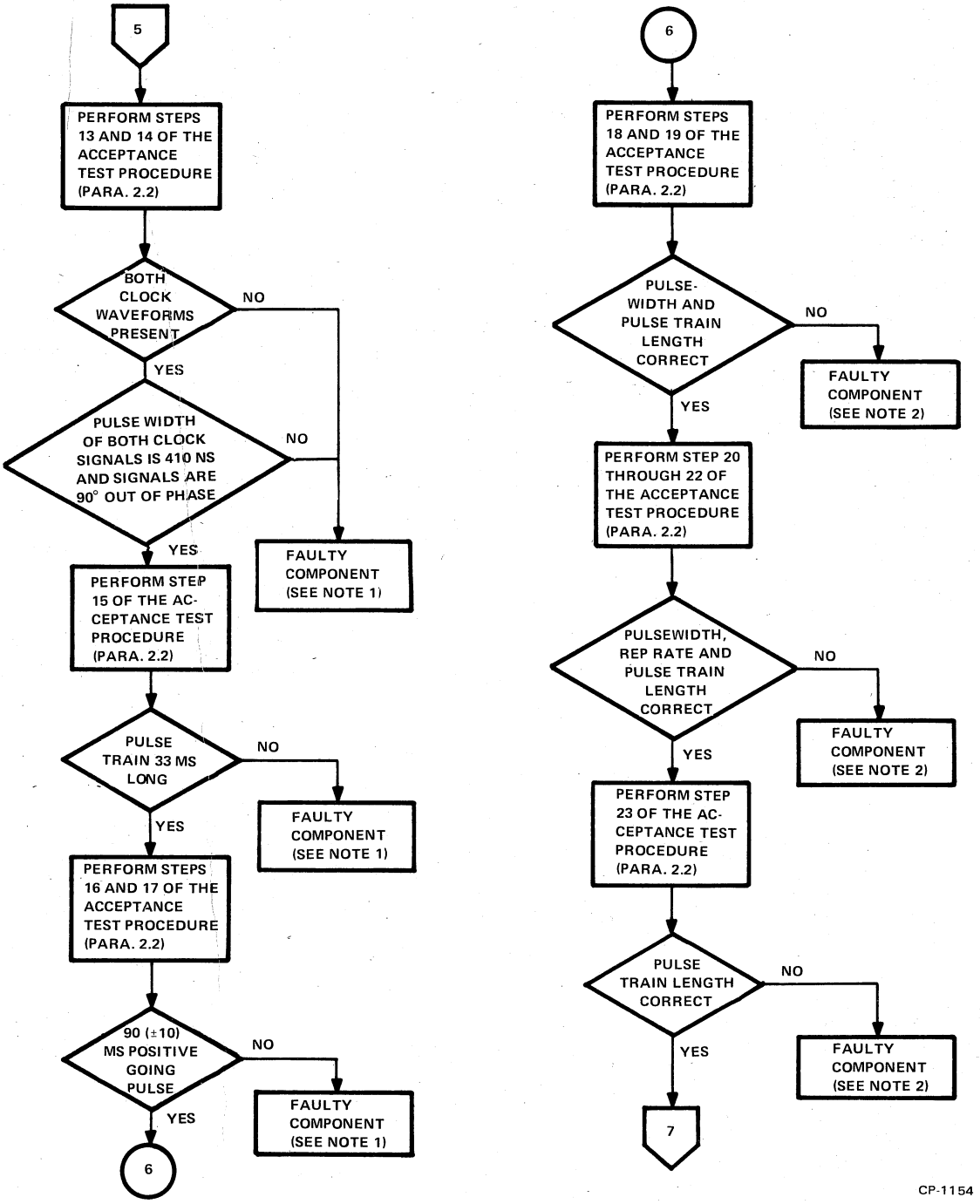


Figure 5-1 RS64-TA Troubleshooting Flow Diagram (Sheet 4 of 6)

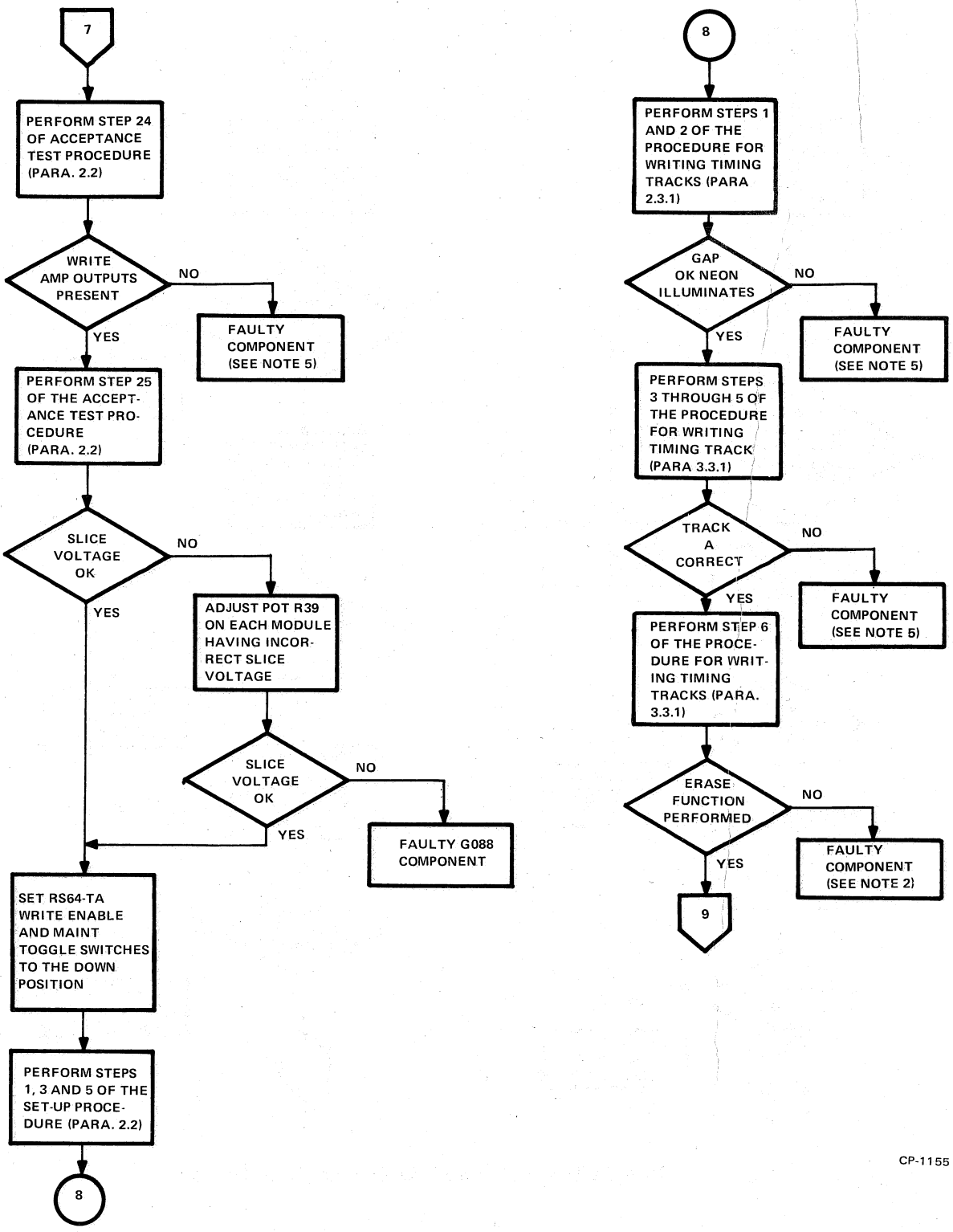
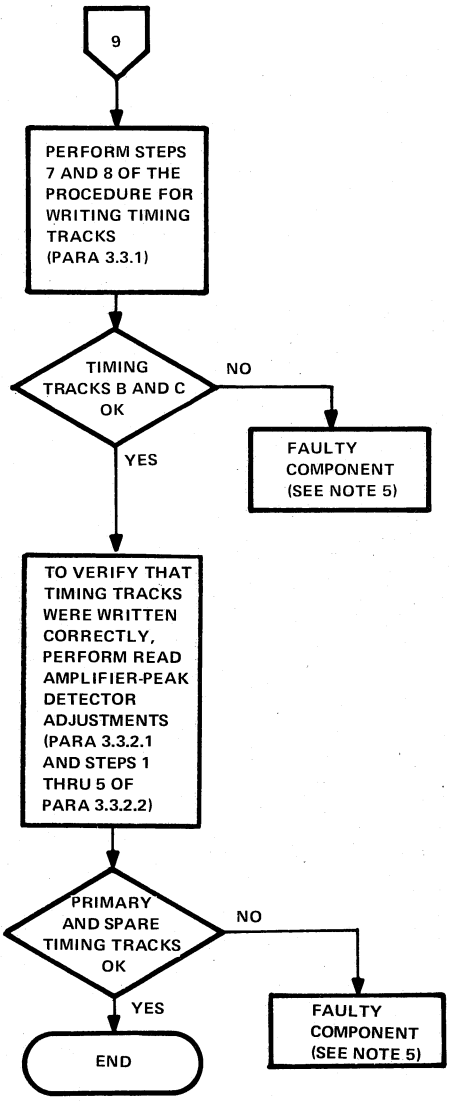


Figure 5-1 RS64-TA Troubleshooting Flow Diagram (Sheet 5 of 6)



NOTES:

1. Refer to RS64-TA Operation Flow Diagram (Figure 4-10) and engineering drawing D-BS-RS64-TA-03 and isolate the fault.
2. Refer to RS64-TA Operation Flow Diagram (Figure 4-10) and engineering drawings D-BS-RS64-TA-03 and 04 and isolate the fault.
3. Refer to RS64-TA Operation Flow Diagram (Figure 4-10) and engineering drawings D-BS-RS64-TA-04 and 05 and isolate the fault.
4. Refer to RS64-TA Operation Flow Diagram (Figure 4-10) and engineering drawings D-BS-RS64-03 and 05 and isolate the fault.
5. Refer to RS64-TA Operation Flow Diagram (Figure 4-10) and engineering drawings D-BS-RS64-TA-03, 04 and 05 and isolate the fault.

CP-1156

Figure 5-1 RS64-TA Troubleshooting Flow Diagram (Sheet 6 of 6)

APPENDIX A
MODULE DESCRIPTIONS

The RS64-TA contains 16 types of logic modules. This appendix provides detailed information on each type. The modules are discussed in the following order:

G088 Read Amplifier-Peak Detector

G291 Disk Writer

M050 50 mA Indicator Driver

M111 Inverter

M112 NOR Gate

M113, M115, M117, M119 NAND Gates

M203 8 R/S Flip-Flops

M205 General Purpose Flip-Flops

M208 8-bit Buffer/Shift Register

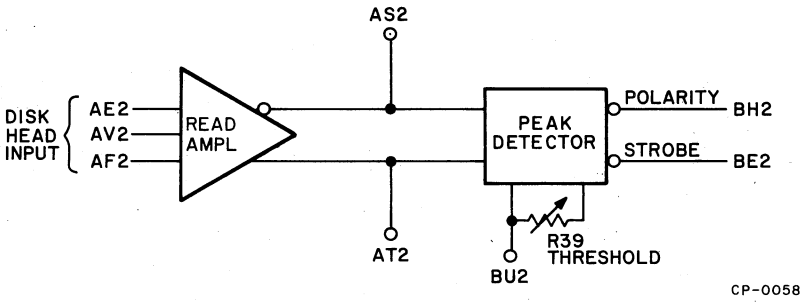
M211 Binary Up/Down Counter

M302 Dual Delay Multivibrator

M401 Variable Clock

M602 Pulse Amplifier

G088 READ AMPLIFIER-PEAK DETECTOR



G088 Read Amplifier-Peak Detector Simplified Diagram

The read amplifier-peak detector reconstructs the digital form of bipolar analog pulses read from disk timing and data tracks. Disk head inputs are provided in differential form and all outputs are TTL compatible.

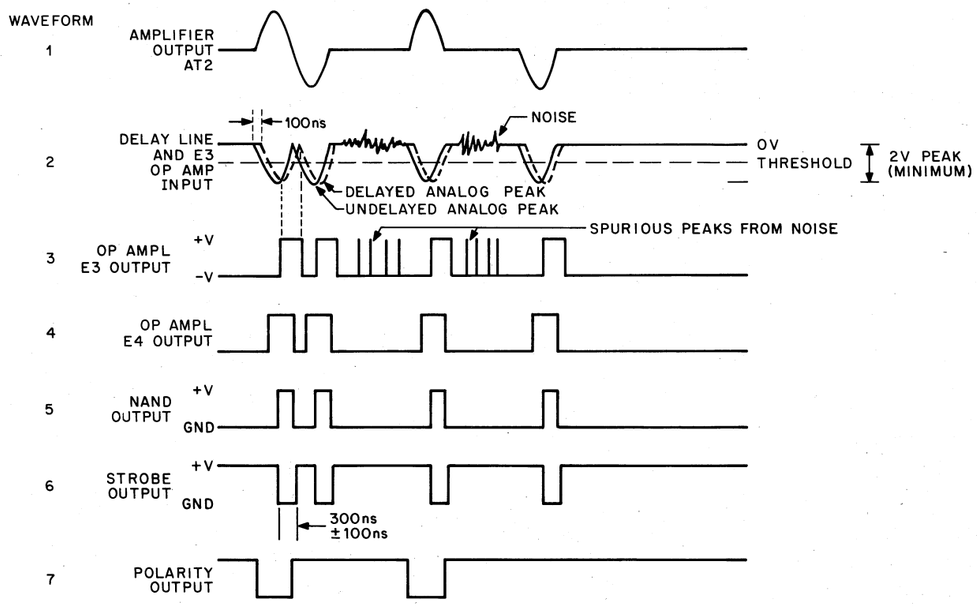
Functionally, the G088 module consists of a differential amplifier and a peak detector. Drawing DS-C-G088-0-1 is a schematic of the G088 module.

The read amplifier portion is a 3-stage, discrete-component differential amplifier (Q1 through Q6) with a 3 dB bandwidth from 60 kHz. The amplifier has linear gain characteristics (up to a maximum gain of 1000) for low-level inputs (up to 10 mV) and nonlinear gain characteristics (gain compression) to prevent peak distortion at higher level inputs. Diodes D5, D6, D10, and D11 provide the gain compression features.

The differential output of the amplifier is ac-coupled to the peak detector. The amplifier output and the waveforms for the peak detector are shown below. The peak detector portion detects the peaks of the bipolar pulses provided by the read amplifier and generates a 300-ns, negative-true strobe pulse for each peak. It also generates a polarity output denoting the polarity of the peak; a negative pulse denotes a positive polarity input pulse. Two test points (AS2 and AT2) permit monitoring of the amplified output.

Transistor stages Q8 and Q9 (with diodes D12 and D13) rectify the bipolar pulse input and provide a single-ended signal to the 100-ns delay line and amplifier E3. Peak detection is accomplished by delaying the analog input by 100 ns then comparing the magnitude of the delayed signal with the undelayed signal. Stage E3 functions as an analog voltage comparator that is operated open-loop. Its output saturates positive whenever the delayed analog signal is more negative than the undelayed analog signal. (See G088 waveforms.) Conversely, its output is negative whenever the difference in the analog inputs is zero or the undelayed input is more negative than the delayed input. Thus, its output approximates a digital form and is positive for each analog peak.

When both the delayed and undelayed analog inputs are at zero (no peaks), any noise that exceeds the input threshold of E3 causes spurious peaks in its output. To eliminate this aspect, the delayed analog signal is compared with a voltage reference (provided by R39 and R42) at operational amplifier E4 and the output of E4 remains negative unless the analog input exceeds the threshold reference. This threshold is set such that noise peaks cannot drive the output of E4 positive, yet data peaks can. Since the output of E4 is ANDed with the output of E3, the net effect cancels noise peaks in the output of NAND gate E1 (Waveform 5, G088 waveforms). Test point BU2 is provided for adjusting the threshold. This reference is set to the midpoint between maximum noise peaks and minimum data peaks. Nominally, this reference is −1.2 V.



CP-0084

G088 Read Amplifier-Peak Detector Waveforms

The pulse width of the strobe output is standardized by one-shot E2. This circuit, triggered by a negative transition, produces a nominal 300-ns strobe pulse. The leading edge of this pulse denotes the data peak position. This pulse is inverted for a negative-true strobe output (Waveform 6, G088 waveforms).

Transistor stage Q7 produces a polarity pulse for each positive pulse in the disk head input. The output of Q7 is inverted for a negative-true pulse. This pulse has a duration corresponding to the width of the input pulse.

Specifications

Inputs

Pin	Use	Drive or Load
AE2, AF2	Head Differential Input	5 to 10 mV
AV2	Head Center Tap	

Outputs

BE2	Strobe (300 ± 100 ns)	10 TTL loads*
BH2	Polarity	10 TTL loads
AS2, AT2	Read Amplifier Output Test Points	
BU2	Peak Detector Threshold Test Point	

Power

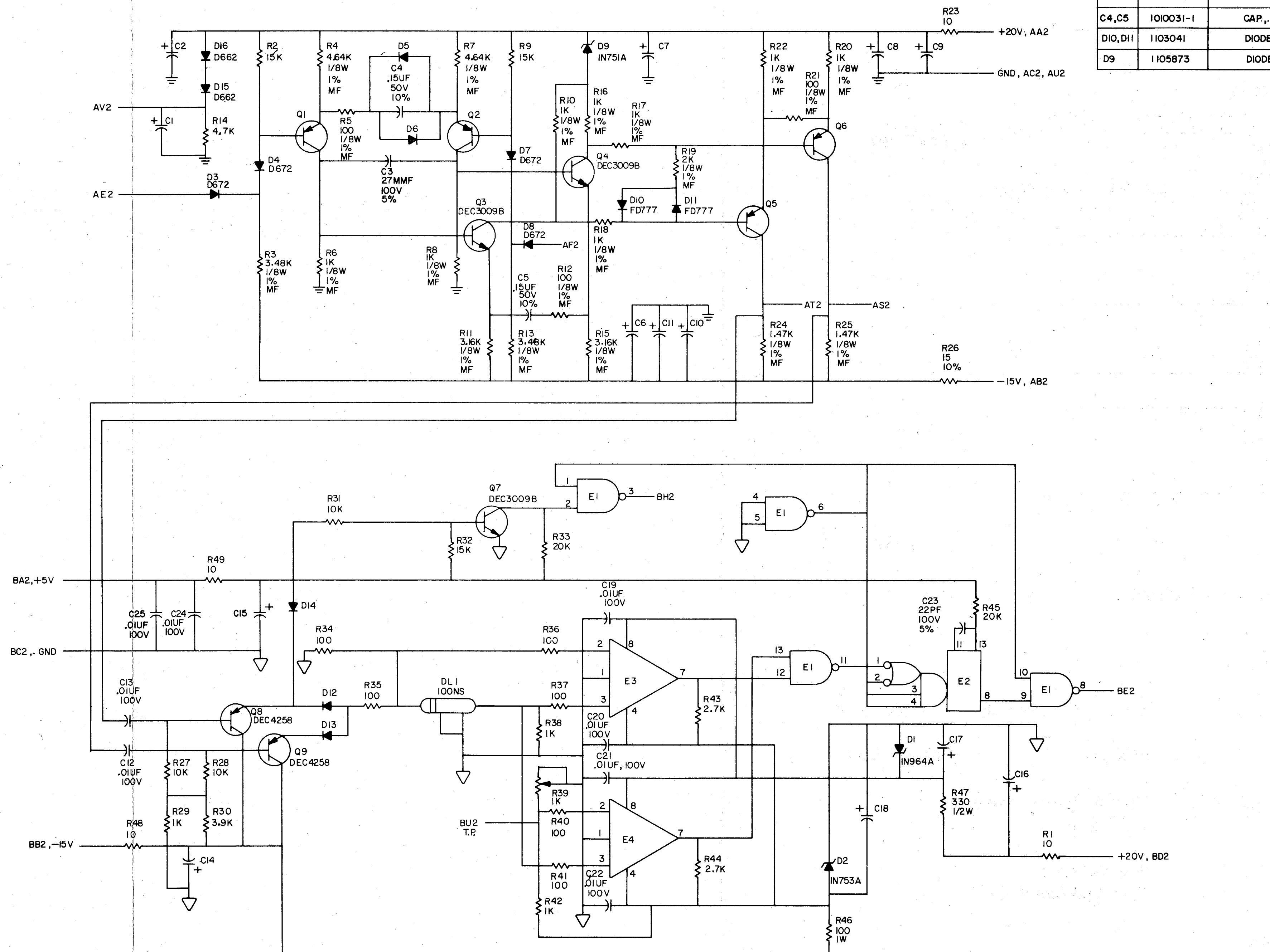
BA2	25 mA at +5 V
AB2, BB2	60 mA at -15 V
AC2, BC2	GND
AA2, BD2	60 mA at +20 V

*One TTL unit load is 1.6 mA (maximum).

D	CS	G088-0-1	H

ALLOWABLE SUBSTITUTION LIST

COMP. REF.	ORIGINAL PART NO.	SUBSTITUTE PART DESCRIPTION	SUBSTITUTE PART PART NO.	ITEM NO.
C4,C5	1010031-1	CAP.,.1UF, 50V, 10%	1010031-2	10
D10,D11	1103041	DIODE D333	1109072	15
D9	1105873	DIODE 5.1V, 2%, 400MW	1110925	17



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE 6.8UF, 35V, 20%
DIODES ARE D664
TRANSISTORS ARE DEC6534C
POTENTIOMETER IS A 1K, 3/4W, 76PR
DEC7400 = E1
DEC9601 = E2
UA710 = E3, E4
PIN 7 = GND, PIN 14 = +5V ON E1 AND E2

REVISIONS

DRN.	DATE 1-6-71
CHKD.	DATE 1-15-71
ENG.	DATE 1/19/71
PROD.	DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	IN3606	D672	IN3653
D662	IN645	IN751A	SAME
IN964A	SAME	DEC3009B	2N3646
IN753A	SAME	DEC6534C	NONE
FD777	SAME	DEC4258	2N4258

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE READ AMP PEAK DETECTOR G088

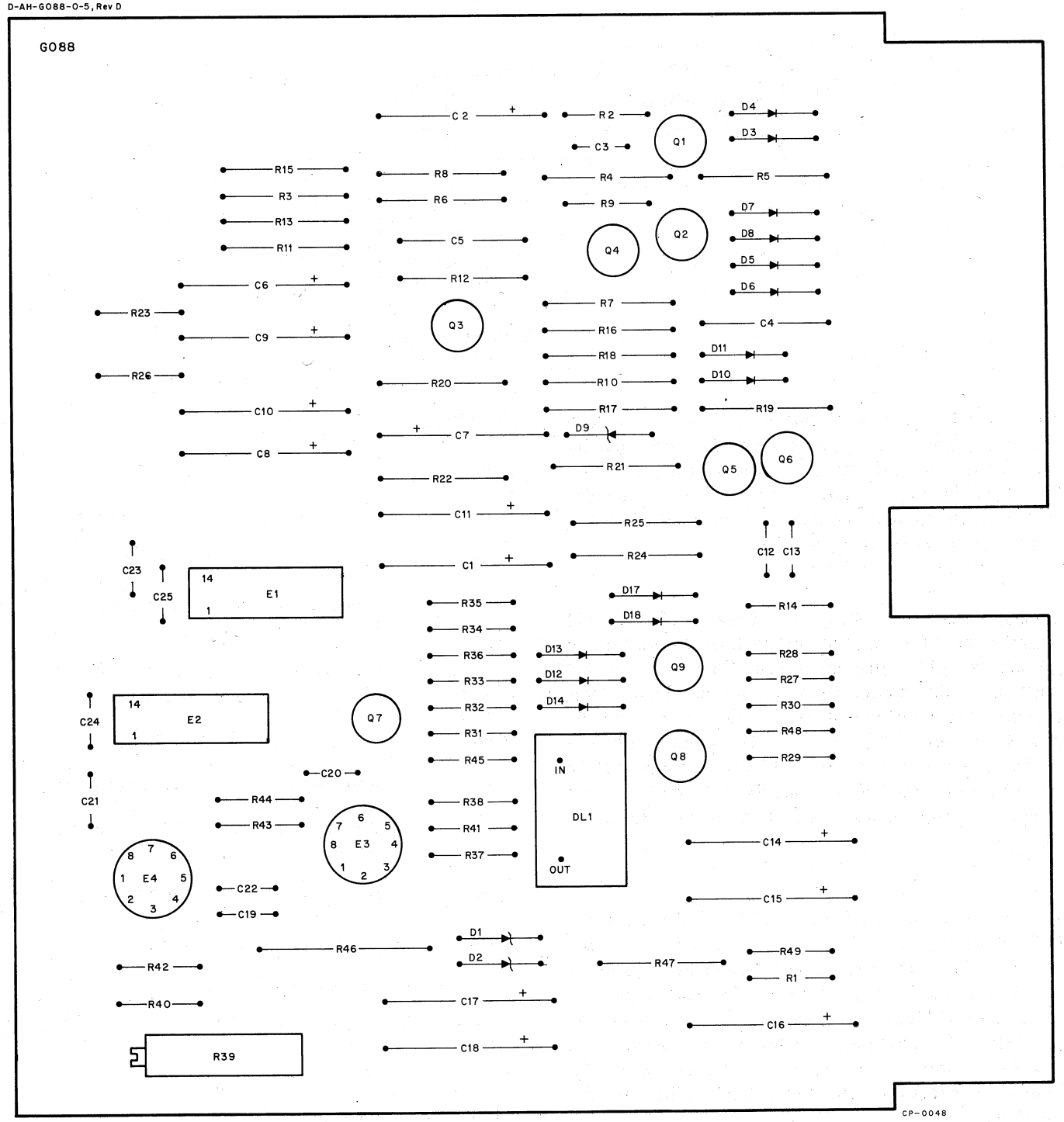
SIZE	CODE	NUMBER	REV.
D	CS	G088-0-1	H

PRINTED CIRCUIT REV. E

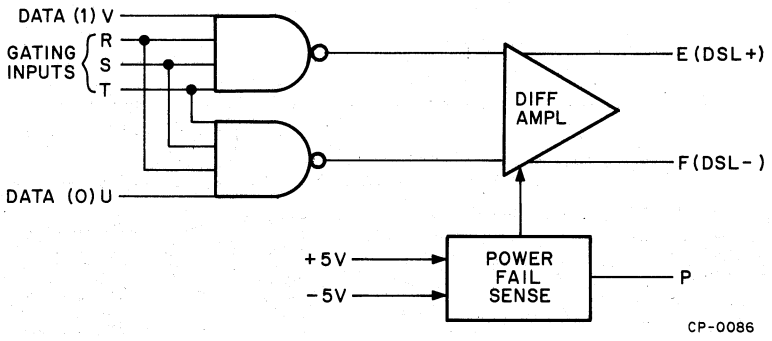
DEC FORM NO. DEB 110

D-AH-G088-0-5, Rev D

G088



G291 DISK WRITER



G291 Disk Writer Simplified Diagram

The disk writer records information on a disk. Functionally, it consists of an 80-mA differential-current amplifier with two 4-input AND gates for accepting complementary TTL data inputs (and gating signals). The module also contains a power-fail sensor that holds the writer off during power-up or power-down sequencing.

Transistor stages Q1 through Q4 (Drawing CS-G291-0-1) comprise the differential-current amplifier. Stages Q1 and Q4 are the differential input pair. Stages Q2 and Q3 function as the current sinks for writing. These stages complete the write current path between −15 V and the data sense lines (DSL). With the data input to pin V a logical 1 (and gating inputs at +3 V), Q2 completes the current path for the DSL (+) line. Similarly, with the data complement at pin U a logical 1, Q3 connects −15 V to the DSL (−) line.

Transistors Q5 and Q6 (with breakdown diodes D3 and D17) monitor the +5 V and −15 V for a power fail condition. When the sum of these potentials drops below 16.4 V, Q2 and Q3 are clamped off. This feature prevents the disk writer from recording extraneous information on the disk during power-up or power-down sequencing. A power fail output is also made available at pin P. This output is low (0 V) whenever power is below the power-fail threshold.

Specifications

Inputs

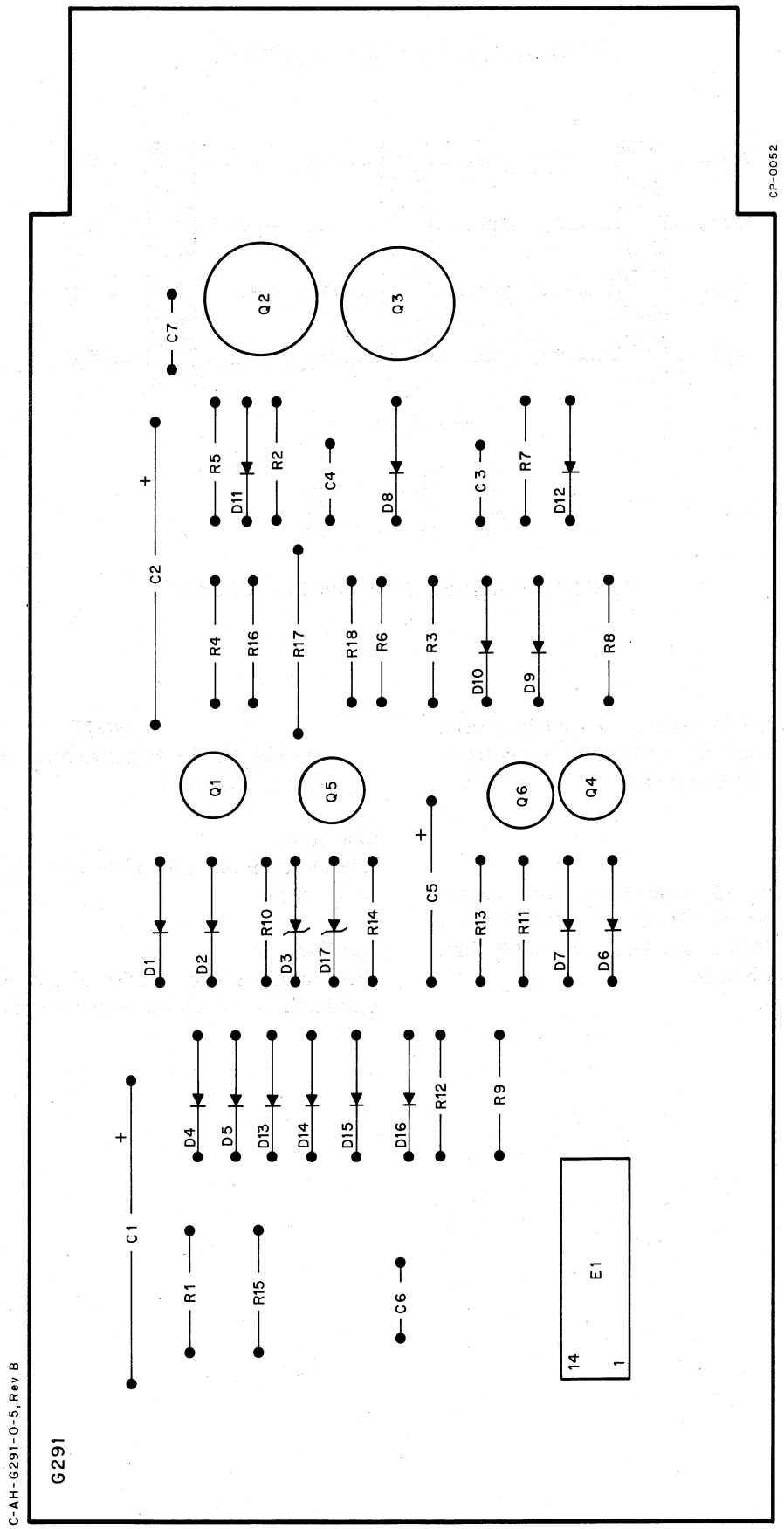
Pin	Use	Drive or Load
V2	Data Input	1 TTL load
U2	Complementary Data Input	1 TTL load
R2, S2, T2	Write Enable	2 TTL loads each

Outputs

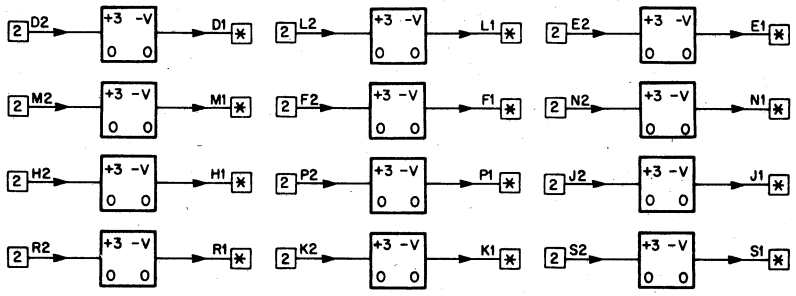
E2	Write Output	80 mA (nominal)
F2	Complementary Write Output	80 mA (nominal)
P2	Power Fail	10 TTL loads

Power

A2	30 mA at +5 V
B2	85 mA at −15 V
C2	GND
D2	1 mA at +20 V


G291
C-AH-G291-0-5, Rev B
CP-0052
C1
C2
C3
C4
C5
C6
C7
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
Q1
Q2
Q3
Q4
Q5
Q6
E1
14
1

M050 50 MA INDICATOR DRIVER



Volts	Power mA (max.)	Pin
+5	47	A2
GND		C2
−15	16	B2

M050 50 mA Indicator Driver Simplified Diagram

The M050 is a single-height module. It contains twelve transistor inverters that can drive miniature incandescent bulbs such as those on an indicator panel.

Applications

The M050 is used to provide drive current for a remote indicator, such as Drake 11-504, Dialco 39-38-375, or Digital Indicator type 4908, or as a level converter to drive 4917 and 4918 indicator boards.

NOTE

Do not use the M050 to drive inductive loads (relays, solenoids).

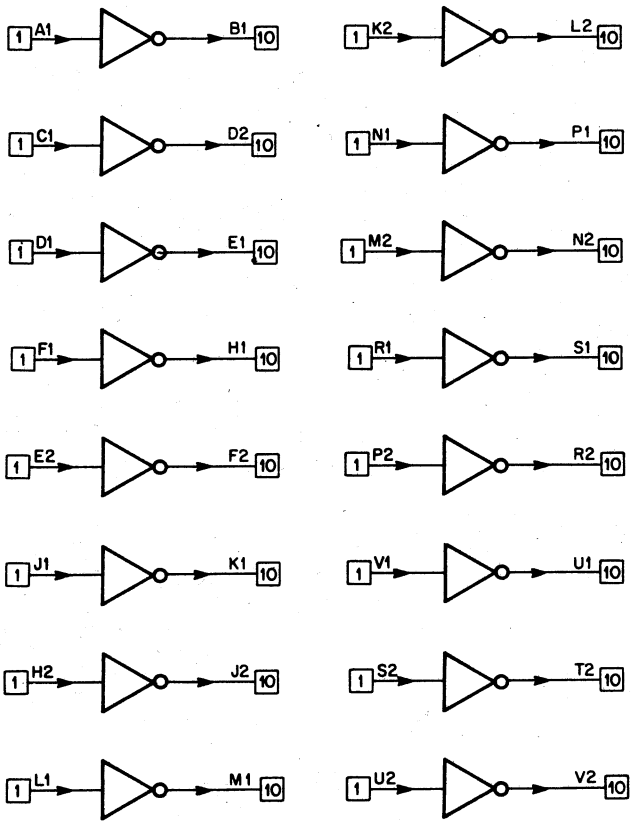
Functions

A low level on the input of the driver causes current to flow in the output.

Specifications

Each output is able to drive 50 mA into an external load connected to any voltage between ground and −30 V.

M111 INVERTER

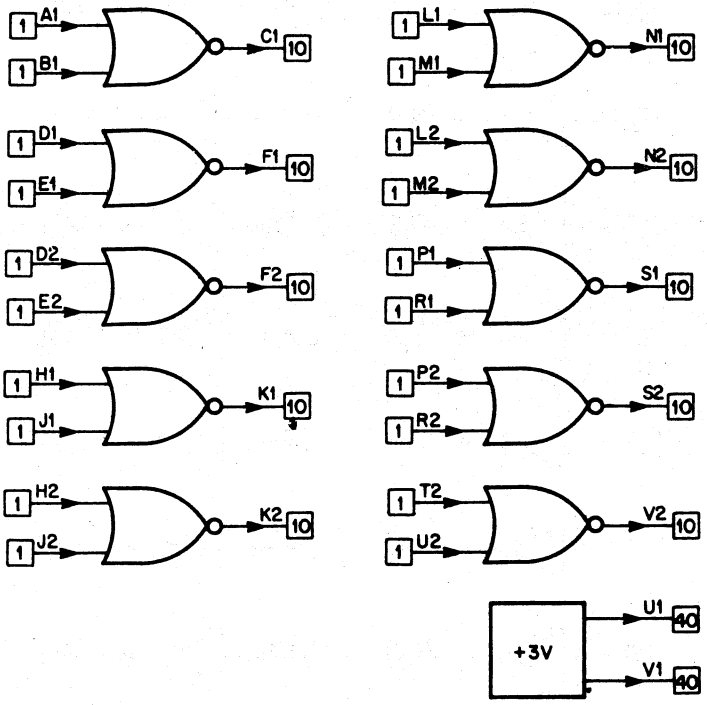


M111 Inverter Simplified Diagram

The M111 is a single-height module. It contains 16 inverters with input/output connections as shown in the simplified diagram.

Its applications include output expansion and logical inversion.

M112 NOR GATE



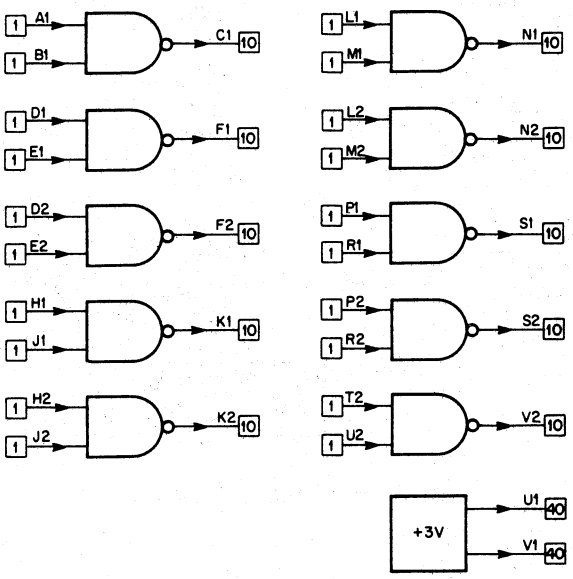
Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

M112 NOR Gate Simplified Diagram

The M112 is a single-height module. It contains 10 positive NOR gates, each performing the function A+B. Pins U1 and V1 provide two separate logic high sources (+3 V), each capable of holding up to 40 unused inputs high.

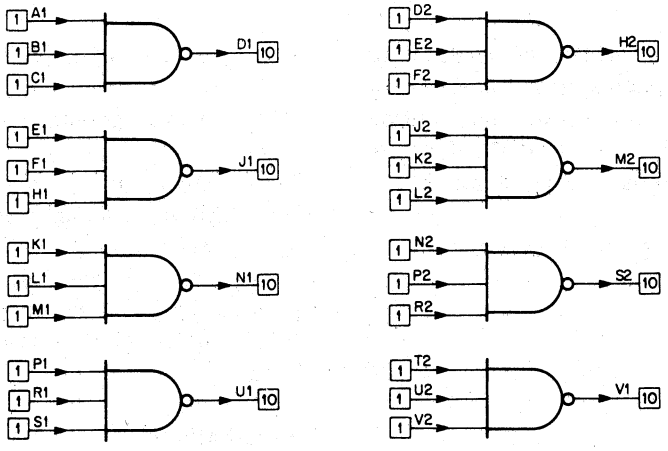
The M112 is used for logic gating applications.

M113, M115, M117, M119 NAND GATES

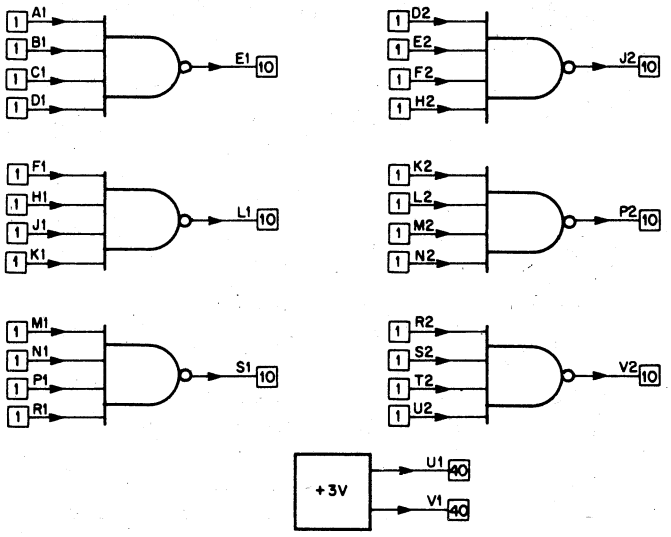


Volts	Power mA (max.)	Pins
+5	71 M113	A2
+5	41 M115	A2
+5	41 M117	A2
+5	19 M119	A2
GND		C2, T1

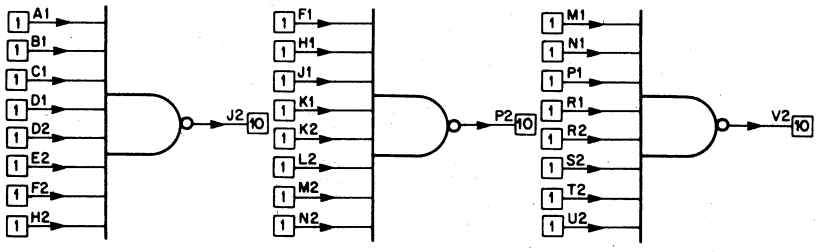
M113 Two-Input NAND Gates



M115 Three-Input NAND Gates



M117 Four-Input NAND Gates



M119 Eight-Input NAND Gates

The M113, M115, M117, and M119 are single-height modules. They provide general-purpose gating and are most commonly used for decoding, comparison, and control. Each module performs the NAND function ($\overline{\cdot B \cdot C \cdot \_\_\_ N}$), depending on the number of inputs.

These modules are used for logic gating applications.

Functions

M113 – Ten two-input NAND gates that also may be used as inverters.

M115 – Eight three-input NAND gates.

M117 – Six four-input NAND gates.

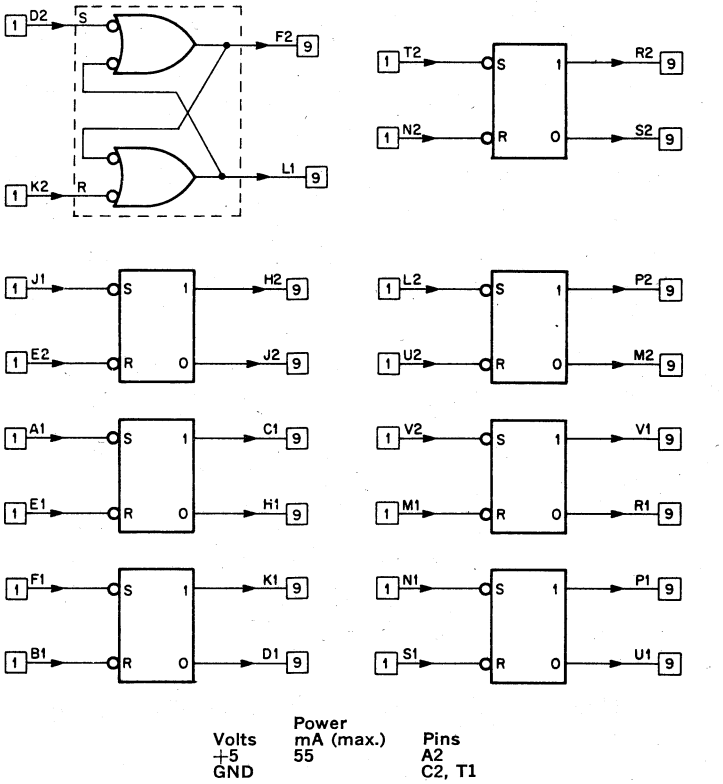
M119 – Three eight-input NAND gates.

Unused inputs on any gate must be returned to a source of logic high for maximum noise immunity. In the M113, M117, M119, M121, M617, and M627 modules, two pins are provided (U1 and V1) as the source of +3 V for this purpose. Each pin can supply up to 40 unit loads. M103, M111, and M002 provide additional sources of logic high level.

Specifications

Typical propagation delay is 15 ns.

M203 8 R/S FLIP-FLOPS



M203 8 R/S Flip-Flops Simplified Diagram

The M203 is a single-height module. It is made up of 8 R/S-type flip-flops. Each flip-flop is made up of two 2-input NAND gates with cross-coupled outputs.

R/S flip-flops provide an inexpensive method of storage.

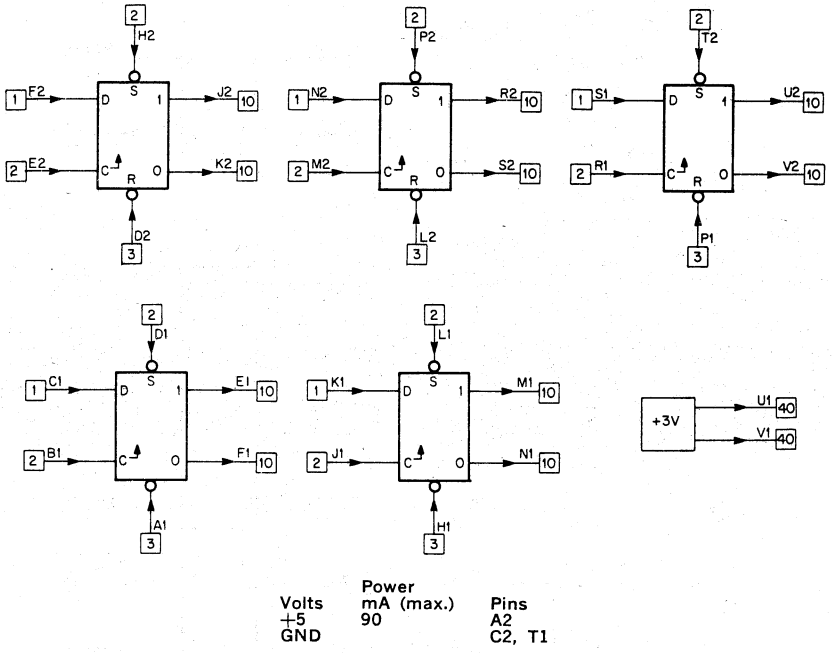
Precautions

Care must be taken not to place the SET and RESET inputs low at the same time. The last of the inputs to go high will determine the final state of the flip-flop.

Specifications

The propagation delay of the M203 is approximately 30 ns.

M205 GENERAL PURPOSE FLIP-FLOPS



M205 General Purpose Flip-Flops Simplified Diagram

The M205 is a single-height module. It contains five separate D-type flip-flops. Each flip-flop has independent gated data, clock, dc set, and dc reset inputs.

Applications

- Storage Registers
- Counters and Shift Registers
- Flags and Control Storage

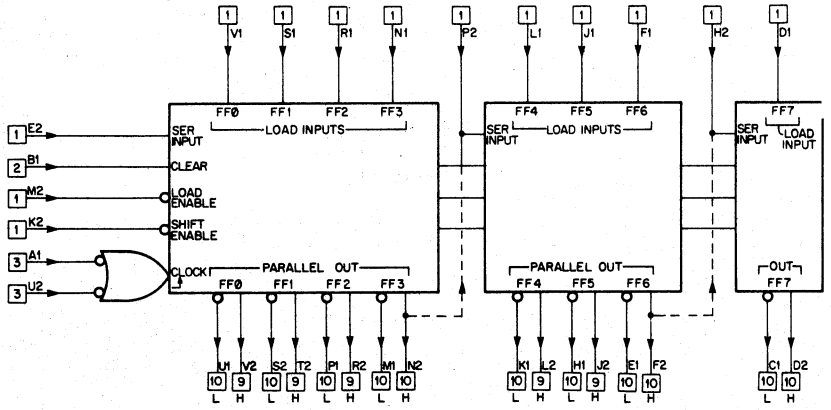
Functions

For each flip-flop, information present on the D input is transferred to the output when the threshold is reached on the leading (positive-going voltage) edge of the clock pulse.

Specifications

Information must be present on the D input 20 ns (max) prior to a standard clock pulse and should remain at the input at least 5 ns (max) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 ns, maximum. Typical width requirement for the clock, dc reset, and dc set pulses is 30 ns each.

M208 8-BIT BUFFER/SHIFT REGISTER



Volts	Power mA (max.)	Pins
+5	184	A2
GND		C2, T1

M208 Eight-Bit Buffer/Shift Register

The M208 is a single-height module. It is an internally connected 8-bit buffer/shift register. Provisions are made for gated single-ended parallel load, bipolar parallel output, and serial input. The shift register is divided into three segments:

- Bits 0 through 3: Serial input to bit 0, bipolar outputs from bits 0 through 3.
- Bits 4 through 6: Serial input to bit 4, bipolar outputs from bits 4 through 6.
- Bit 7: Serial input to 7, bipolar outputs from bit 7.

Functions

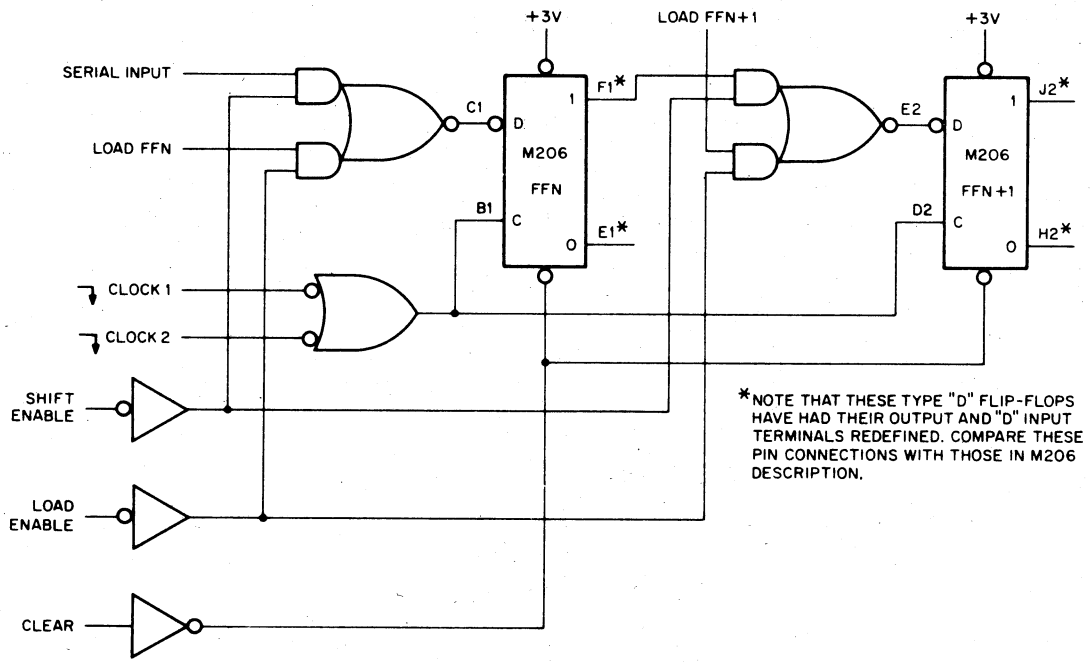
Each of the register groups shares a common shift line (the ORed CLOCK 1 and CLOCK 2 inputs) and a common parallel load line (LOAD ENABLE). To form a 6-bit shift register, for example, the true output of bit 3 is connected to the serial input of stage 4. A shift register of 8 bits may be constructed from a single module. Modules may be cascaded to form shift registers of any desired length. A few additional stages may be formed more economically from NAND and AND/OR gates plus a D-type flip-flop. A representative stage of this type is illustrated. Two CLOCK inputs are provided so that individual LOAD and SHIFT CLOCK sources may be used.

Precautions

Care must be taken that the clock inputs remain in the high state in the off condition because either input going to the low state will produce a positive edge at the output of the NAND gate and trigger the D-type flip-flop.

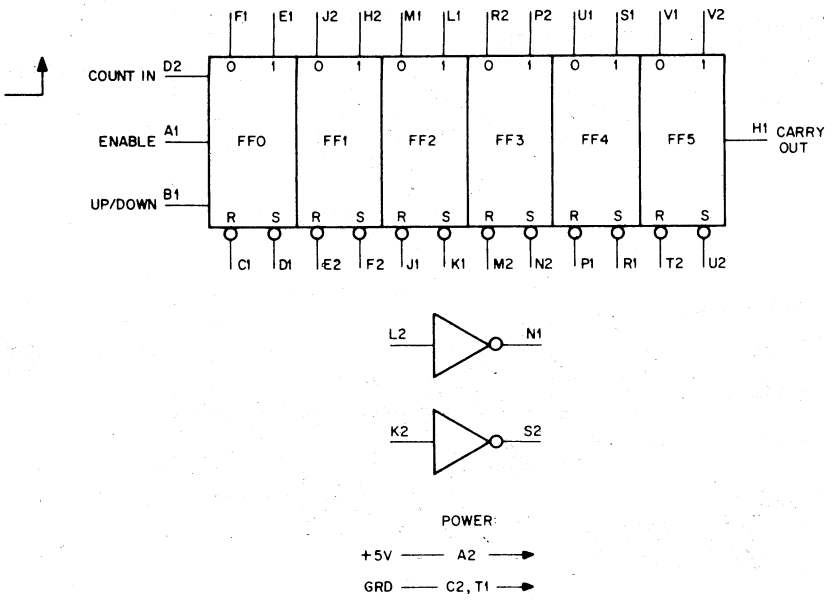
Specifications

Data shifted or parallel loaded into the M208 will appear on the outputs within 55 ns (max) of the CLOCK pulse leading edge threshold. LOAD and SHIFT ENABLE levels and parallel data must be present at least 50 ns prior to a CLOCK pulse. Propagation delay from the leading edge of a CLEAR pulse to the outputs is 40 ns max.



Two Representative Stages

M211 BINARY UP/DOWN COUNTER



M211 Binary Up/Down Counter Simplified Diagram

The M211 is a six-bit binary up/down counter. It can switch counting mode (up or down) without disturbing the contents of the counter. Maximum count rate is 10 MHz. Set/reset inputs are available for each bit. Maximum carry propagation time is 80 ns per bit.

Enable Line
The enable input must be negated 100 ns prior to an up/down level command. It must *not* be negated earlier than 500 ns after the leading edge (positive-going voltage) of the clock pulse. The enable input must be asserted at least 60 ns prior to the first count.

Up/Down Control Line
A logical 1 on this line will yield an up count. A logical 0 on this line will yield a down count.

Carry Out
The Carry Out will yield a positive level change whenever a carry or borrow occurs.

Inputs

Count In – Positive transition or pulse with less than 400 ns rise-time. Count In presents two unit loads.

Reset – Each reset input presents three unit loads.

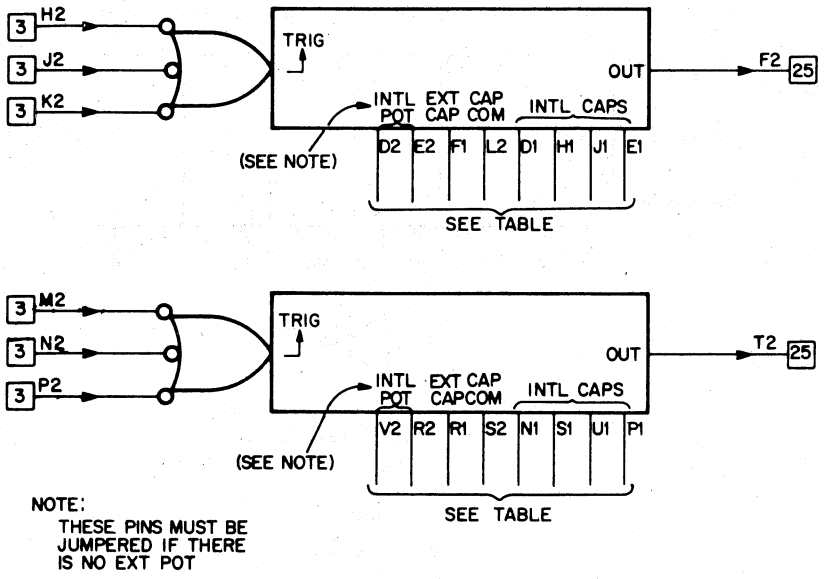
Set – Each set input presents two unit loads.

All other inputs present one unit load.

Outputs
Each flip-flop output (1 or 0) can drive eight unit loads. Carry Out can drive ten unit loads. Each inverter output can drive 30 unit loads.

Power
+5.0 V, 217 mA (max).

M302 DUAL DELAY MULTIVIBRATOR



Volts	Power mA (max.)	Pins
+5	166	A2
GND		C2, T1

M302 Dual-Delay Multivibrator Simplified Diagram

The M302 is a single-height module. It contains two delays (one-shot multivibrators) which are triggered by a level change from high to low or a pulse to low whose duration is equal to or greater than 50 ns. When the input is triggered, the output changes from low to high for a predetermined length of time and then returns to low.

The delay time is adjustable from 50 ns to 7.5 ms using the internal capacitors and can be extended by adding an external capacitor.

Applications

- Time Delays
- Variable Width Pulses

Functions

Delay Range: The basic delay range is determined by an internal capacitor. The delay range may be increased by selection of additional capacitance which is available by connecting various module pins or by the addition of external capacitance. An internal potentiometer can be connected for fine delay adjustments within each range or an external resistance may be used. If an external resistance is used, the combined resistance of the internal potentiometer and the external resistance should be limited to 10,000 ohms.

Delay Range	Capacitor Value	Interconnections Required Delay 1	Delay 2
50 ns – 750 ns	100 pF (internal)	None	None
500 ns – 7.5 μs	1000 pF (internal)	D1 – L2	N1 – S2
5 μs – 75 μs	0.01 μF (internal)	H1 – L2	S1 – S2
50 μs – 750 μs	0.10 μF (internal)	J1 – L2	U1 – S2
500 μs – 7.5 ms	1.00 μF (internal)	E1 – L2	P1 – S2
Above 7.5 ms	Add external capacitors between specified pins	F1 – L2	R1 – S2

Adjustable Delays: Connect pins D2 to E2 for delay 1 and V2 to R2 for delay 2 in order to add the internal potentiometers.

NOTE

If there is no external potentiometer, these pins must be jumpered.

Without a potentiometer, the delay will not recover. An external potentiometer of less than 10K ohms can be used by connecting it between E2 or R2 and ground pin C2. Use of an external adjustment resistor will cause some increase in jitter. It is recommended that leads to an external potentiometer be twisted pairs and as short as possible.

Precautions

Care should be exercised in the selection of external capacitors to assure low leakage as leakage will affect the time delay.

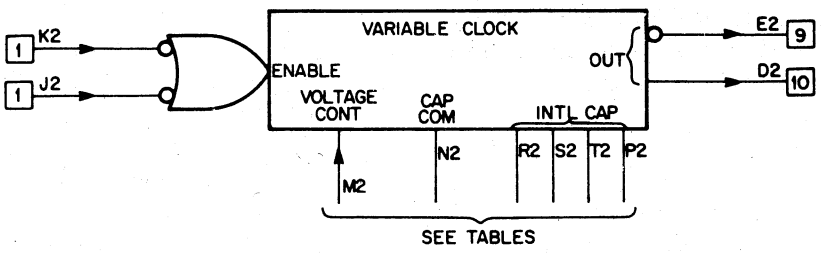
Specifications

Trigger Input Fall Time: Must be less than 400 ns.

Recovery Time: Defined as the time all inputs must remain high before any input goes low to trigger the delay

1. Without external capacitance: 30 ns min.
2. With external capacitance: 300 C ns min., where C is in nanofarads.

M401 VARIABLE CLOCK



Volts	Power mA (max.)	Pins
+5	80*	A2
GND		C2, T1

* using printed circuit board revision E or later

M401 Variable Clock Simplified Diagram

The M401 is a single-height module. It is a stable RC-coupled multivibrator which produces standard timing pulses at adjustable repetition rates.

The repetition rate is adjustable from 175 Hz to 10 MHz in five ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control. An internal potentiometer provides continuously variable adjustment within each range.

A 0 to 10 V control voltage will vary the frequency over about 30% of each frequency range.

This module is intended for use as the primary source of timing signals in a digital system.

Functions

Start Control: A two-input OR gating input is provided for start-stop control of the pulse train. A level change from high to low with fall time less than 400 ns is required to enable the clock.

Frequency Range:

Frequency Range		Interconnections Required
1.5 MHz to 10 MHz	(100 pF)	None
175 kHz to 1.75 MHz	(1000 pF)	N2 – R2
17.5 kHz to 175 kHz	(.01 μFd)	N2 – S2
1.75 kHz to 17.5 kHz	(0.1 μFd)	N2 – T2
175 Hz to 1.75 kHz	(1.0 μFd)	N2 – P2

Fine Frequency Adjustment: Controlled by an internal potentiometer. No provision is made for any external connections. An external capacitor may be added by connection between pins N2 and C2.

Voltage Control of Frequency: The M401 may also be voltage controlled by applying a control voltage to pin M. This feature is available only in M401 modules using printed circuit board revision E or later. The voltage applied to pin M should be limited to the range of 0 V to +10.0 V. This voltage swing will allow

the frequency to be shifted by approximately 30 percent in the frequency range using the internal capacitors of 1.0, 0.1, 0.01 and 0.001 μF. If the voltage applied to pin M is dc or low frequency (below 1 kHz), pin M will appear approximately as a +1.0 V source with a Thevenin resistance of 800 ohms. Modulating the M401 with a 10 V P-P signal about a center frequency, as derived by the application of a mean voltage of +5 V to pin M, will yield a typical frequency excursion in excess of plus or minus 15% about the center frequency. Typical frequency excursions which may be obtained are shown in the following table.

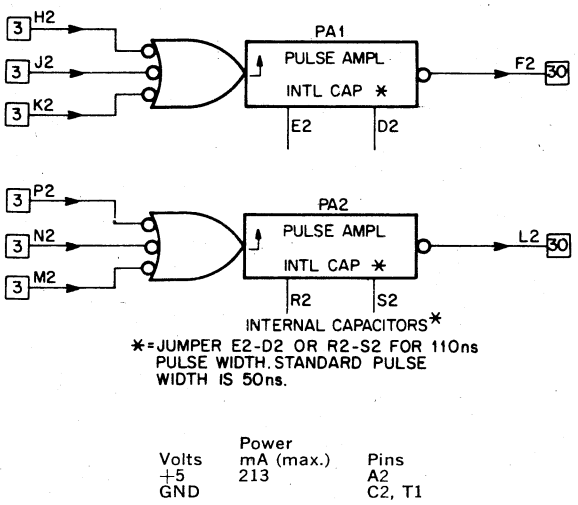
Specifications

Maximum delay from enabling inputs to output E2 is 50 ns. The output pulse width is 50 ns.

Output Frequency in kHz

Voltage Applied to Pin M	Capacitor			
	1.0 μFd	0.1 μFd	0.01 μFd	0.001 μFd
0	1.000	10.00	100.0	1000
+1	1.054	10.49	104.6	1036
+2	1.101	10.94	109.2	1071
+3	1.147	11.39	113.6	1108
+4	1.193	11.83	118.0	1142
+5	1.238	12.26	122.2	1181
+6	1.282	12.69	126.4	1271
+7	1.325	13.10	130.4	1295
+8	1.368	13.50	134.2	1312
+9	1.408	13.87	137.7	1322
+10	1.443	14.20	140.9	1323

M602 PULSE AMPLIFIER



M602 Pulse Amplifier Simplified Diagram

The M602 is a single-height module. It contains two pulse amplifiers which provide power amplification, standardize pulses in amplitude and width, and transform level changes into a standard pulse.

Functions

A negative pulse output is produced when the input is triggered by a transition from high to low. An internal capacitor is brought out to pin connections to permit the standard 50 ns output pulse to be increased to 110 ns (nominal).

Specifications

Propagation Time: 30 ns max. between input and output thresholds.

Recovery Time: Equal to that of the output pulse width. The input must have a fall time (10% to 90% points) of less than 400 ns and must remain below 0.8 V for at least 30 ns. Maximum PRF is 10 MHz.

APPENDIX B
ENGINEERING DRAWINGS

NOTE

The RC8-E option's engineering drawings, although contained in this drawing set, are not discussed in this manual because there are no RS64-TAs currently in service with the RC8-E option installed.

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

THIS IS PRINT SET

	SEQUENCE
DRAWING DIRECTORY	B-DD-RS64-TA
RS64 TTW TIMING DIAG	B-TD-RS64-TA-06
RS64 TTW CLK & CNTL	D-BS-RS64-TA-03
RS64 TTW SR-WC & WRT FLOPS	D-BS-RS64-TA-04
WRITERS READ AMPS & GAP DET	D-BS-RS64-TA-05
MODULE UTILAZATION	D-MU-RS64-TA-02
MODULE UTILIZATION(PL)	A-PL-RS64-TA-02
UNIT ASSY	D-UA-RS64-TA-0
WIRED ASSY	D-AD-7008324-0-0
WIRED ASSY (PL)	A-PL-7008324-0-0
CONTROL PANEL ASSY	D-AD-9305476-0-0
CONTROL PANEL CABLE	D-IA-7008589-0-0
DISK PLUG CABLE	D-IA-7008590-0-0
POWER CABLE	D-IA-7008588-0-0
TEST CABLE	C-IA-7008668-0-0
RS64-TA OPERATING PROC.	A-SP-RS64-TA-7
RS64-TTW FOR RC8/E	D-BS-RS64-TA-09
RS64 TTW TIMING DIAGRAM RC8/E	D-BS-RS64-TA-08

UNIT VARIATIONS

VARIATION	TITLE	PRINT SET TYPE: RS64-TA
RS64-TA	RS64-TA TIMING TRACK WRITER TESTER	X

REVISIONS	REV	CHG. NO.	DATE
	—	ORIGNATED - 00001	—
A		RS64TA-00002	10-72
B		RS64TA-00003	1-73
C		RS64TA-00004	6-73

USED ON OPTION/MODEL: RS64-TA-[illegible]

DRN.	[signature]	DATE 3/2/72
CH'K'D	[signature]	DATE 3/2/72
PROJ ENG.	[signature]	DATE 3/7/72
PROD.	[signature]	DATE 3/2/72
FIELD SERV.	[signature]	DATE 3/4/72

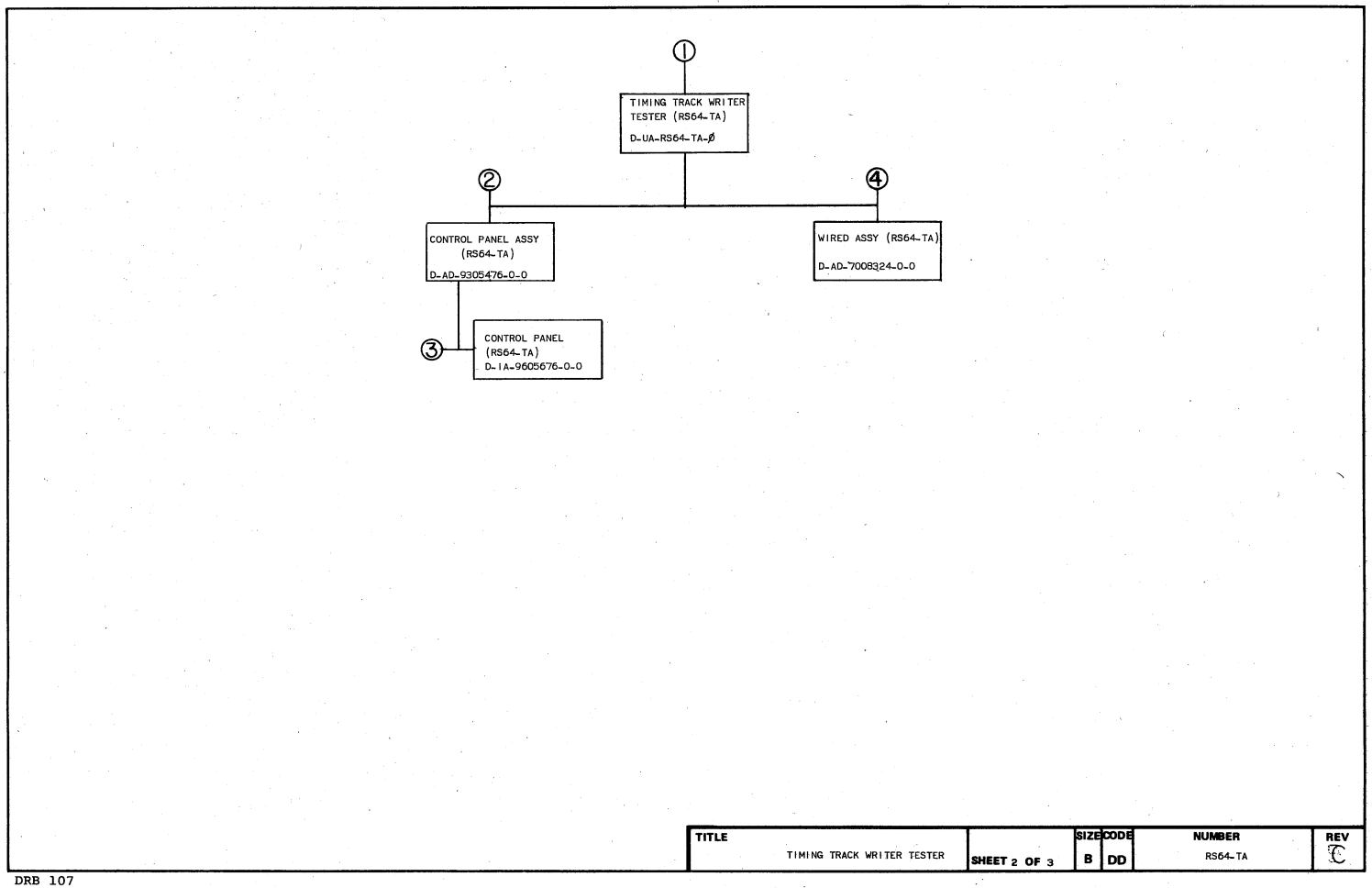
TITLE: TESTER TIMING TRACK WRITER (RS64-TA)

SIZE	CODE	NUMBER	REV
B	DD	RS64-TA	C

SHEET 1 OF 3 DIST

DRB 106

DEC 16—(325)—1062—1—N871



TITLE		SIZE	CODE	NUMBER	REV
TIMING TRACK WRITER TESTER	SHEET 2 OF 3	B	DD	RS64-TA	C

DRB 107
DEC 16—(325)—1062—3—N871

ELECTRICAL

CUSTOMER PRINT SET RS64-TA	MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
X		1	B-DD-RS64-TA	X	3	DRAWING DIRECTORY	
X			D-MU-RS64-TA-02	B	1	MODULE UTILIZATION	
X			A-PL-RS64-TA-02	B	1	MODULE UTILIZATION (PL)	
X			D-BS-RS64-TA-03	C	1	RS64 TTW CLK & CNTL	
X			D-BS-RS64-TA-04	B'	1	RS64 TTW SR-WC & WRT FLOPS	
X			D-BS-RS64-TA-05	B'	1	WRITERS READ AMPS & GAP DET	
X			D-TD-RS64-TA-06	B'	1	RS64 TTW TIMING DIAGRAM	
X			D-UA-RS64-TA-0	B	1	TIMING TRACK WRITER TESTER	
X			A-SP-RS64-TA-7	B	5	RS64-TA OPERATING PROCEDURE	
X			D-BS-RS64-TA-09	*	1	RC8/E LOGIC	
X			D-TD-RS64-TA-08	*	1	TIMING DIAGRAM RC8/E	
			K-WL-RS64-TA-10	A	1	WIRE LIST	
X		4	D-AD-7008324-0-0	B	2	WIRED ASSY	
X			A-PL-7008324-0-0	B	1	WIRED ASSY (PL)	

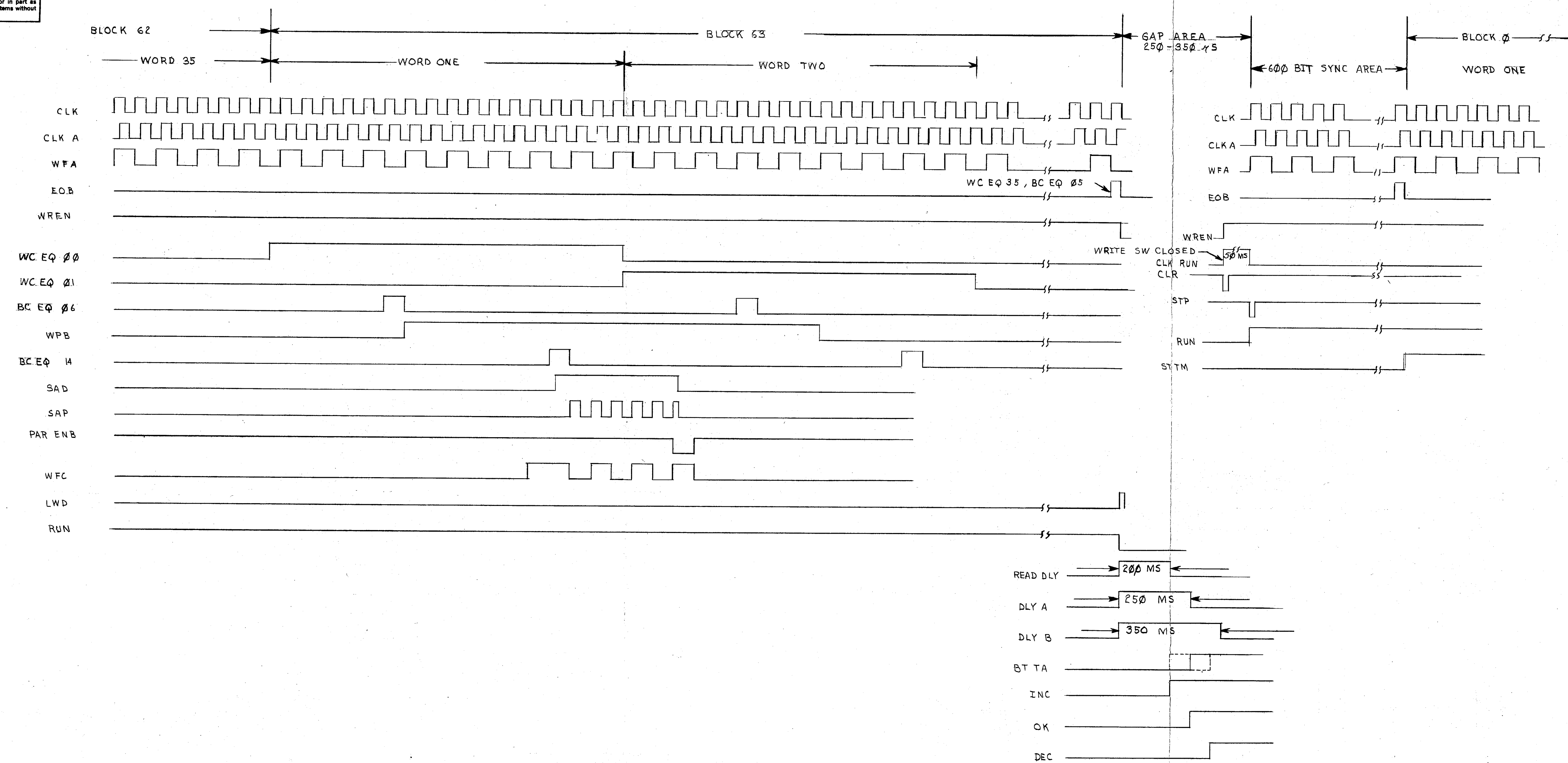
MECHANICAL

CUSTOMER PRINT SET RS64-TA	MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
		1	D-UA-RS64-TA-0	B	1	TIMING TRACK WRITER TESTER	
			E-IA-9605709-0-0		1	TESTER CHASSIS	
			D-IA-9605714-0-0		1	BACK PANEL	
			D-IA-9605713-0-0		1	DIVIDER BRKT.	
			C-IA-9605712-0-0		1	BRKT, CHASSIS	
			D-MD-9605710-0-0		1	HINGE CONTROL PANEL	
			E-IA-9605711-0-0		1	COVER, CHASSIS	
X			D-IA-7008588-0-0	#	1	POWER CABLE	
X			C-IA-7008668-0-0	#	1	TEST CABLE	
			C-IA-9605796-0-0		1	MODULE HOLDDOWN BRKT	
			C-IA-7405642-0-0		1	MODULE RETAINER SCREW	
X		2	D-AD-9305476-0-0	#	1	CONTROL PANEL ASSY	
X			D-IA-7008589-0-0	#	1	CONTROL PANEL CABLE	
X			D-IA-7008590-0-0	#	1	DISK PLUG CABLE	
			B-MA-4908-0-1		1	4908 IND LIGHT ASSY	
			B-MD-9605726-0-0		1	HOLD DOWN BRKT. 36 PIN CONN.	
		3	D-IA-9605676-0-0		1	CONTROL PANEL	
			C-SS-9605676-0-1		1	SILK SCREEN	
		4	D-AD-7008324-0-0		2	WIRED ASSY	
			A-PL-7008324-0-0		1	WIRED ASSY (PL)	
			D-MD-9605733-0-0		1	CASTING FRAME REWORK	
			D-SC-1205348-0-0		1	288 PIN BLOCK	
			[illegible]		1	[illegible]	

TITLE	SHEET	SIZE	CODE	NUMBER	REV
TIMING TRACK WRITER TESTER	3 OF 3	B	DD	RS64-TA	C

DRB 108

DEC 16—(325)—1062—2—N871



REVISIONS	CHANGE NO.	REV.	CHK
	RS64TA-00001	A	
	P. GADAIRE		

FIRST USED ON OPTION/MODEL: PDP-11

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL: —

FINISH: —

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

		DATE
DRN.	A. Campbell	2-22-71
CHK'D		4-6-71
ENG.		9-29-71
PROJ. ENG.		9-29-71
PROD.		2/3/72

NEXT HIGHER ASSY.: B-DD-RS64-TA

SCALE: —

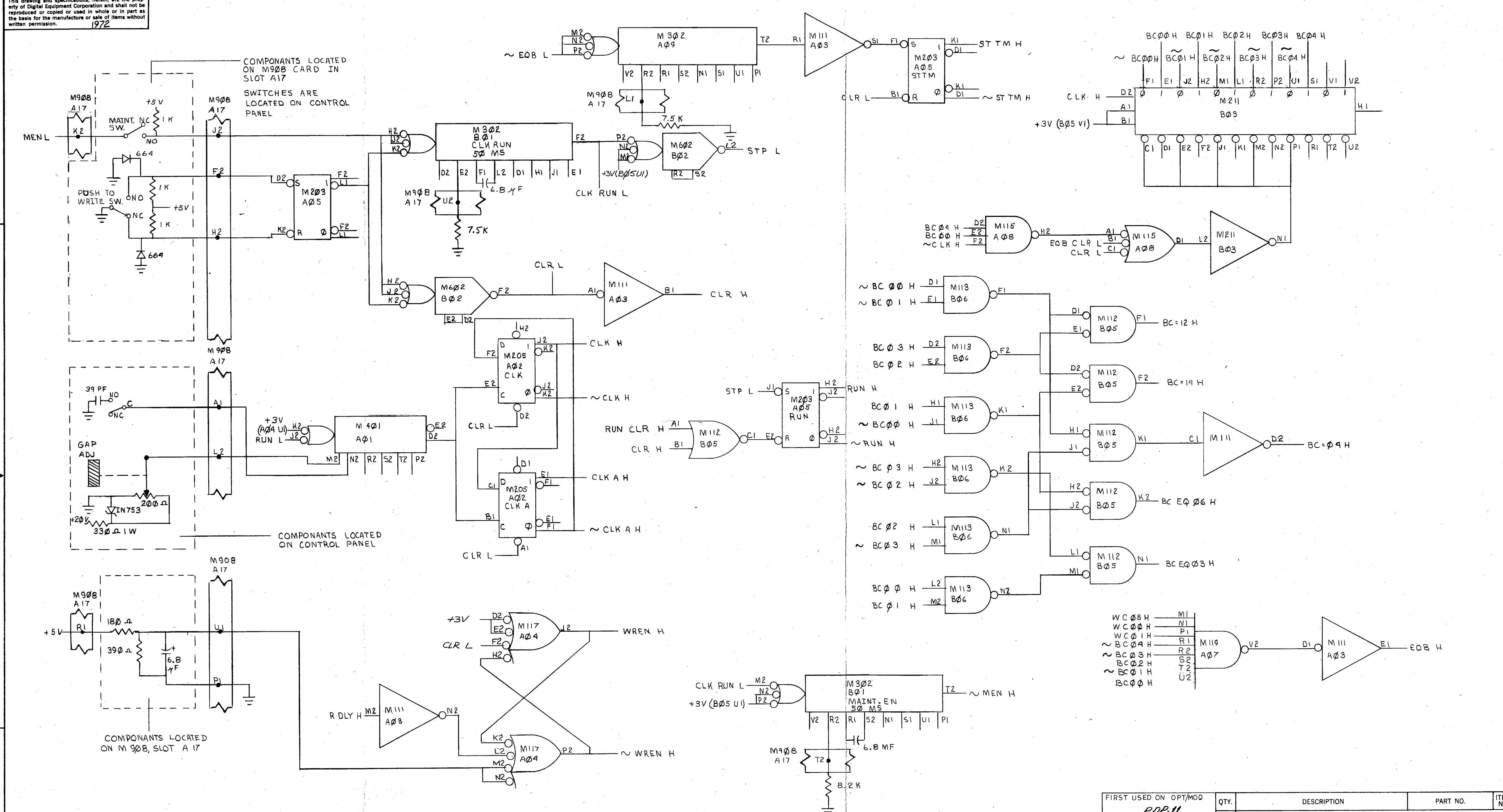
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: RS64 TTW TIMING DIAGRAM

SIZE	CODE	NUMBER	REV.
D	TD	RS64-TA-Ø6	A

DEC FORM NO DRD 102-B



FIRST USED ON OPT/MOD: PDP-11

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —
FINISH —

DRN. DATE 2-6-71
CHK'D. DATE 9-6-71
ENG. DATE 3-24-71
PROJ. ENG. DATE 3-29-71
PROD. DATE 3/31/72

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE RS64 TTW CLK & CNTL

NEXT HIGHER ASSY B-DD-RS64-T A

SIZE D CODE BS NUMBER RS64-TA-Ø3 REV. C

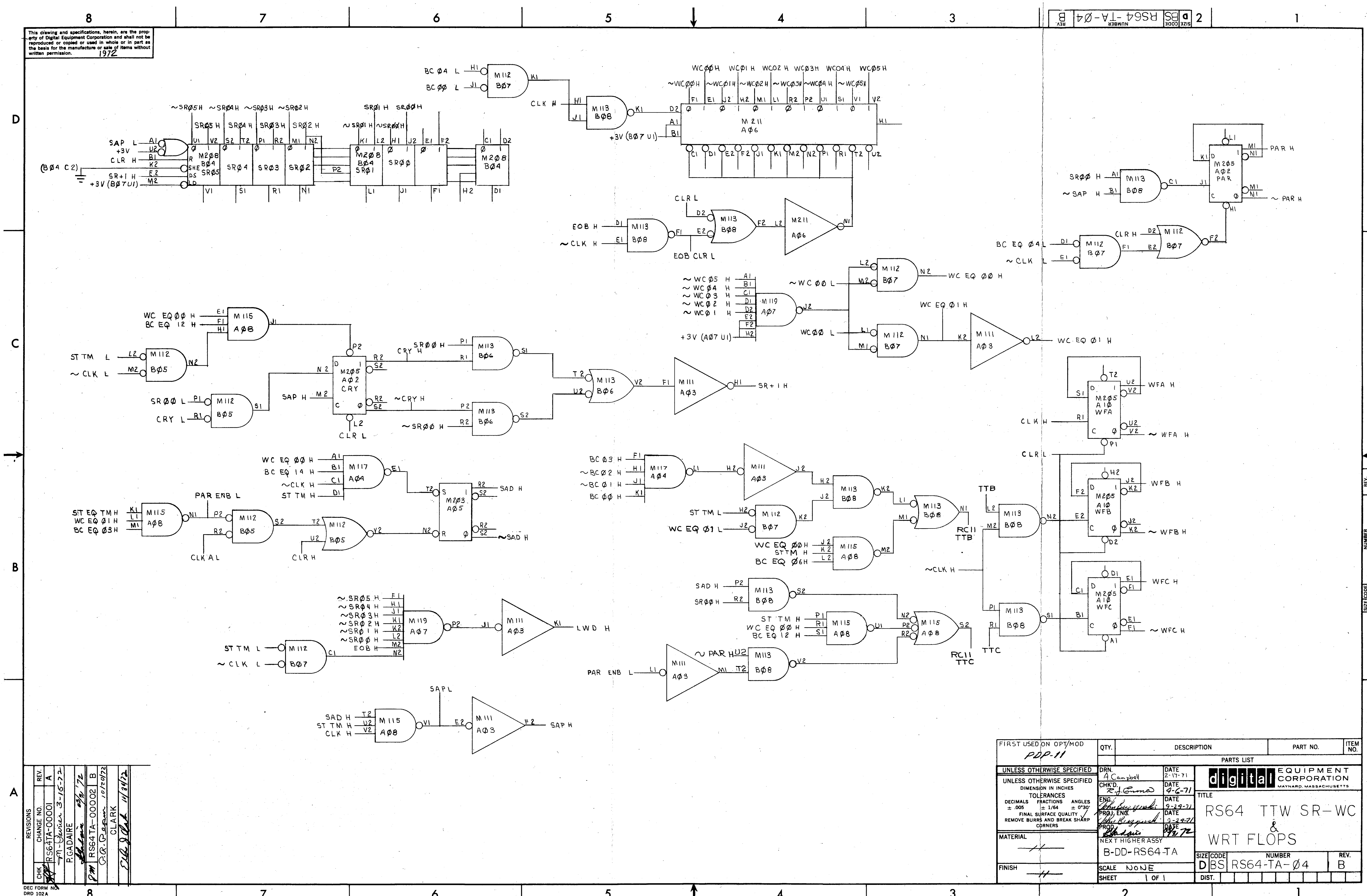
SCALE NONE SHEET 1 OF 1

DIST.

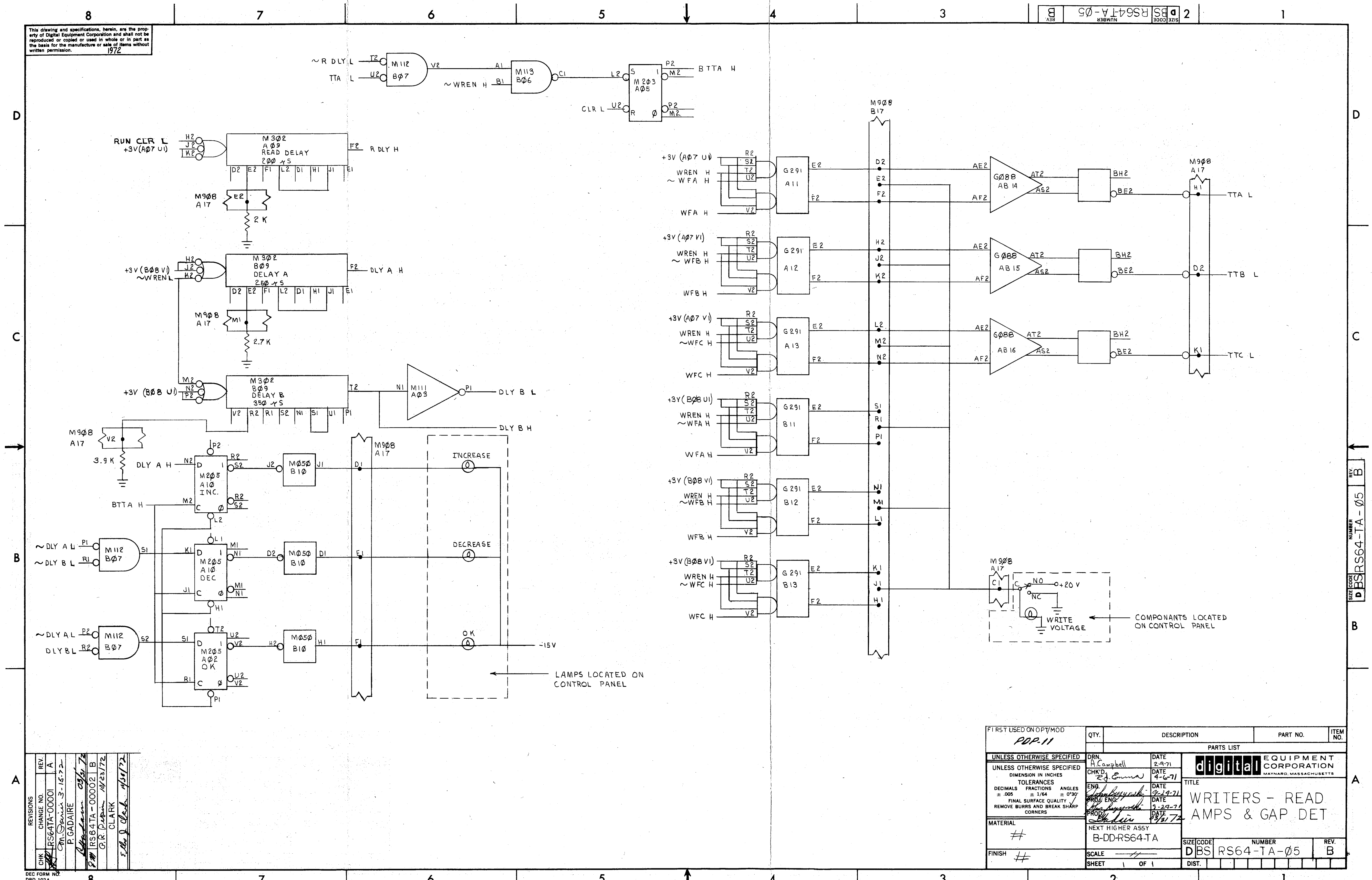
REVISIONS

CHK	CHANGE NO.	REV.
	RS64TA-00001 P. GADAIRE 3-15-72	A
	RS64TA-00002 G.R. Pope 10/23/72	B
	RS64TA-00004 CLARK 11/30/72 J. BUZYNSKI 7-6-73	C

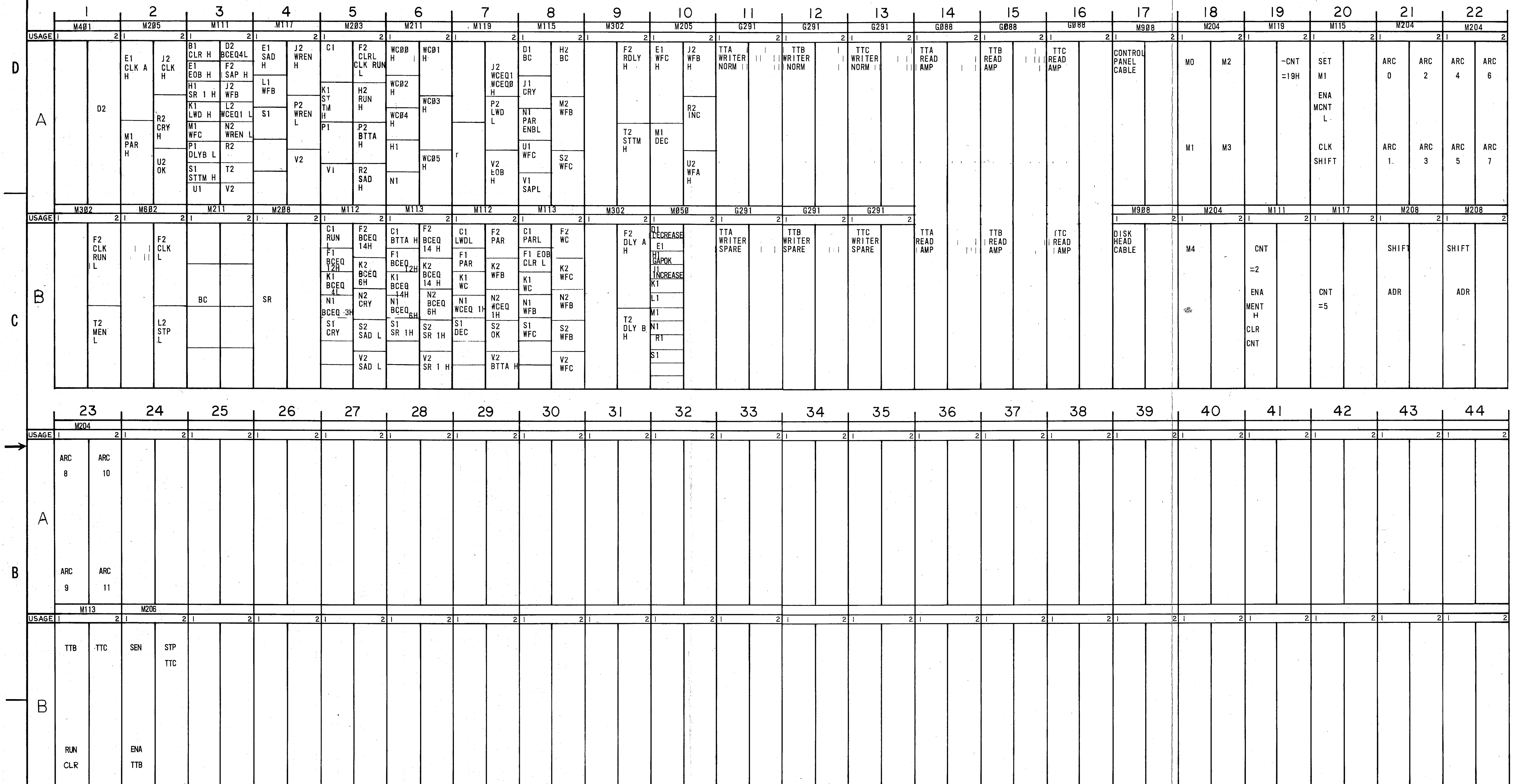
DEC FORM NO DRD 102A



This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission. 1972
BC Ø4 L
BC ØØ L
M112 BØ7
CLK H
M113 BØ8
WCØØH WCØ1H WCO2H WCØ3H WCO4H WCØ5H
M211 AØ6
+3V (BØ7 U1)
~SRØ5H ~SRØ4H ~SRØ3H ~SRØ2H
SRØ1H SRØØH
SAP L
+3V
CLR H
(BØ4 C2)
SR+1 H
+3V (BØ7U1)
M2Ø8 BØ4 SRØ5
SRØ4
SRØ3
SRØ2
M2Ø8 BØ4 SRØ1
SRØØ
M2Ø8 BØ4
CLR L
EOB H
~CLK H
EOB CLR L
M211 AØ6
SRØØ H
~SAP H
M113 BØ8
M2Ø5 AØ2 PAR
PAR H
~ PAR H
BC EQ Ø4 L
~CLK L
CLR H
M112 BØ7
~WCØ5 H
~WCØ4 H
~WCØ3 H
~WCØ2 H
~WCØ1 H
+3V (AØ7 U1)
M119 AØ7
~WCØØ L
M112 BØ7
WC EQ ØØ H
WC EQ Ø1 H
WCØØ L
M111 AØ3
WC EQ Ø1 H
WC EQ ØØ H
BC EQ 12 H
M115 AØ8
ST TM L
~CLK L
M112 BØ5
SRØØ L
CRY L
M112 BØ5
SAP H
M2Ø5 AØ2 CRY
CLR L
CRY H
SRØØ H
~CRY H
~SRØØ H
M113 BØ6
M113 BØ6
M111 AØ3
SR+1 H
WFA H
~WFA H
M2Ø5 A1Ø WFA
CLK H
CLR L
WC EQ ØØ H
BC EQ 14 H
~CLK H
ST TM H
M117 AØ4
PAR ENB L
ST EQ TM H
WC EQ Ø1 H
BC EQ Ø3H
M115 AØ8
M112 BØ5
M112 BØ5
CLK AL
CLR H
M2Ø3 AØ5
SAD H
~SAD H
BC Ø3 H
~BCØ2 H
~BCØ1 H
BC ØØ H
M117 AØ4
M111 AØ3
M113 BØ8
ST TM L
WC EQ Ø1 L
M112 BØ7
WC EQ ØØ H
ST TM H
BC EQ Ø6H
M115 AØ8
M113 BØ8
RC11 TTB
TTB
M113 BØ8
WFB H
~WFB H
M2Ø5 A1Ø WFB
~CLK H
SAD H
SRØØ H
M113 BØ8
ST TM H
WC EQ ØØ H
BC EQ 12 H
M115 AØ8
M115 AØ8
RC11 TTC
TTC
M113 BØ8
WFC H
~WFC H
M2Ø5 A1Ø WFC
~SRØ5 H
~SRØ4 H
~SRØ3 H
~SRØ2 H
~SRØ1 H
~SRØØ H
EOB H
M119 AØ7
M111 AØ3
LWD H
ST TM L
~CLK L
M112 BØ7
~PAR H
PAR ENB L
M111 AØ3
M113 BØ8
SAP L
SAD H
ST TM H
CLK H
M115 AØ8
M111 AØ3
SAP H
REVISIONS
CHK | CHANGE NO. | REV.
RS64TA-00001 | A
M. Sevier 3-15-72
P. GADAIRE
RS64TA-00002 | B
G.R. Regan 10/20/72
CLARK
FIRST USED ON OPT/MOD
PDP-11
UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
QTY. | DESCRIPTION | PART NO. | ITEM NO.
PARTS LIST
DRN. A Campbell DATE 2-17-71
CHK'D DATE 9-6-71
ENG. DATE 9-29-71
PROJ. ENG. DATE
PROD. DATE
NEXT HIGHER ASSY
B-DD-RS64-TA
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE
RS64 TTW SR-WC & WRT FLOPS
SIZE D CODE BS NUMBER RS64-TA-Ø4 REV. B
SCALE NONE
SHEET 1 OF 1
DIST.
DEC FORM NO. DRD 102A


This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission. 1972
~R DLY L
TTA L
M112 BØ7
~WREN H
M113 BØ6
CLR L
M2Ø3 AØ5
B TTA H
RUN CLR L
+3V (AØ7 U1)
M3Ø2 AØ9 READ DELAY 200 ns
R DLY H
M9Ø8 A17
2 K
+3V (BØ8 V1)
~WREN L
M3Ø2 BØ9 DELAY A 250 ns
DLY A H
2.7 K
+3V (BØ8 U1)
M3Ø2 BØ9 DELAY B 350 ns
M111 AØ3
DLY B L
DLY B H
3.9 K
DLY A H
M2Ø5 A1Ø INC.
BTTA H
M2Ø5 A1Ø DEC
M2Ø5 AØ2 OK
~DLY A L
~DLY B L
M112 BØ7
MØ5Ø B1Ø
INCREASE
DECREASE
OK
-15V
LAMPS LOCATED ON CONTROL PANEL
M9Ø8 B17
+3V (AØ7 U1)
WREN H
~WFA H
WFA H
G291 A11
+3V (AØ7 V1)
~WFB H
WFB H
G291 A12
~WFC H
WFC H
G291 A13
+3V (BØ8 U1)
G291 B11
+3V (BØ8 V1)
G291 B12
G291 B13
GØ88 AB14
GØ88 AB15
GØ88 AB16
TTA L
TTB L
TTC L
NO
+20 V
NC
WRITE VOLTAGE
COMPONANTS LOCATED ON CONTROL PANEL
FIRST USED ON OPT/MOD PDP-11
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN. A. Campbell DATE 2-9-71
CHK'D DATE 4-6-71
ENG. DATE
PROD. ENG. DATE
PROJ. DATE
NEXT HIGHER ASSY B-DD-RS64-TA
SCALE
SHEET 1 OF 1
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE
WRITERS - READ AMPS & GAP DET
SIZE D CODE BS NUMBER RS64-TA-Ø5 REV. B
DIST.
REVISIONS
REV. A CHANGE NO. RS64TA-00001 P. GADAIRE
B RS64TA-00002 G.R. Pepin 11/23/72 CLARK
DEC FORM NO. DRD 102A

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission. 1972



FIRST USED ON OPTION/MODEL	RS64-TA
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL	—
FINISH	—
NEXT HIGHER ASSY	B-DD-RS64-TA
SCALE	—
SHEET	1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: MODULE UTILIZATION

SIZE D CODE MU NUMBER RS64-TA-Ø2 REV. B

REVISIONS

REV.	CHANGE NO.	CHK
A	RS64TA-00001 3-15-72 P. GADAIRE	
B	RS64TA-00002 10/25/72 CLARK	

DEC FORM NO. DRD 112

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY JOHN BUZYNSKI	CHECKED		SECTION
DATE 2/3/71	DATE 6-28-71		
ENG JOHN BUZYNSKI	PROD		ISSUED SECT.
DATE 2/3/71	DATE		

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION
	MØ5Ø	50 MA INDICATOR DRIVER	1
	M111	INVERTER	2
	M112	NOR GATE 2 INPUT	2
	M113	NAND GATE 2 INPUT	4
	M115	NAND GATE 3 INPUT	1
	M117	NAND GATE 4 INPUT	2
	M119	NAND GATE 8 INPUT	2
	M2Ø3	R/S FLIP FLOP	1
	M2Ø5	D TYPE FLIP FLOP	2
	M2Ø8	8-BIT BUFFER/SHIFT REGISTER	2
	M211	BINARY UP/DOWN COUNTER	2
	M3Ø2	DUAL DELAY MULTIVIBRATOR	3
	M4Ø1	VARIABLE CLOCK	1
	M6Ø2	PULSE AMPLIFIER	1
	M9Ø8	RIBBON CONNECTOR	2
	GØ88	DISK PRE AMP & PEAK DETECTOR	3
	G291	DISK WRITER W/POWER FAIL	6
	M204	GENERAL PRUPOSE BUFFER AND COUNTER	
	M206	GENERAL PURPOSE FLIP FLOP	1

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
MODULE UTILIZATION (RS64-TA)	D-MU-RS64-TA-Ø2	A	PL	RS64-TA-Ø2	B	RS64-TA 00002
	SHEET 1 OF 1	DIST.				

DEC FORM DEC 16–(325)–1031–N870
DRA 110

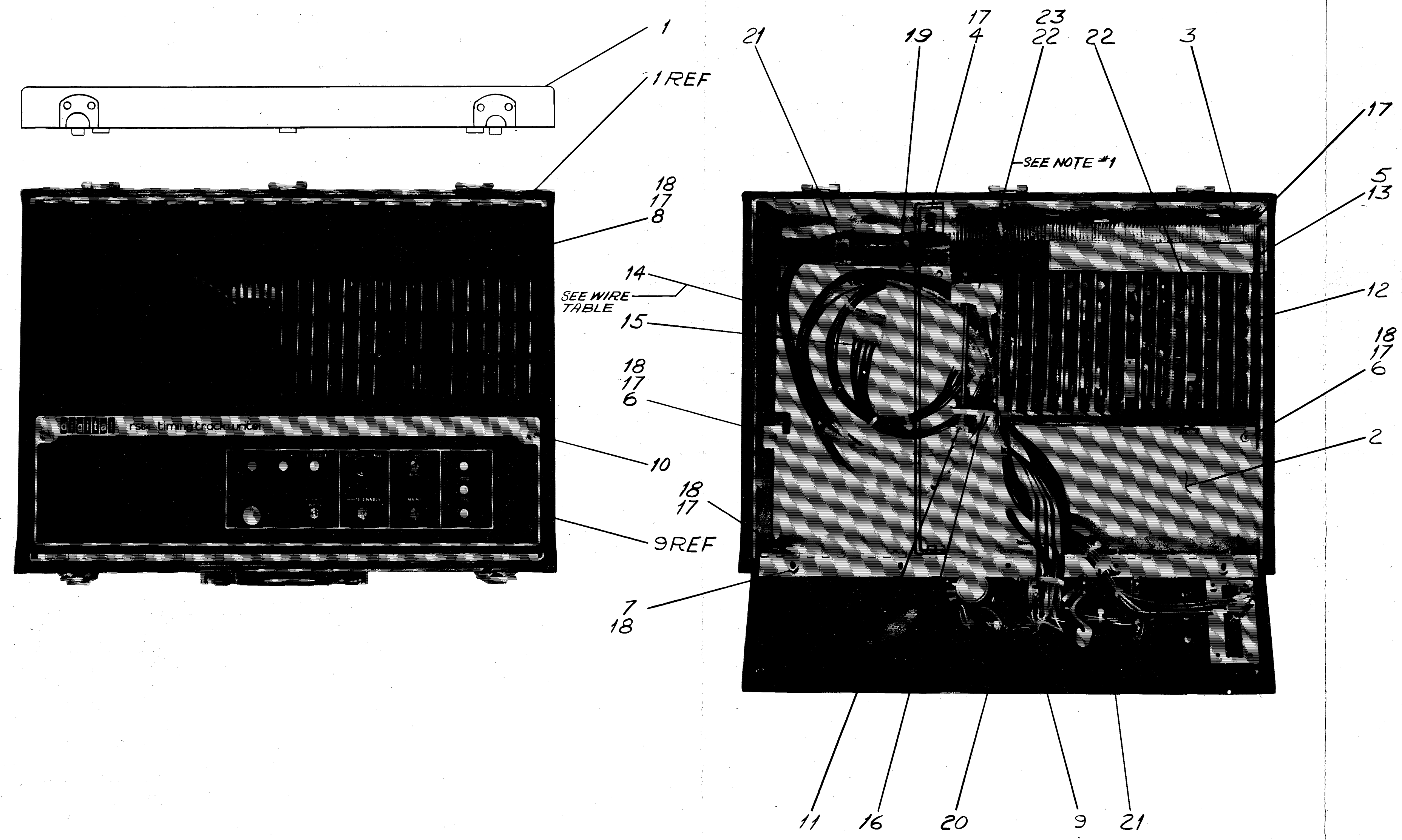
D | UA | RS64-TA-0 | REV. B

WIRE TABLE

ITEM NO.	DESCRIPTION: COLOR	DESCRIPTION: AWG	CONNECTIONS: FROM	CONNECTIONS: WITH	CONNECTIONS: TO	CONNECTIONS: WITH	REMARKS
14	RED	14	P3-1	A24A2	—	—	P1-P4 LOCATED ON CABLE DWG.
↕	BLK		P3-6	A24C2	—	—	
↕	YEL		P3-8	B15D2	—	—	
14	BLU	14	P3-12	B16B2	—	—	

NOTES:

1. REMOVE EXISTING SCREW FROM LOGIC AND REPLACE WITH ITEM #23 TO MOUNT ITEM #22
2. FOR DRAWING DIRECTORY REFER TO DWG. B-DD-RS64-TA



QTY.	DESCRIPTION	PART NO.	ITEM NO.
2	PHL. FILL. HD. SCR. #8-32X1½LG.	9007799-6	23
2	CABLE RETAINING BLOCK (NYLON)	1209850	22
3	CLAMP, CABLE ⅜ DIA.	9007083	21
1	TIE WRAP, SCREW DOWN	9007033	20
2	SCRW. PHL. PAN HD. #8-32X½LG.	9006039-1	19
17	KEPS NUT #8-32	9006563	18
20	SCW. PHL. FLAT HD. #8-32X⅜LG.	9006037-2	17
1	MODULE HOLDOWN BRKT.	C-IA-9605796-1-0	16
1	CABLE, TEST RS64	C-IA-7008668-0-0	15
1	POWER CABLE, RS64-TA	D-IA-7008588-0-0	14
1	WIRED ASSY (RS64-TA)	D-AD-7008524-0-0	13
1	MODULE PARTS LIST	A-PL-RS64-TA-2	12
2	MODULE RETAINER SCREW	7405642	11
2	FASTENERS, SOUTHCO #58-27-310-24	9008430	10
1	CONTROL PANEL ASSY. (RS64-TA)	D-AD-9305976-0-0	9
1	COVER, CHASSIS	E-IA-9605711-0-0	8
1	HINGE, TESTER CONT. PANEL	D-MD-9605710-0-0	7
2	BRKT, TESTER CHASSIS	C-IA-9605712-0-0	6
8	POP RIVETS AD43BS	9006509	5
1	DIVIDER BRK'T, TESTER	D-IA-9605713-0-0	4
1	BACK PANEL, TESTER	D-IA-9605714-0-0	3
1	CHASSIS, TESTER	E-IA-9605709-0-0	2
1	ATTACHÉ CASE	29 19153	1

PARTS LIST

CHK	CHANGE NO.	REV.		
[signature]	RS64TA-00001	A	M. Poirier 3-15-72	P. GADAIRE REDRAWN & REVISED, P. Gadaire 03/31/72
P.M.	RS64TA-00002	B	G.Q. Pepin 10/23/72	CLARK, Eddie J. Clark 11/30/72

REVISIONS

DEC FORM NO. DRD 100-A

FIRST USED ON OPTION/MODEL: RS64-TA

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL: —

FINISH: —

DRN. D. Schmidt	DATE 2/22/72
CHK'D. R. Russ	DATE 2/29/72
ENG. P. Gadaire	DATE 03/07/72
PROJ. ENG. P. Gadaire	DATE 03/31/72
PROD. P. Gadaire	DATE 03/31/72

NEXT HIGHER ASSY.: B-DD-RS64-TA

SCALE: NONE

SHEET | OF

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

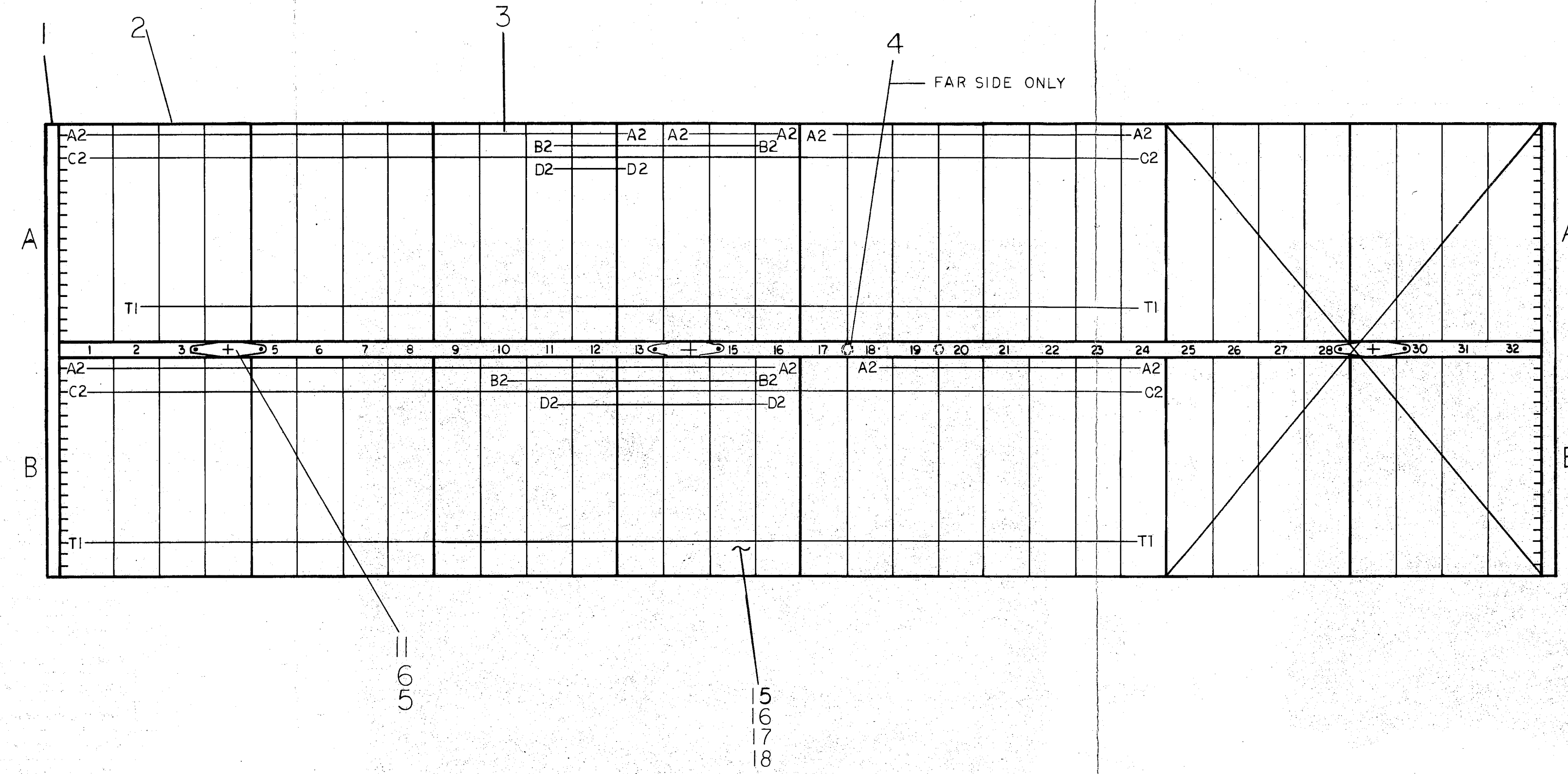
TITLE: TIMING TRACK WRITER TESTER (RS64-TA)

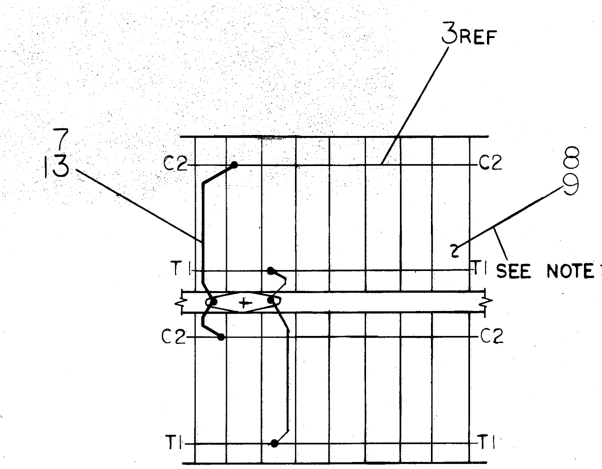
SIZE	CODE	NUMBER	REV.
D	UA	RS64-TA-Ø	B

DIST.

NOTES:

1. CONNECTIONS ON ITEM NUMBER 7 & 13 TO BE LOCATED AND SOLDERED AT MINIMUM PRACTICAL HEIGHT ABOVE BLOCKS.
2. USE YELLOW WIRE (ITEM # 8) FOR MACHINE WRAPPED AND BLUE WIRE (ITEM # 9) FOR HAND WRAPPED WIRING





DETAIL A
3 PLACES

REVISIONS

REV.	CHANGE NO.	CHK.
A	RS64TA-00001 M. Gracia 3-15-72 P. GADAIRE	
B	RS64TA-00002 G.G. Gagne 10/20/72 CLARK 11/21/72	

FIRST USED ON OPTION/MODEL	PDP-11
DO NOT SCALE DRAWING	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY √ REMOVE BURRS AND BREAK SHARP CORNERS	
MATERIAL	—
FINISH	—
DRN.	DATE 2-17-71
CHK'D	DATE 9-6-71
ENG.	DATE 9-29-71
PROJ. ENG.	DATE 9-29-71
PROD.	DATE 03/31/72
NEXT HIGHER ASSY	B-DD-RS64-TA
SCALE	NONE
SHEET	1 OF 2

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: WIRED ASS'Y

SIZE	CODE	NUMBER	REV.
D	AD	7008324-0-0	B

DIST.

DEC FORM NO. DRD 116

WIRE TABLE

ITEM NO	DESCRIPTION AWG	COLOR	CONNECTIONS FROM	TO	REMARKS
19 & 20	30	RED	A11 E2	B17 D2	TWP(4 TURNS PER INCH)
		WHT	A11 F2	B17 F2	
		RED	A12 E2	B17 H2	
		WHT	A12 F2	B17 K2	
		RED	A13 E2	B17 L2	
		WHT	A13 F2	B17 N2	
		RED	B11 E2	B17 S1	
		WHT	B11 F2	B17 P1	
		RED	B12 E2	B17 N1	
		WHT	B12 F2	B17 L1	
19 & 20		RED	B13 E2	B17 K1	TWP(4 TURNS PER INCH)
	30	WHT	B13 F2	B17 H1	
17	24	RED	B16 A2	B18 A2	+5V
17	24	RED	A01 A2	B01 A2	+5V
			A08 A2	B08 A2	
			A13 A2	B13 A2	
			A13 A2	A17 A2	
17	24	RED	A17 A2	A17 R1	+5V
17	24	RED	A24 A2	B24 A2	+5V
18	24	YEL	A14 A2	A13 D2	+20V
18	24	YEL	A13 D2	B13 D2	+20V
18	24	YEL	A16 A2	B16 D2	+20V
16	24	BLU	A12 B2	B12 B2	-15V
16	24	BLU	A16 B2	B16 B2	-15V

COMPONENT LIST

ITEM NO	COMP	POL	FROM		TO	POL	REMARKS
10	CAP	-	B01 F1		B01 L2	+	INS WIRES / ITEM
10	CAP	-	B01 R1		B01 S2	+	7, USE TERMI -
10	CAP	-	A05 C2		A03 A2	+	CLIPS ITEM 14
10	CAP	-	A11 B2		A09 C2	+	
10	CAP	-	A12 C2		A14 A2	+	
21	RES		A14 A2		A17 S2		
22	RES		A24 E1		A24 K1		
22	RES		A24 E2		A24 K2		
22	RES		A24 L1		A24 R1		

REVISIONS | REV. | CHANGE NO. | CHK

FIRST USED ON OPTION/MODEL: PDP-11	QTY.	DESCRIPTION: PARTS LIST	PART NO. / ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES: DECIMALS .XXX = .005, .XX = .02, .X = .1; ANGLES ±0° 30'	DRN.	DATE 2-19-71	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
	CHK'D.	DATE 2-19-71	
	ENG. John Maynard	DATE 9-29-71	TITLE: WIRED ASSY (RS64-TA)
	PROJ. ENG. John Maynard	DATE 9-24-71	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	PROD.	DATE 10/1/71	
MATERIAL: //	NEXT HIGHER ASSY. B-DD-RS64-TA		SIZE D CODE AD NUMBER 7008324-0-0 REV. B
FINISH: //	SCALE // SHEET 2 OF 2		DIST.

DEC FORM NO. DRD 102-B

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY A, CAMPBELL	CHECKED J. DEVIN	SECTION
DATE 2/18/71	DATE 9-22-71	1
ENG [signature]	PROD	ISSUED SECT.
DATE 9/24/71	DATE	1

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION
1	D-MD-9605733-0-0	FRAME CASTING REWORK 16"	1
2	D-SC-1205348-0-0	288 PIN BLOCK #H803	6
3	1205541	BUS STRIP	A/R
4	90-06210-6	SCR PHIL HD PHIL #8-32X5/8 SST	12
5	9006035	SCR PHIL HD PAN #8-32X1/2 SST	2
6	9007597	TERM #216-08-0-0 SHAKEPROOF	2
7	9107265-09	#22 TEFLON TUBING WHT	A/R
8	9105740-44	#30 AWG SOLID TEF INS WIRE (YEL)	A/R
9	9105740-66	#30 AWG SOLID TEF INS WIRE (BLU)	A/R
10	1000067	CAP 6.8 F 35V 20%	2
11	9006034	WASH INT TOOTH #8	2
~~12~~	~~A-BC-7406370-0-0~~	~~LOGIC FRAME DECAL WHT~~	~~A/R~~
13	9107560-01	#22 AWG BUS WIRE	A/R
14	9007655	TERMI POINT CLIP #85952-3	A/R
15	9107470-00	#24 AWG STRD TEF INS COLOR BLK	A/R
16	9107470-66	#24 AWG STRD TEF INS COLOR BLU	A/R
17	9107470-22	#24 AWG STRD TEF INS COLOR RED	A/R
18	9107470-44	#24 AWG STRD TEF INS COLOR YEL	A/R
19	9105740-22	#30 AWG STRD TEF INS WIRE (RED)	A/R
20	9105740-99	#30 AWG SOLID TEF INS WIRE (WHT)	A/R
21	1300298	RESISTOR 330 Ω 1W 10%	1
22	13-00365	RESISTOR 1 KΩ 1/4 5%	3

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
WIRED ASSY PARTS LIST	D-AD-7008324-0-0	A	PL	7008324-0-0	B	RS64TA 00002
	SHEET 1 OF 1	DIST.				

DEC FORM DEC 16-(325)-1031-N870
DRA 110

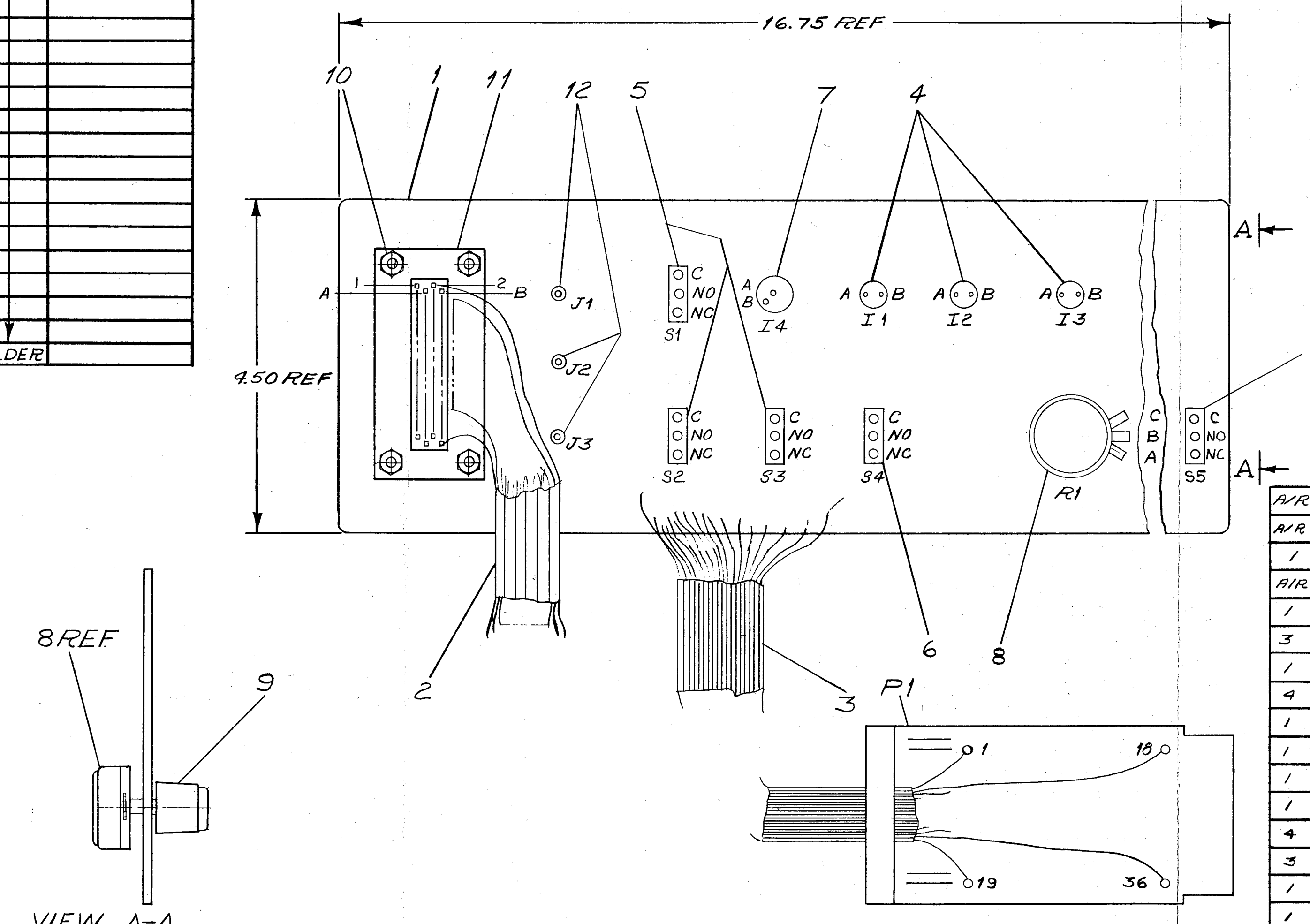
This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission. 1972

WIRE TABLE

ITEM NO.	DESCRIPTION COLOR	AWG.	FROM CONN.	FROM WITH	TO CONN.	TO WITH	REMARKS
3	BLK.	22	P1-10		J3	SOLDER	
	BRN.		P1-11		R1-C		
	RED		P1-12		J1		
	ORN		P1-13		I2-A		
	YEL		P1-14		I1-A		
	GRN		P1-15		I3-A		
	BLU		P1-16		S3-C		
	VIO		P1-17		S3-NO		
	GRY		P1-18		S1-C		
	WHT		P1-29		I3-B		
	BLK		P1-28		R1-B		
	BRN		P1-27		S2-C		
	RED		P1-26		S2-NO		
	ORN		P1-25		S4-NC		
	YEL		P1-24		S4-NO		
	GRN		P1-33		R1-A		
	BLU		P1-32		S5-NC		
	VIO		P1-31		S5-NO		
	GRY		P1-23		S5-C		
3	WHT	22	P1-22		J2		
7	RED	14	I4-A	SOLDER	S3-C		
7	BLK	14	I-4-B		S3-NC		
16	BLU	22	I2-B		I3-B		
16	BLU	22	I1-B		I2-B		
17	BLK	22	S3-NC		S4-C		
17	BLK	22	S4-C	SOLDER	R1-C	SOLDER	

EXTERNAL COMPONENT TABLE

ITEM	COMP	POL	FROM	TO	POL	REMARKS
15	CAP		S1-NO	S3-NC		USE WITH ITEM #14
13	DIO	−	R1-C	R1-A	+	" " " #14



PARTS LIST

QTY.	DESCRIPTION	PART NO.	ITEM NO.
A/R	WIRE, #22 AWG I.P.V.C. (BLK)	9107350-00	17
A/R	WIRE #22 AWG I.P.V.C. (BLU)	9107350-66	16
1	CAP 39 MMF 100 V	1000010	15
A/R	TUBING, TEFLON #22 AWG (BLU)	9107256-06	14
1	IN 753 DIODE	1202451	13
3	TERM., CAMBION	29-19155	12
1	BRKT, HOLD DOWN 36 PIN CONN	B-MD-9605726-0-0	11
4	KEP NUT #8-32	9006563	10
1	KNOB BUCKEYE	1204747	9
1	POT 10 TURN 200Ω, 2 W, 5%	13-09532-02	8
1	LAMP #1090-024 INDUS DEV	1205299	7
1	SWITCH MICRO PUSHBUTTON 1PBS	1203457	6
4	SWITCH MICRO 1PST 6AT1-T2	1201168	5
3	4908 IND LIGHT ASSY.	B-MA-4908-0-1	4
1	CONTROL PANEL CABLE	D-IA-7008589-0-0	3
1	DISK PLUG CABLE	D-IA-7008590-0-0	2
1	CONTROL PANEL (RS64-TA)	D-IA-9605676-0-0	1

REVISIONS

CHK	CHANGE NO.	REV.
—	RS64TA-00001 ORIGINATED	—
	RS64TA-00002 CLARK	A
	RS64TA-00004 J. BUZYNSKI	B

FIRST USED ON OPTION/MODEL: RS64-TA

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: .XXX = .005, .XX = .02, .X = .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL: SEE PARTS LIST

FINISH

DRN DATE 2/22/72 — CHK'D DATE 3-4-72 — ENG DATE 3-7-72 — PROJ. ENG. DATE 3/31/72 — PROD. DATE 3/31/72

NEXT HIGHER ASSY. D-UA-RS64-TA-0

SCALE NONE — SHEET OF

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: CONTROL PANEL ASSY RS64-TA

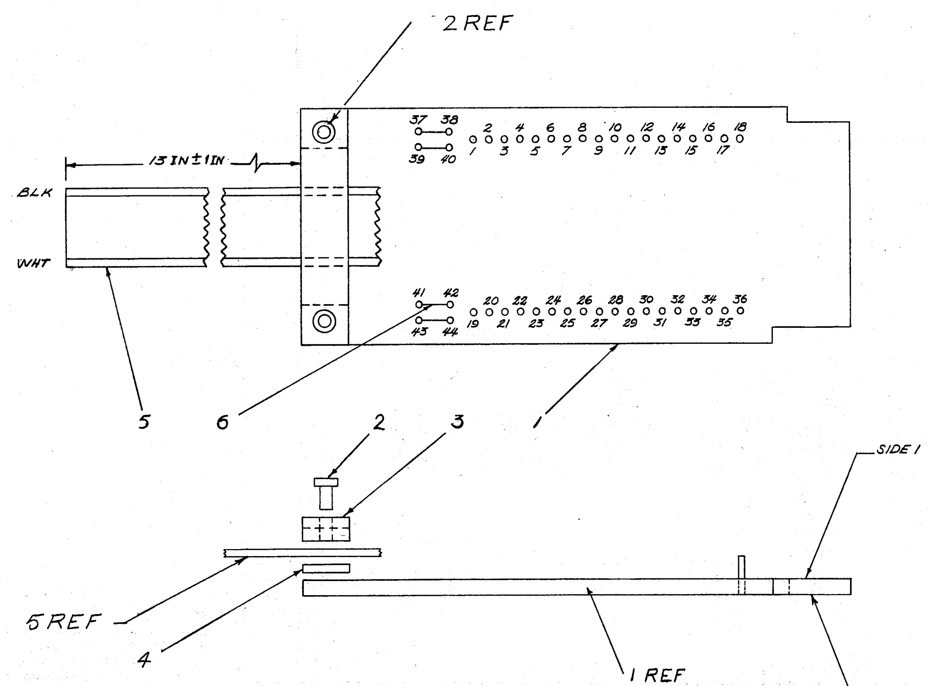
SIZE D — CODE AD — NUMBER 9305476-0-0 — REV. B

DIST.

DEC FORM NO. DRD 100-A

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.

NOTE:
1. FOR CABLE CONNECTIONS TO FRONT PANEL REFER TO DWG. D-AD-9305476-0-0



PARTS LIST			
ITEM NO	DESCRIPTION	PART NO	QTY
1	M908 MODULE	M908	1
2	EYELET GS-4-7 STIMPSON	9006732	2
3	CABLE CLAMP	1202704	1
4	4032 STOCK MT TAPE	9007834	A/R
5	20 CONDUCTOR RIBON CABLE	9107575	1
6	#22 AWG BUS WIRE	9107560-01	4
7	RESISTOR, 180 Ω, 1/4 W, 5%	1300260	1
8	RESISTOR, 390 Ω, 1/4 W, 5%	1300309	1
9	CAPACITOR, 6.8 MFD, 35V, 10%	1005306	1
10	RESISTOR, 1K Ω, 1/4 W, 5%	1300365	3
11	DIODE, D664	1100114	2
12	RESISTOR, 2K Ω, 1/4 W, 5%	1302388	1
13	RESISTOR, 8.2K Ω, 1/4 W, 5%	1301316	1
14	RESISTOR, 2.7K Ω, 1/4 W, 5%	1300426	1
15	RESISTOR, 3.9K Ω, 1/4 W, 5%	1300444	1
16	RESISTOR, 7.5K Ω, 1/4 W, 5%	1301422	2
17	#22 TEFLON TUBING (BRN)	9107256-01	A/R

WIRE TABLE					
ITEM NO	AWG	COLOR	FROM	TO	REMARKS
5	22	BLK	5	M908-10	SEE NOTE #1
5		BRN		-11	
5		RED		-12	
5		ONG		-13	
5		YEL		-14	
5		GRN		-15	
5		BLU		-16	
5		VIO		-17	
5		GRY		-18	
5		WHT		-29	
5		BLK		-28	
5		BRN		-27	
5		RED		-26	
5		ONG		-25	
5		YEL	5	-24	
6	22	BUSS	M908-37	M908-38	
6	22		-39	-40	
6	22		-41	-42	
6	22	BUSS	-43	-44	
5	22	GRN	5	M908-33	
5		BLU		-32	
5		VIO		-31	
5		GRY		-23	
5	22	WHT	5	M908-22	SEE NOTE #1

EXTERNAL COMPONENT TABLE						
ITEM NO	COMP	POL	FROM	TO	POL.	REMARKS
7	RES		M908-2	M908-5		USE ITEM 17 WITH ALL COMP.
8	RES		-2	-6		
9	CAP	+	-2	-6	–	
10	RES		-19	-24		
10	RES		-19	-25		
10	RES		-19	-26		
11	DIO	–	-21	-24	+	
11	DIO	–	-21	-25	+	
12	RES		-3	-7		
14	RES		-3	-8		
16	RES		-3	-9		
15	RES		-30	-36		
16	RES		-30	-35		
13	RES		M908-30	M908-34		

REVISIONS			
REV.	CHANGE NO.	CHK	
A	RS64TA-00001		M. Quinn 3-15-72
	P. GADAIRE		03/31/72

FIRST USED ON OPTION/MODEL: RS64-TA

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —//—
FINISH —//—

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

DRN. DATE 9-12-71
CHK'D DATE 9-15-71
ENG. DATE 9-24-71
PROJ. ENG. DATE 9-24-71
PROD. DATE 03/31/72

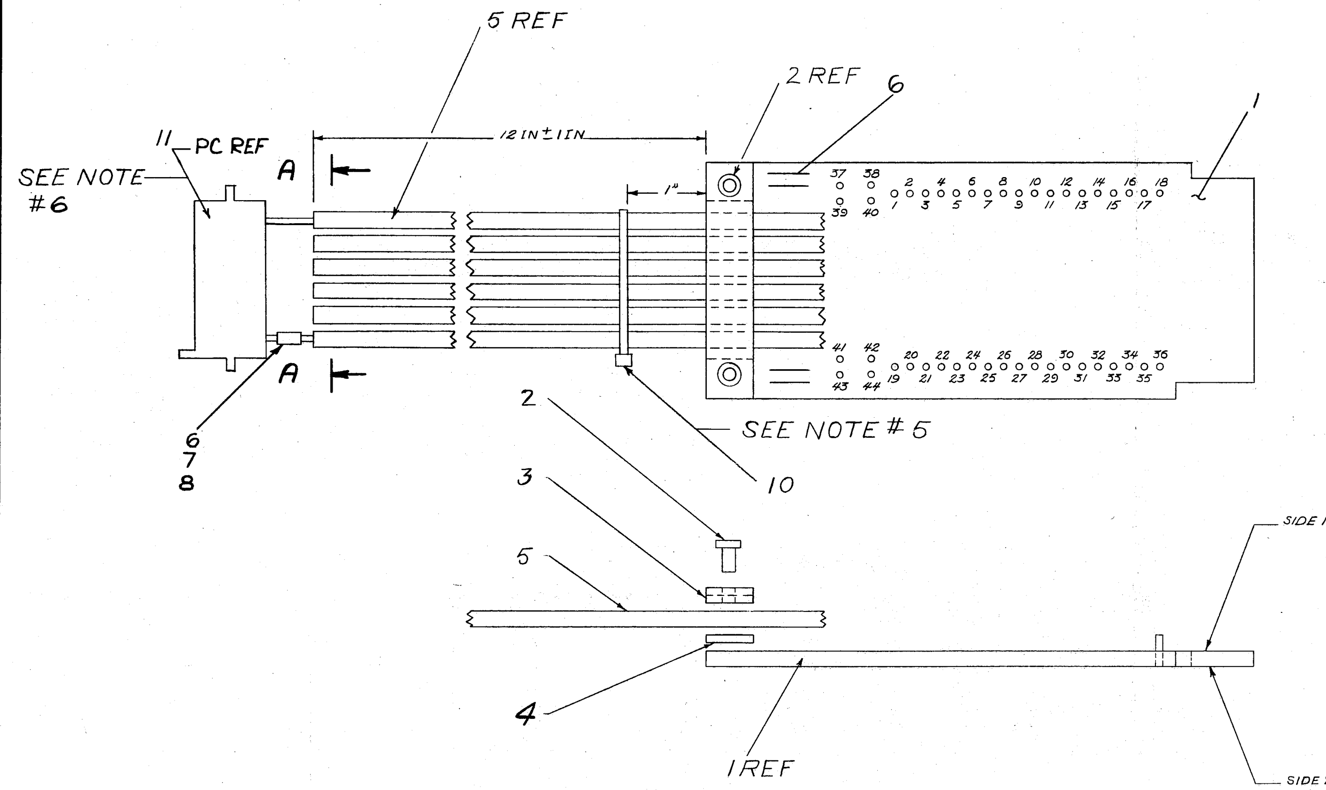
FIRST USED ON NEXT HIGHER ASSY: D-AD-9305476-0-0
SCALE —//—
SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: CONTROL PANEL CABLE (RS64-TA)

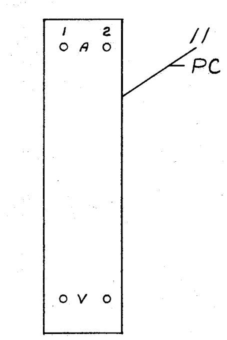
SIZE D CODE IA NUMBER 7ØØ8589-Ø-Ø REV. A

DEC FORM NO. DRD 102A



WIRE TABLE								
ITEM NO	AWG	COLOR	FROM	TO	EQUIP FROM	WITH ITEM	EQUIP TO WITH ITEM	REMARKS
5		RED	PC-D2	M908-22	6, 7, 8		8 & 9	A
5		WHT	PC-E2	-23				A
5		BLU	PC-F2	-24				A SEE NOTES 1,2,4,6
5		RED	PC-H2	-25				B
5		WHT	PC-J2	-26				B
5		BLU	PC-K2	-27				B
5		RED	PC-L2	-28				C
5		WHT	PC-M2	-29				C
5		BLU	PC-N2	-30				C
5		RED	PC-S1	-4				D
5		WHT	PC-R1	-5				D
5		BLU	PC-P1	-6				D
5		RED	PC-N1	-7				E SEE NOTES 1,3,4,6
5		WHT	PC-M1	-8				E
5		BLU	PC-L1	-9				E
5		RED	PC-K1	-10				F
5		WHT	PC-J1	-11				F
5		BLU	PC-H1	M908-12	6,7,8		8,9	F

PARTS LIST			
ITEM NO	DESCRIPTION	PART NO	QTY
1	M908 MODULE	M908	1
2	EYELET, GS-4-7 STIMPSON	9006732	2
3	CABLE CLAMP	1202704	1
4	4032 STOCK MT. TAPE	9007834	A/R
5	MICRODOT WIRE # 202-4007	1700014	6
6	#22 AWG BUS WIRE	9107560-01	A/R
7	SLEEVING	9008356	A/R
8	HY SHRINK TUBING 3/16"	9107254	A/R
9	#22 TEFLON TUBING (BROWN)	9107266-01	A/R
10	TIE WRAP SSTIM	9007031	A/R
11	36 PIN CONN BLOCK # H807	1209123	1



VIEW A-A

NOTES:

1. UNBRAID SHIELD THEN TWIST AND COVER SHIELD WITH ITEM 9.
2. SOLDER SHIELD ENDS A, B & C AT M908 END OF CABLE TO M908-21.
3. SOLDER SHIELD ENDS D, E & F AT M908 END OF CABLE TO M908-3.
4. COVER EXPOSED SHIELD AT BOTH ENDS WITH ITEM 8.
5. TIE WRAP AT 1" FROM M908 AND EVERY 3" THERE AFTER (ITEM 10), CABLE LENGTH IS 12".
6. DO NOT CONNECT SHIELD AT PC END OF CABLE

REVISIONS		
CHK	CHANGE NO.	REV.
	RS64TA-00001	A

FIRST USED ON OPTION MOD: RS64-TA

UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —//—

FINISH —//—

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

DRN. DATE 1/27/71
CHK'D DATE 9-15-71
ENG. DATE 9-29-71
PROJ. ENG. DATE 9-29-71
PROD. DATE 03/31/72

~~FIRST USED ON~~ NEXT HIGHER ASSY D-AD-7008698-0-0

SCALE —//—
SHEET 1 OF 1

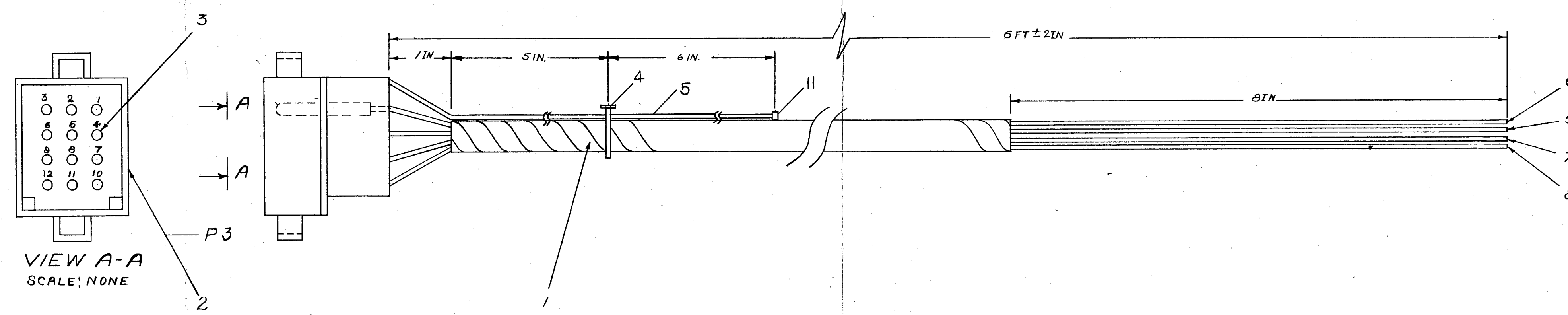
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DISK PLUG CABLE (RS64-TA)

SIZE	CODE	NUMBER	REV.
D	IA	7008590-0-0	A

DIST.

DEC FORM NO. DRD 102A



PARTS LIST			
ITEM NO.	DESCRIPTION	PART NO.	QUANTITY
1	SPIRAL WRAP TUBING, .250 OD	91-Ø724Ø	A/R
2	MATE-N-LOCK SOCKET HOUSING. AMP #1-48Ø278-Ø	12-Ø9351-12	1
3	MATE-N-LOCK CONTACT (MALE) AMP # 6Ø62Ø-1	12-Ø9378-12	8
4	TIE WRAP SST-1-5M	90-Ø788Ø	1
5	AWG #14 STRD TEF INS COLOR (BLACK)	91-Ø737Ø-ØØ	A/R
6	AWG #14 STRD TEF INS COLOR (RED)	91-Ø737Ø-22	A/R
7	AWG #14 STRD TEF INS COLOR (YELLOW)	91-Ø737Ø-44	A/R
8	AWG #14 STRD TEF INS COLOR (BLUE)	91-Ø737Ø-66	A/R
9	AWG #24 STRD TEF INS COLOR (RED)	91-07450-22	A/R
1Ø	AWG #24 STRD TEF INS COLOR (BLACK)	91-07450-00	A/R
11	AMP SOLDERLESS CONNECTOR	90-06776	1

WIRE TABLE						
ITEM NO.	AWG	COLOR	FROM	TO	EQUIP FROM WITH ITEM	EQUIP TO WITH ITEM
6	14	RED	P3-1	~~P1~~	3	~~*~~
5	14	BLACK	P3-6	~~P4~~	3	~~* NOTE 1~~
7	14	YELLOW	P3-8	~~P2~~	3	~~*~~
8	14	BLUE	P3-12	~~P5~~	3	~~*~~
9	24	RED	P3-3	P3-4	3	~~*~~
1Ø	24	BLACK	P3-5	P3-6	3	NOTE 1
5	14	BLACK	P3-9		3	11

NOTES:

1. PIN 6 HAS TWO WIRES ONE OF WHICH IS A JUMPER TO PIN 5
2. ~~* P1 THRU P4 ARE LOCATED ON THE CONTROL PANEL ASSY DWG D-AD-7008598-0-0~~

REVISIONS		
CHK.	CHANGE NO.	REV.
	RS64TA-00001 M. Quinn 3-15-72 P. GADAIRE	A
	RS64TA-00002 G.Q. Quinn 10/2/72 CLARK	B
	RS64TA-00003 1-28-73 J. BUZYNSKI	C

FIRST USED ON OPT MOD: RS64-TA

NEXT HIGHER ASSY: D-AD-7008598-0-0

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —//—

FINISH —//—

DRN. C. Law DATE 2-3-71
CHK'D DATE 9-15-71
ENG. DATE 9-29-71
PROJ. ENG. DATE 9-29-71
PROD. DATE 3-31-72

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: POWER CABLE (RS64-TA)

SIZE D CODE A NUMBER 7ØØ8588-Ø-Ø REV. C

SCALE —//— SHEET 1 OF 1

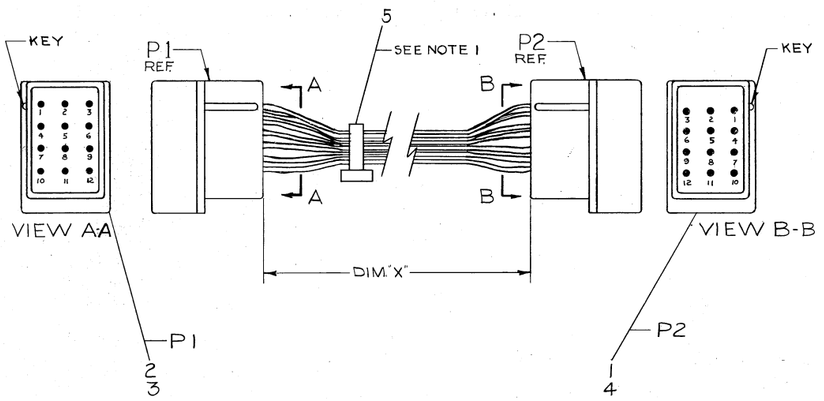
DEC FORM NO. DRD 102A

WIRE TABLE

ITEM NO.	DESCRIPTION AWG.	COLOR	FROM CONNECTION	TO CONNECTION	REMARKS
6	18	RED	P1-1	P2-1	
6	18	RED	P1-2	P2-2	
6	18	RED	P1-3	P2-3	
6	18	RED	P1-4	P2-4	
7	18	BLK.	P1-5	P2-5	
7	18	BLK.	P1-6	P2-6	
7	18	BLK.	P1-9	P2-9	
8	18	GRN.	P1-8	P2-8	
8	18	GRN.	P1-7	P2-7	
9	18	BLU.	P1-10	P2-10	
9	18	BLU.	P1-11	P2-11	
9	18	BLU.	P1-12	P2-12	

LEGEND NUMBER	VARIATION DIM. X
7008668-2	2.0" ± .5"

NOTE:
1. ASSEMBLE ITEM #5(TIE,CABLE) EVERY 3.0 INCHES



A/R	WIRE #18 AWG. STD TEF INS. (BLU.)	9107360-66	9
A/R	WIRE #18 AWG. STD. TEF INS. (GRN.)	9107360-55	8
A/R	WIRE #18 AWG. STD. TEF INS. (BLK.)	9107360-00	7
A/R	WIRE #18 AWG STD. TEF. INS. (RED)	9107360-22	6
A/R	TIE, CABLE SST-1-5M	9007680	5
1	HOUSING, SOCKET 1-480275-0 AMP	1209350-12	4
1	HOUSING, PIN CONT. 1-480278-0 AMP	1209351-12	3
12	TERM., PIN CONT. 60620-4 AMP	1209378-01	2
12	SOCKET, TERM. CONT. 60619-4 AMP	1209379-01	1

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RS64		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: .XXX ± .005, .XX ± .02, .X ± .1; ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL: SEE PARTS LIST
FINISH

		DATE
DRN.	[illegible]	10/29/71
CHK'D.	[illegible]	11/1/71
ENG.	[illegible]	11-31-71
PROJ. ENG.	[illegible]	11-3-71
PROD.	[illegible]	11-3-71

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: RS64 P/S TEST CABLE

NEXT HIGHER ASSY.

SIZE	CODE	NUMBER	REV.
C	IA	7008668-0-0	

SCALE NONE
SHEET 1 OF 1
DIST.

REVISIONS: REV. | CHANGE NO. | CHK.

DEC FORM NO. DRC 100-A

SIZE C CODE IA NUMBER 7008668-0-0 REV.

CNT=19 · ST TM · CLK · CNT=19 · CLR CNT · STP · EOB · ST TM · CNT=Ø5 · CNT = 19 · M3 (1) · M3(1) · CNT=Ø2 · CLK A · SEN (Ø) · CLR CNT · (CLEAR) · (SHIFT ENA) · (SER IN) · (LOAD ENA) · SEN (Ø) · STP TTC (Ø) · SER OUT · CNT=Ø2 · RUN · ARC Ø1(1) · ARC Ø6(1) · ARC Ø3 (1) · ARC Ø4 (1) · ARC Ø3(1) · ARC Ø4(1) · ARC Ø6 (1) · ARC Ø3 (1) · ARC Ø4 (1) · ARC II (1) · CNT=19 · STP TTC (Ø) · ARC Ø1 (1) · ARC II (1) · ARC II (1) · B19 D2 · B19 H1 · B19 D2 · RC11 TTB · B19 H1 · RC11 LWD · RC11 TTC · SER OUT · +5V · 1KΩ · +5V · 1KΩ · RC/8 E · RC 11 · TTB · RUN CLR · RUN CLR · TTC

FIRST USED ON OPTION/MODEL	RS64-TA
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES	DECIMALS: .XXX = .005, .XX = .02, .X = .1 · ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	
MATERIAL	
FINISH	
DRN.	Barry — DATE 11.6.72
CHK'D	— DATE 11/27/72
ENG	Ellen J Clark — DATE 11/27/72
PROJ. ENG.	Ellen J Clark — DATE 11/27/72
PROD.	Ellen J Clark — DATE 11/30/72
NEXT HIGHER ASSY.	
SCALE	—
SHEET	OF

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: RS64 TTW RC8/E

QTY.	DESCRIPTION	PART NO.	ITEM NO.

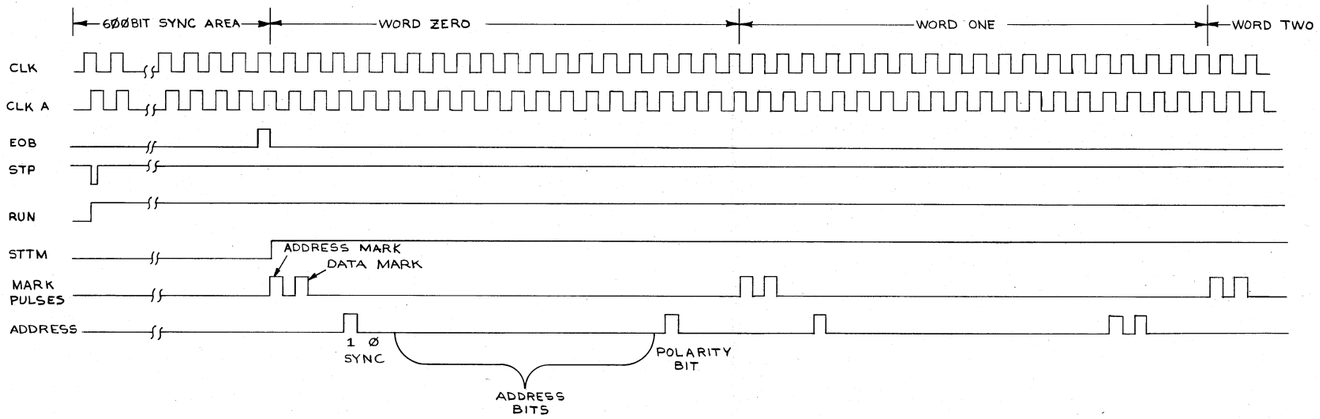
PARTS LIST

SIZE	CODE	NUMBER	REV.
D	BS	RS64-TA-Ø9	—

DIST.

REVISIONS	REV.
CHANGE NO	—
RS64-TA-OCOOO2	
ORIGINATED	
CHK	

DEC FORM NO DRD 102-B



REVISIONS	REV.	CHANGE NO.	CHK

BRUNING 40-107 15968

DEC FORM NO DRD 100-A

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP8/E		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS: .XXX = .005, .XX = .02, .X = .1 — ANGLES: ±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL

FINISH

DRN. E. CLARK	DATE 10-3-72	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D. P. McCullough	DATE 11-21-72	
ENG. Ellen Clark	DATE 11/21/72	
PROJ. ENG. Ellen Clark	DATE 11/21/72	
PROD. Ellen Clark	DATE 11/21/72	

NEXT HIGHER ASSY.

SCALE

SHEET 1 OF 1

TITLE: RS64 TIMING DIAGRAM RC8/E FORMAT

SIZE	CODE	NUMBER	REV.
D	TD	RS64-TA-Ø8	

DIST.

SIZE D TD NUMBER RS64-TA-Ø8 REV.

RS64 TIMING TRACK WRITER MAINTENANCE LOG

DATE	MAINTENANCE (Check One)		FAULT SYMPTOMS	SOLUTION
	Preventive	Corrective		

Reader's Comments

RS64 TIMING TRACK WRITER
MAINTENANCE MANUAL
DEC-FS-HRSMM-A-D

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults do you find with the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

Would you please indicate any factual errors you have found. _____

_____

_____

_____

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

CUT OUT ON DOTTED LINE

— — — — — — — — — — — — Fold Here — — — — — — — — — — — —

— — — — — — — — — — Do Not Tear - Fold Here and Staple — — — — — — — —

FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

Postage will be paid by:

Digital Equipment Corporation
Technical Documentation Department
146 Main St.
Maynard, Massachusetts 01754

Digital Equipment Corporation
Maynard, Massachusetts

printed in U.S.A.