

pdp11

DL11  
asynchronous  
line interface  
engineering drawings

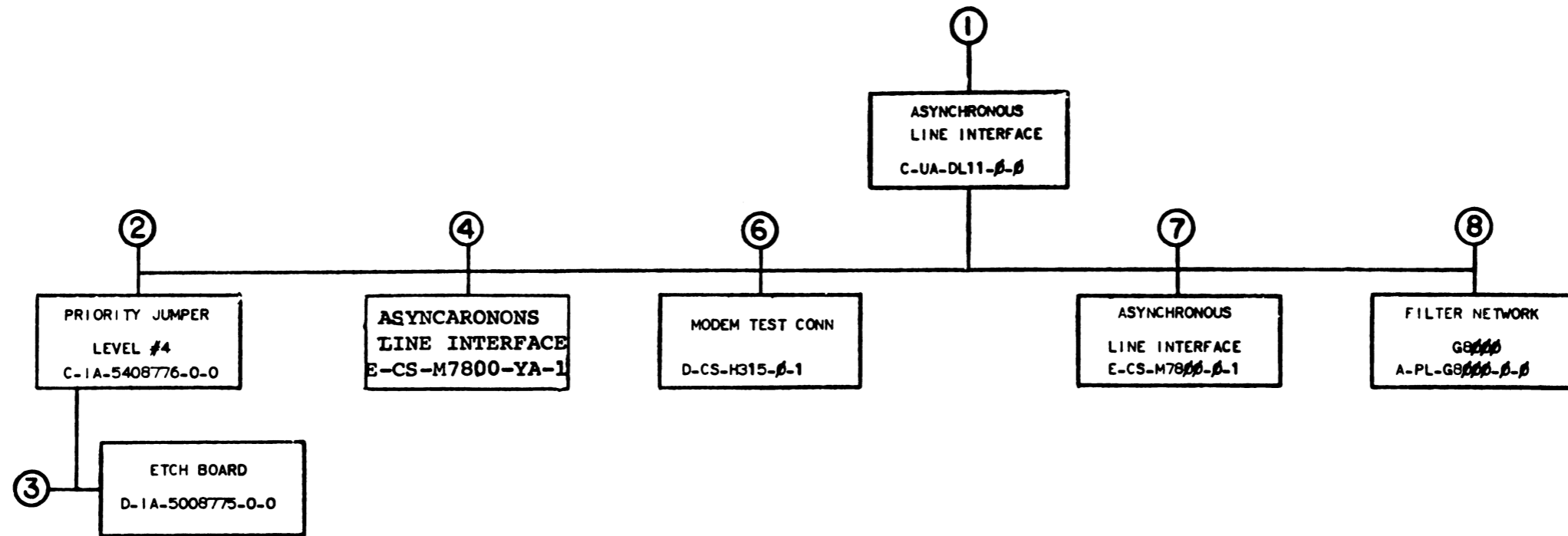
digital



**DL11  
asynchronous  
line interface  
engineering drawings**



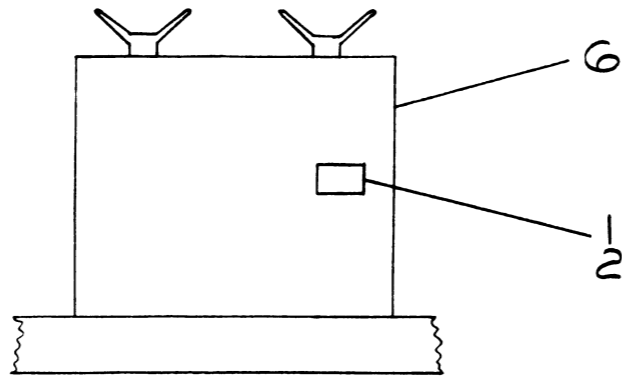




TITLE	ASYNCHRONOUS LINE INTERFACE	SHEET 2 OF 3	SIZE CODE B DD	NUMBER DL11 - Ø	REV K
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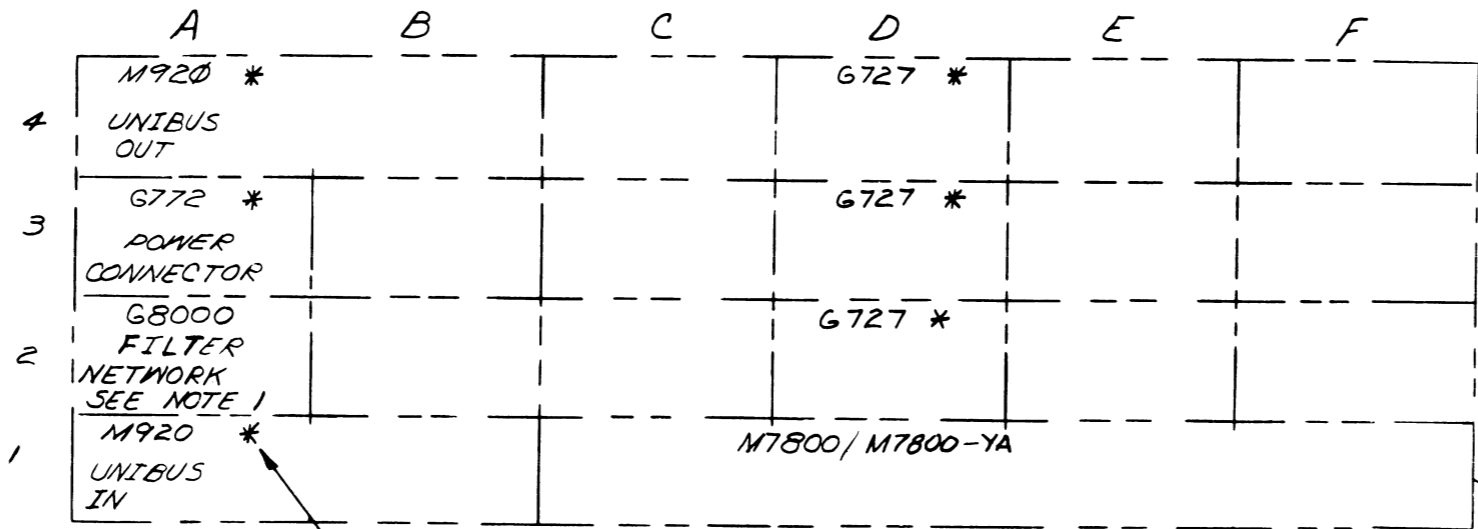


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1972



NOTES:

- G 8000 IS REQUIRED ONLY IN PDP 11 SYSTEMS WHERE +15V IS NOT AVAILABLE. THE INSTALLATION REQUIRES 2 WIRES TO BE ADDED.  
A03V2-A02V2  
A02N2-CXXUI  
WHERE (XX) IS THE SLOT NUMBER CONTAINING THE DL11.
- ITEMS INDICATED WITH ASTERICK (\*) ARE SHOWN FOR REFERENCE ONLY AND ARE NOT PART OF THIS UNIT.



DD11-A\*

SEE NOTE 2

REV.	CHG. NO.	DATE	BY
A	DL11-00001	2-18-72	R. JANSON
B	DL11-00002	7-17-72	R. JANSON
C	DL11-00005	12-5-72	R. JANSON
D	DL11-00006	7-31-73	L. CONDON
E	DL11-00008	11-1-73	L. CONDON
F	DL11-00009	12-FEB-76	J. MCINTYRE

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP-11		PARTS LIST		
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES	DRN. <i>M. Rivera</i>	DATE <i>7/18/72</i>	<b>digital</b> EQUIPMENT CORPORATION <small>MAYNARD, MASSACHUSETTS</small>	
DECIMALS	CHK'D. <i>A. F. Jensen</i>	DATE <i>4-29-72</i>		
ANGLES	ENG. <i>P. E. Jensen</i>	DATE <i>5-11-72</i>		
.XXX = .005 .XX = .02 .X = .1	PROL ENG. <i>P. E. Jensen</i>	DATE <i>5-11-72</i>		
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	BROD. <i>J. McIntyre</i>	DATE <i>5-15-72</i>	TITLE <b>ASYNCHRONOUS LINE INTERFACE</b>	
MATERIAL	NEXT HIGHER ASSY.		SIZE CODE	NUMBER
FINISH			C UA	DL11-0-0
			DIST. G	

REV. E  
NUMBER DL11-0-0  
SIZE CODE C UA



**DIGITAL EQUIPMENT CORPORATION**  
MAYNARD, MASSACHUSETTS  
**PARTS LIST**

MADE BY M. PIERCE	CHECKED J. FERGUSON	SECTION
DATE 4/27/72	DATE 4/27/72	1
ENG P. E. JANSON	PROD <i>J. Mc Jone</i>	ISSUED SECT.
DATE 5/11/72	DATE 5/15/72	1

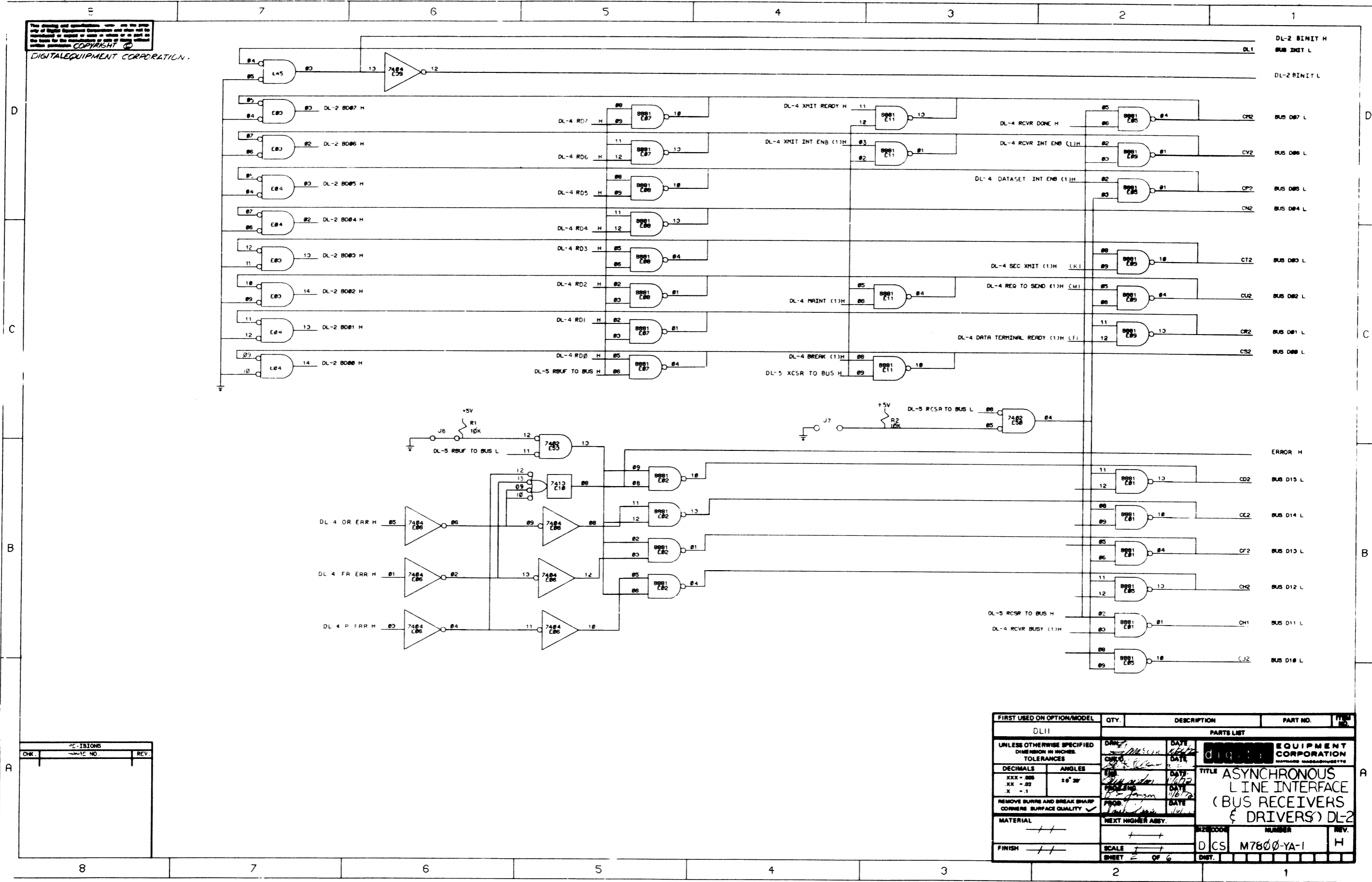
**QUANTITY/VARIATION**

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E								
1	C-IA-5408776-0-0	PRIORITY JUMPER LEVEL #4	1	1	1	1	1								
3	D-UA-BC05C-25	CABLE MODEM BC05C	-	1	-	1	1								
4	D-IA-7008360-0-0	CABLE ASSEMBLY (KL8E)	1	-	1	-	-								
5	D-CS-H315-0-1	MODEM TEST CONNECTOR	-	-	-	-	-	A/R	See Note 2						
6	E-CS-M7800-0-1	ASYNCHRONOUS LINE INTERFACE	-	1	-	1	1								
7	<del>C-PL-00000-0-0</del>	<del>FILTER NETWORK</del>	<del>-</del>	<del>A/R</del>	<del>-</del>	<del>A/R</del>	<del>A/R</del>	<del>A/R</del>	<del>See Note 1</del>						
8		CRYSTAL	A/R	RA	RA	RA	RA	F	See Note 3						
9	E-CS-M7800-YA-1	ASYNCHRONOUS LINE INTERFACE	1	-	1	-	-								
10	9008269	TRANSPARENT VINYL TAPE	A/R												
NOTES:															
1. G8000 IS REQUIRED ONLY IN PDP11 SYSTEMS WHERE +15V IS NOT AVAILABLE. ONE PER DD11-A															
2. ONE H315 PER PDP11 SYSTEM															
3. CRYSTAL FREQUENCY DEFINED BY CUSTOMER SPECIFIED BAUD RATE OR BY THE DOCUMENTATION OF AN OPTION WHICH USES THE DL11.															
4. APPLY TAPE TO TOP SURFACES OF CRYSTAL AND MOUNTING BRACKETS TO INSULATE FROM ADJACENT MODULES.															
5. PRIORITY LEVELS 5, 6, or 7 MAY BE SPECIFIED BY THE CUSTOMER OR THE DOCUMENTATION OF AN OPTION WHICH USES THE DL11.															

TITLE	ASYNCHRONOUS LINE INTERFACE	ASSY NO.	C-UA-DL11-0-0	SIZE	A	CODE	PL	NUMBER	DL11-0-0	REV.	F	ECO NO.	DL11-00009
SHEET 1 OF 1		DIST.											



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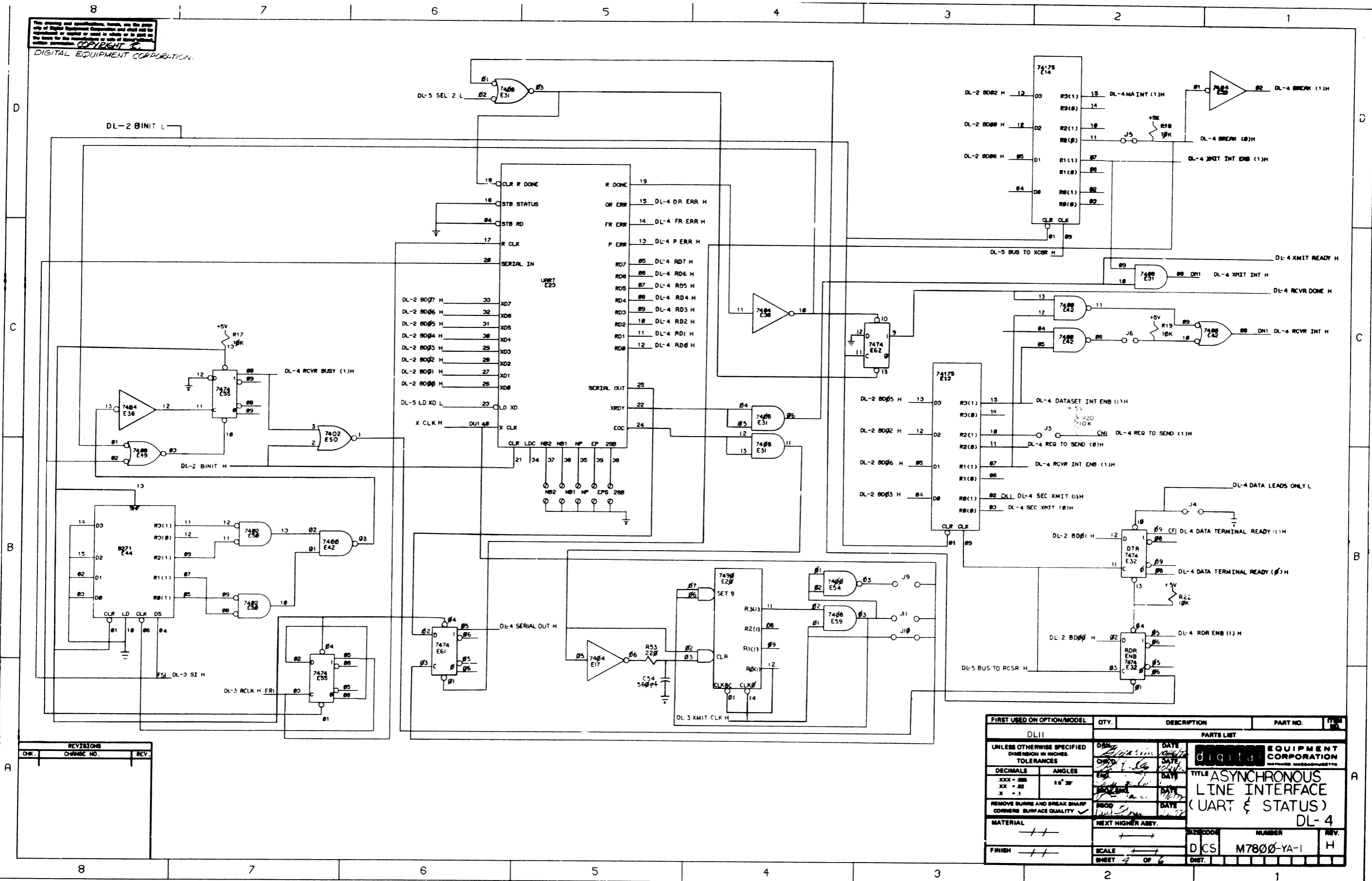
REVISIONS		
CHK	REV. NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DL11		PARTS LIST		
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES		DATE: 11/17/72	DATE: 11/17/72	DIGITALEQUIPMENT CORPORATION M7800-YA-1
DECIMALS	ANGLES	DATE: 11/17/72	DATE: 11/17/72	
XXX - .005	±0° 30'	DATE: 11/17/72	DATE: 11/17/72	TITLE ASYNCHRONOUS LINE INTERFACE (BUS RECEIVERS & DRIVERS) DL-2
.XX - .02		DATE: 11/17/72	DATE: 11/17/72	
X - .1		DATE: 11/17/72	DATE: 11/17/72	
REMOVES BURRS AND BREAK SHARP CORNERS SURFACE QUALITY		DATE: 11/17/72	DATE: 11/17/72	
MATERIAL	NEXT HIGHER ASSY.	DATE: 11/17/72	DATE: 11/17/72	
FINISH	SCALE	DATE: 11/17/72	DATE: 11/17/72	
	SHEET 2 OF 6	DATE: 11/17/72	DATE: 11/17/72	



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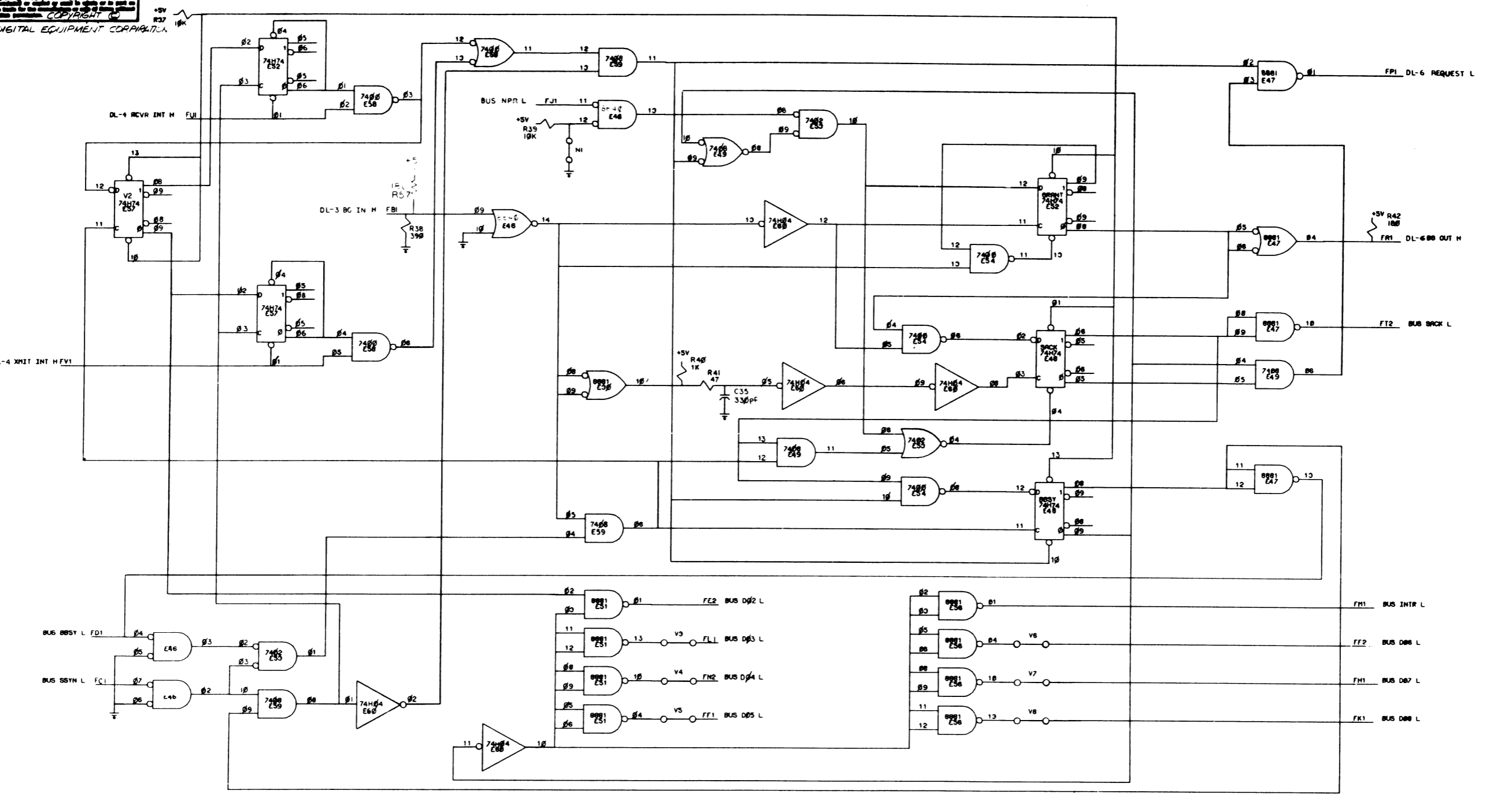
REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	TITLE
DL11				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES				
DECIMALS		ANGLES		
.XXX - .000		± 0° 30'		
.XX - .00				
.X - .0				
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY				
MATERIAL		NEXT HIGHER ASSY.		
FINISH		SCALE		
		SHEET 4 OF 6		

PARTS LIST		EQUIPMENT CORPORATION	
TITLE	NUMBER	REV.	
ASYNCHRONOUS LINE INTERFACE (UART & STATUS)	M7800-YA-1	H	
DL-4			



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NOTE: THE V LINES ARE TO BE JUMPED FOR A 1.

REVISIONS		
CHK	CHANGE NO.	REV.

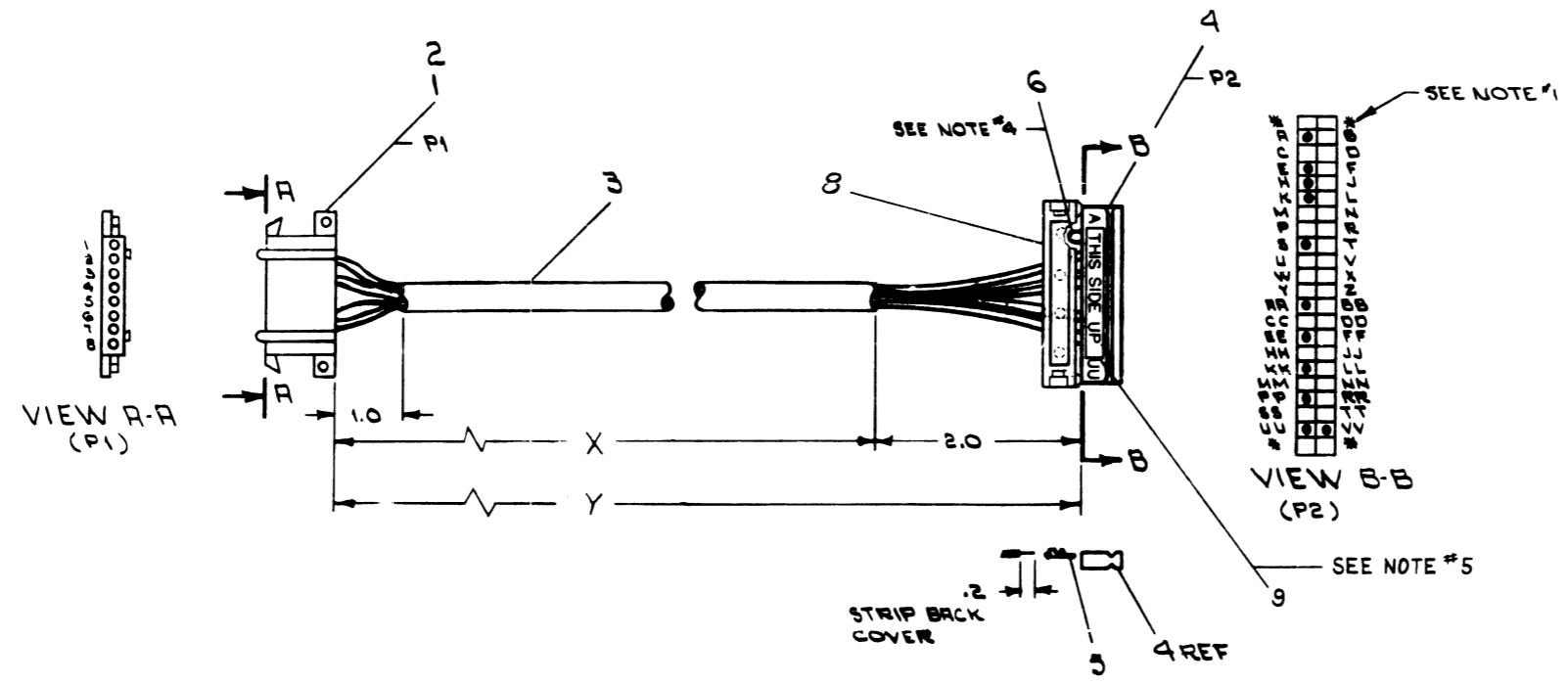
FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	TITLE
DL11				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES				
DECIMALS		ANGLES		
.XXX - .000		± 0° 30'		
.XX - .00				
.X - .1				
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY				
MATERIAL		NEXT HIGHER ASSY.		
FINISH		SCALE		
		SHEET 6 OF 6		
PARTS LIST			TITLE	
DIGITAL EQUIPMENT CORPORATION			ASYNCHRONOUS LINE INTERFACE (INTERRUPT CONTROL) DL-6	
D CS M7800-YA-1			REV. H	

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WIRE TABLE						
ITEM NO.	AWG	COLOR	PAIR NO.	FROM CONNECTION	WITH CONNECTION	TO CONNECTION
3	22	BLK	1	P1-2	2	P2-KK
3		RED		P1-3	2	P2-S
3,7		SHIELD		SEE NOTE #2	-	P2-R(NOTE#3)
3		BLK	2	P1-4	2	P2-EE
3		WHT		P1-5	2	P2-RR
3,7		SHIELD		SEE NOTE #2	-	P2-UU(NOTE#3)
3		BLK	3	P1-6	2	P2-PP
3		GRN		P1-7	2	P2-K
3,7		SHIELD		SEE NOTE #2	-	P2-VV(NOTE#3)
6	22	BLK	-	P2-E	5	P2-H

LEGEND		
VARIATION	LENGTH	
	X	Y
7008360-0	25IN±1.0	27IN±1.0
7008360-1	46IN±1.0	48IN±1.0

- NOTES:
- \* ASTERISKS INDICATE CAVITIES NOT USED OR DESIGNATED BY LETTERS.
  - DRAIN WIRES TO BE CUT BACK TO OUTER INSULATION ON P1 END OF CABLE ONLY. SHIELDS TO BE CUT BACK TO OUTER INSULATION ON BOTH ENDS OF CABLES.
  - DRAIN WIRES ON P2 END OF CABLE TO BE EACH ENCLOSED WITH ITEM #7 (TUBING) FROM END OF CABLE JACKET TO POINT WHERE THEY ENTER P2 CONNECTOR.
  - ITEM #6 (WIRE) TO BE APPROXIMATELY ONE (1) INCH LONG.
  - PLACE ITEM #9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM #4 (BERG HOUSING) AS SHOWN.



REV.	DATE	BY	CHKD.	DESCRIPTION
A	10/19/71	R. REGAN		INITIAL DESIGN
B	11/10/71	R. REGAN		REVISED TO ADD SHIELD
C	12/22/71	R. REGAN		REVISED TO ADD DRAIN WIRE
D	1/21/74	R. REGAN		REVISED TO ADD CONTACT MATE-LOCK
E	3/21/74	R. REGAN		REVISED TO ADD STRIP BACK COVER
F	10/14/74	R. REGAN		REVISED TO ADD THIS SIDE UP STICKER

FIRST USED ON OPTION / MODEL  
PDP-8E

DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED
TOLERANCES	ANGLES = 0°30'
FINISH SURFACE QUALITY	REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL	SEE PARTS LIST
FINISH	

DATE: 11/22/71	DATE: 11/22/71	DATE: 11/22/71	DATE: 11/22/71
CHKD: [Signature]	ENG: [Signature]	PROJ. ENG: [Signature]	PROD: [Signature]
<b>digital EQUIPMENT CORPORATION</b> MAYNARD, MASSACHUSETTS			
<b>CABLE ASSEMBLY (KL8E)</b>			
SIZE CODE: DIA	NUMBER: 7008360-0-0	REV: F	
SHEET: 1	OF: 1	DIST: 1	

QTY	DESCRIPTION	PART NO.	ITEM NO.
1	LABEL, THIS SIDE UP	3611567	9
1	DRAIN TUB	21116	8
1	AIR TUB #18 TEF. THINWALL NAT	910278-11	7
1	AIR WIRE #22 AWG STRD TEF BLK	9107350-00	6
1	SOCKET, CRIMP #4 7216	1210089-07	5
1	HOUSING, BERG #.50 43-715	1210317-15	4
1	CABLE, BELDEN #8TT-3PR SHLD	9107723-0	3
6	CONTACT MATE-LOCK (FEMALE)	1209379-03	2
1	CONN. MATE-LOCK (FEMALE)	1209340-00	1

PART NO. DIA 7008360-0-0 E





DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				LEGEND		QUANTITY / VARIATION											
ACCESSORY LIST				D	DOCUMENT	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	KIT CHECK	BY	DATE	INSTALLATION CHECK	BY	DATE	
MADE BY	E. Pellegrini	CHECKED	<i>P. Janson</i>	DN	DOCUMENT CHANGE NOTICE												
DATE	June 26, 1972	DATE	<i>8-8-72</i>	PA	PAPER TAPE ASCII												
ENG	Paul Janson	PROD.	<i>J. Miller</i>	PB	PAPER TAPE BINARY												
DATE	June 26, 1972	DATE	<i>8-8-72</i>	PM	PAPER TAPE READ-IN-MODE												
SECTION		ISSUED SECT.															
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION				DL11-A	DL11-B	DL11-C	DL11-D	DL11-E							
1	M7800	ASYNCHRONOUS LINE INTERFACE (EIA)				1	1	1	1	1							
2	G8000	FILTER NETWORK				0	A/R	0	A/R	0							
3	M7800-YA	ASYNCHRONOUS LINE INTERFACE (CURRENT LOOP)				1	0	1	0	0							
4	5408776	PRIORITY JUMPER LEVEL #4				1	1	1	1	1							
5	BC05-C-25	MODEM CABLE				0	1	0	1	1							
6	7008360	TTY CABLE				1	0	1	0	0							
7	-	CRYSTAL				1	1	1	1	1							
8	-	DL11 ENGINEERING DRAWINGS				1	1	1	1	1							
9	DEC-11-HDLAA-A-D	DL11 ASYNCHRONOUS LINE INTERFACE MANUAL				1	1	1	1	1							
10	LIBKIT-11-KL11-04	KL11 MAINDEC				1	1	0	0	0							
11	LIBKIT-11-DL11C-A-K	DL11 MAINDEC				0	0	1	1	0							
12	LIBKIT-11-DL11E-A-K	DL11 MAINDEC				0	0	0	0	1							
13	H315	MODEM TEST CONNECTOR				0	0	0	0	A/B							
NOTES: 1. G8000 IS REQUIRED ONLY IN PDP-11 SYSTEMS WHERE +15V IS NOT AVAILABLE. ONE PER DD11-A.																	
2. CRYSTAL FREQUENCY DEFINED BY CUSTOMER SPECIFIED BAUD RATE.																	
3. ONE H315 PER PDPII SYSTEM																	
4. INSURE THAT TRANSPARENT VINYL TAPE HAS BEEN APPLIED TO THE TOP SURFACE OF THE CRYSTAL AND MOUNTING BRACKET.																	
TITLE				ASSY. NO.	SIZE CODE	NUMBER			REV.	ECO NO							
DL11 CHECK LIST					A AL	DL11-0-5			C	DL11-00005							
SHEET 1 OF 1				DIST.													

**DIGITAL EQUIPMENT CORPORATION**  
MAYNARD, MASSACHUSETTS

DATE 6-21-72

TITLE DL11 INSTALLATION PROCEDURE

REVISIONS					
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY
C	CHANGE PER ECO	DL11-4	JANSON	3/73	<i>P. Danon</i>
D	CHANGE PER ECO	DL11-5	CONDON	7/73	<i>P. Condon</i>
E	CHANGE PER ECO	DL11-7	CONDON	8/74	<i>P. Condon</i>
F	CHANGE PER ECO	DL11-8	CONDON	4-75	<i>P. Condon</i>

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ENG PAUL E. JANSON  
DEC FORM NO 16-1081-1022-0370  
DRA 108

APPD *P. E. Janson*

SIZE CODE A SP  
NUMBER DL11-0-2  
REV F

SHEET 1 OF 9

**ENGINEERING SPECIFICATION**

TITLE DL11 INSTALLATION PROCEDURE

DL11 INSTALLATION PROCEDURE:

Installation of the M7800 module or its variation as a DL11-A through DL11-E option consists of the following preparations:

1. Jumper insertion/deletion for selection of operation mode (A, B, C, D, or E).
2. Register address assignment.
3. Vector address assignment.
4. Priority assignment.
5. Special NPR jumper insertion/deletion.
6. Selection of data format (data bits, stop bits, parity).
7. Selection of crystal for baud rate.
8. Installation of 68000 in systems where +15v is not available.
9. Filter capacitor selection for high baud rate current-loop.

**OPERATION MODE:**

The following describes the jumpers associated with controlling the mode of operation (A,B,C,D, or E):

- J1. Ties EIA driver to REQUEST-TO-SEND lead (pin 4) of dataset cable. IN for DL11-B,D, and E; does not affect DL11-A and C. Drawing DL-7.
- J2. Ties EIA driver, normally used for the REQUEST-TO-SEND lead, to FORCE BUSY lead (pin 25) for use with Bell 103E. This is a customer option. If not specified, Jumper is OUT for all DL11's. Drawing DL-7.
- J3. When inserted, allows REQUEST-TO-SEND lead (pin 4) to be controlled by bit 2 of the receiver status register. OUT for DL11-B and D; IN for DL11-E; does not affect DL11-A and C. Drawing DL-4.
- J4. When inserted, forces "DATA LEADS ONLY" mode of EIA operation. Turns DATA TERMINAL READY (pin 20) and REQUEST-TO-SEND (pin 4) on. IN for DL11-B and D; OUT for DL11-E; does not affect DL11-A and C. Drawing DL-4.
- J5. When inserted, allows the BREAK bit to function. OUT for DL11-A and B; IN for DL11-C,D, and E. Drawing DL-4.
- J6. When inserted, allows DSET INT to cause interrupts. OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-4.
- J7. When inserted, allows dataset control bits to be read as part of the receiver status register.

DEC FORM NO 16-1081-1022-0370  
DRA 108

SIZE CODE A SP  
NUMBER DL11-0-2  
REV F

SHEET 2 OF 9

**ENGINEERING SPECIFICATION**

TITLE DL11 INSTALLATION PROCEDURE

- J7. (con't)  
OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-2.
- J8. When inserted, allows error bits to be read as part of the receiver data register. OUT for DL11-A and B; IN for DL11-C,D and E. Drawing DL-2.

Summary of mode control jumpers:

JUMPER	A	B	C	D	E	DRAWING
J1	OUT	IN	IN	IN	IN	DL-7
J2	OUT	OUT	OUT	OUT	OUT	DL-7
J3	*	IN	IN	IN	IN	DL-4
J4	*	IN	IN	IN	IN	DL-4
J5	OUT	OUT	IN	IN	IN	DL-4
J6	OUT	OUT	OUT	OUT	IN	DL-4
J7	OUT	OUT	OUT	OUT	IN	DL-2
J8	OUT	OUT	IN	IN	IN	DL-2

\* = don't care

**B. REGISTER ADDRESS ASSIGNMENTS:**

The DL11 can respond to addresses with the following format:

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	1	1	1	1	1	1	1	1	JUMPERS								1	0

Selects 1 of 4 Registers

Byte Control

Bits 10 through 3 are controlled by jumpers A10 to A3. A Jumper inserted indicates a zero.

For the DL11-A and B used as the console device, address 777560 is assigned. For additional units, assign 776XX0, where XX=50 for the first additional unit and XX=67 for the 16th unit.

For the DL11-C,D and E assign address 77XXX0, where XXX=561 for the first line, and XXX=617 for the 31st line. Assign all C's first, then D's, and then E's.

DEC FORM NO 16-1081-1022-0370  
DRA 108

SIZE CODE A SP  
NUMBER DL11-0-2  
REV F

SHEET 3 OF 9

**ENGINEERING SPECIFICATION**

TITLE DL11 INSTALLATION PROCEDURE

**C. VECTOR ADDRESS ASSIGNMENT:**

Jumpers V8 through V3 control the interrupt vector. A jumper inserted provides a vector bit of one. Vectors can be produced in the form XX0 and XX4 where XX ranges from 00 to 77.

For the DL11-A and B used as a console device the vector address is 060/064. For additional units vectors are floating.

For the DL11-C,D, and E vector addresses are floating. Assign all C's first, then D's, then E's.

**D. PRIORITY ASSIGNMENT:**

Interrupt priority is established by inserting a "priority plug" in the socket at IC location E19. For DL11-A,B,C,D and E use level 4, for the standard assignment or level 5-7 as specified by the customer or the documentation of an option which uses the DL11.

SUMMARY OF REGISTER, VECTOR AND PRIORITY ASSIGNMENTS:

ADDRESS VECTOR PRIORITY

DL11-A,B CONSOLE 777560 60/64 BR4  
777562  
777564  
777566

DL11-A,B ADDITIONAL UNITS 776XX0 FLOATING BR4  
776XX2  
776XX4  
776XX6

Where XX= 50 for line #1 and XX= 67 for line #16

ADDRESS VECTOR PRIORITY

DL11-C,D,E 77XXX0 Floating 4  
77XXX2  
77XXX4  
77XXX6

Where XXX= 561 for line #1 and XXX= 617 for line #31

DEC FORM NO 16-1081-1022-0370  
DRA 108

SIZE CODE A SP  
NUMBER DL11-0-2  
REV F

SHEET 4 OF 9

## ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

### E. SPECIAL MPR JUMPER:

Jumper M1, shown on drawing DL-6, controls the response of the interrupt circuit to an MPR request. The jumper should normally be IN, except for 11/2B and 11/15 systems without the RMI1 option.

### F. SELECTION OF DATA FORMAT:

- Data Bits  
Split lug pairs NB2 and NB1 control the number of data bits in the serial character as follows:

NB2	NB1	# OF DATA BITS
OUT	OUT	8
OUT	IN	7
IN	OUT	6
IN	IN	5

### 2. Parity:

Parity is controlled by split lug pairs MP and EPS as follows:

MP	EPS	PARITY
OUT	OUT	OFF
OUT	IN	OFF
IN	OUT	EVEN
IN	IN	ODD

### 3. Stop Bits

Split lug pair 25B and Jumpers J9, J10 and J11 control the number of stop bits in the serial character as follows:

25B	J9	J10	J11	# OF STOP BITS
OUT	OUT	IN	OUT	2
IN	OUT	IN	OUT	1
IN	OUT	OUT	IN	1.5 for TI, GI, and SCM UARTS
IN	IN	OUT	OUT	1.5 for WD UARTS

### G. CRYSTAL SELECTION:

The clocking scheme of the DL11 consists of a single crystal oscillator feeding a divider network, with two 10-position switches tapping various points to feed into the UART's

DEC FORM NO DEC 16-1981) 1022-N370  
DRA 108

SIZE CODE A SP NUMBER DL11-0-2 REV F

SHEET 5 OF 9

## ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

### 6. Con't

transmitter and receiver sections. Thus, for a given crystal frequency, 8 baud rates are independently selectable for transmit and receive. The two addition switch positions select external clocks.

POSITION	CRYSTAL (KHZ)			
	1	2	3	4
1*	23040	36.7	44.8	50
2	15360	55	67.3	75
3	7680	110	134.5	150
4	3840	220	269	300
5	1920	440	538	600
6	960	880	1076	1200
7	640	1320	1614	1800
8	480	1760	2152	2400

\*Most counter-clock wise position.

To determine a crystal frequency for a non-standard baud rate, pick the position of the closest baud rate in the 1.152MHz column, and then multiply the non-standard baud rate by the factor for that position. For example, if the customer specifies 1050 baud, this is closest to 1200 baud, position 6.

$$1050 \times 960 = 10080000 = 1.008\text{MHZ.}$$

The crystal frequency should not fall outside the range of the standard crystals. Although the above table includes only the standard DL11 crystals other values may be specified by the customer or by other documentation of an option which uses the DL11.

DPC part number for the standard crystals are as follows:

844.8 KHZ	18-10245-1*
1.03296 MHz	18-05501-6
1.152 MHz	18-05501-5
4.608 MHz	18-05501-7

\*Use A or C cut crystals only. Do not use crystals marked NE-60.

When ordering a special crystal, refer to purchase specification 18-05501 for crystal specification.

Insure that transparent vinyl tape (9008269) is applied to the top surfaces of the crystal and mounting brackets to insulate from adjacent modules.

DEC FORM NO DEC 16-1981) 1022-N370  
DRA 108

SIZE CODE A SP NUMBER DL11-0-2 REV F

SHEET 5 OF 9

## ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

### A. 68000 INSTALLATION:

For DL11-B, D, and E a positive voltage is required between 9 and 15 volts to operate the CIA drivers. For PDP-11/20 and PDP-11/15 systems with the M720 power supply, a 68000 module must be installed to provide this voltage. Using a filter network, this module converts the full-wave rectified +8V signal to a positive DC voltage.

- Install 68000 into slot A92 of DD11-A.
- Wire AP3V2 to AB272.
- Wire AP2N2 to C1XU1 where XX is the slot location of the M7800.

Refer to diagram 1.

### I. FILTER CAPACITOR SELECTION:

For DL11-A's and DL11-C's, which operate with 20ma current loops, capacitors are used to filter the receive line and slow the switching time of the transmit line. To avoid excessive distortion above 150 baud, the capacitance in each of these two circuits must be reduced. This is accomplished by clipping C29 (.47 mfd) and C31 (1000 pf), both shown on drawing DL-3.

- DL11-B,D,E in Systems with +15V available using DD11-A There is a special situation of using a DD11-A to mount a DL11-B, D, or E in systems with +15V available. These systems have +15V available and it appears at pin A03V2 of the DD11-A when using power harness such as 7009177, 7008855, or 7008909. In this situation, no 68000 is necessary, and +15V can be wired directly from A03V2 to CXXU1, where XX is the slot number of the DL11.  
NOTE: this does not apply to DL11-A or C or DD11-B.

- When using the DL11-B,D,E in an 11/05 processor pin CXXU1 has +15V available on it so no 68000 or no jumpers are required.

DEC FORM NO DEC 16-1981) 1022-N370  
DRA 108

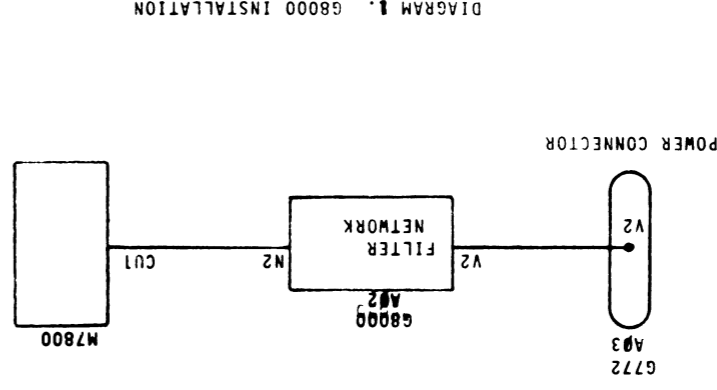
SIZE CODE A SP NUMBER DL11-0-2 REV F

SHEET 7 OF 9

## ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE



DEC FORM NO DEC 16-1981) 1022-N370  
DRA 108

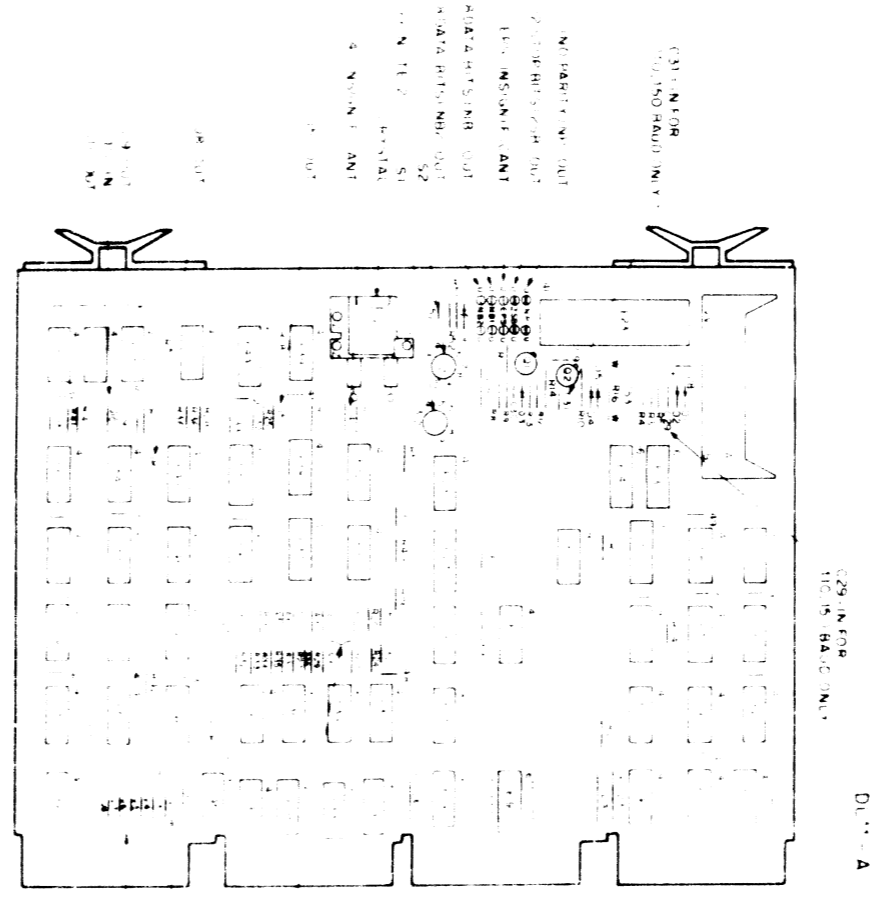
SIZE CODE A SP NUMBER DL11-0-2 REV F

SHEET 8 OF 9

**ENGINEERING SPECIFICATION**

CONTINUATION SHEET

TITLE DEPT. INSTALLATION PROCEDURE



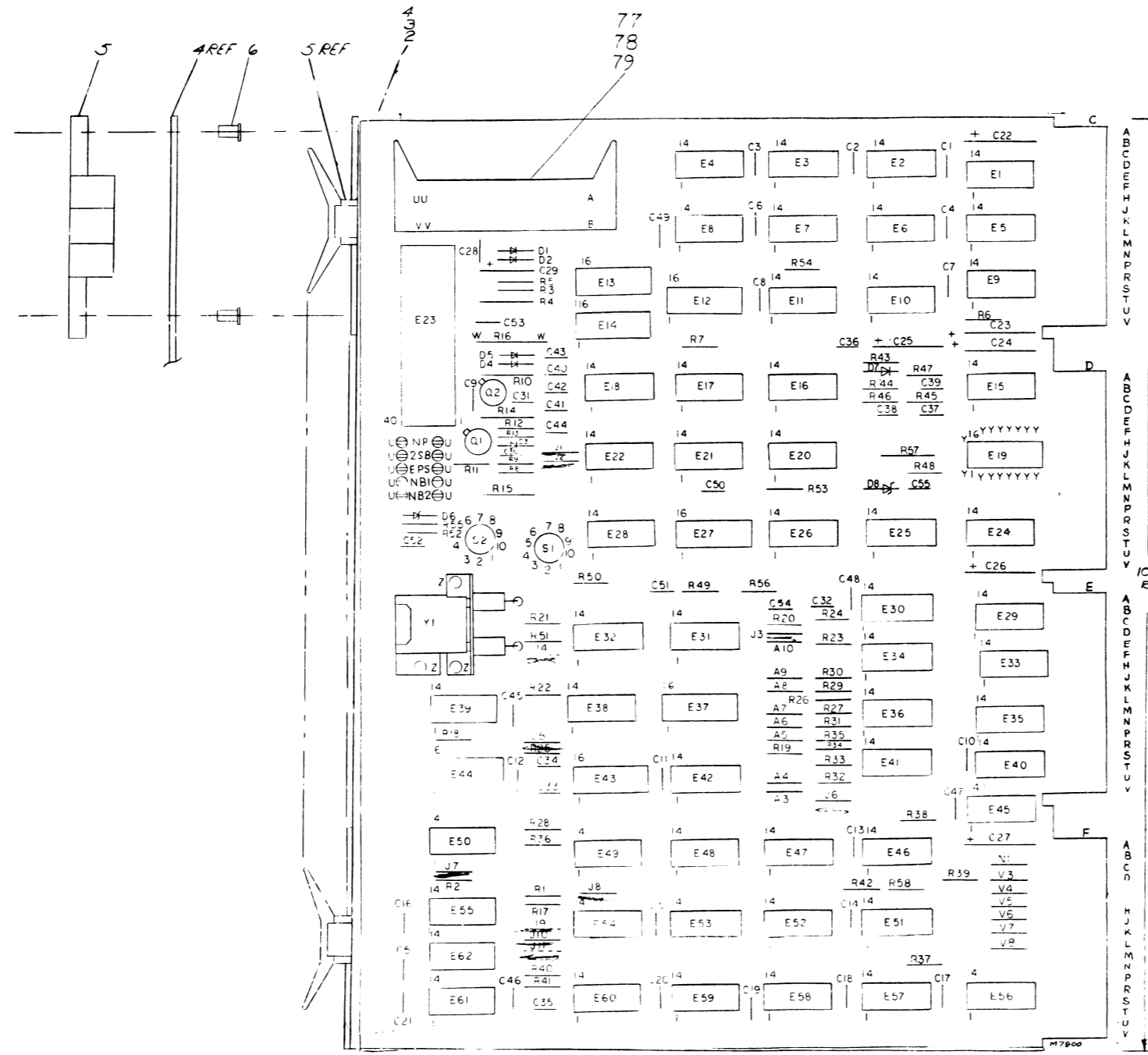
SIZE	CODE	NUMBER	REV
A	SP	DL11-2	F

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NOTES:  
 1. PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE SYSTEM UNIT. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE LEFT.  
 2. JUMPERS TO BE USED AT CONNECTIONS A3-A10, J1-J10, V3-V8, AND N1.  
 3. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X).

PIN NOMENCLATURE  
 MODULE SYSTEM UNIT

4. DEC B6401 WERE PHASED IN AS DEC 380 REPLACEMENTS ANY 380 FAILURES SHOULD BE REPLACED BY B640'S EXCEPT E28, E28 MUST BE REPLACED WITH A 7380.  
 5. FOR YC VERSION, C36 VALUE IS 1200PF.



QTY	REF DESIGNATION	DESCRIPTION	PART NO.	REV
1	128	LATCH NIGHT	1209941-04	79
1	1	LATCH LEFT	209941-03	78
1	1	CONNECTOR BERG	1209941-02	77
1	1	INSULATED JUMPER	9009185	76
1	1	WIRE 22 GAUGE	100214	75
1	1	WIRE 22 GAUGE	100214	74
1	1	RES 39 1/2W 5% 20	1302336	73
1	1	DIODE 4742 12V 10% 1V 1/2W	1101502	72
3	3	INT. WASHER #2	3006631	71
1	1	IC 7410	1910650	70
1	1	IC 7410	1910650	69
1	1	SCREEN PAN HD 25X25X1/8	3006635	68
1	1	ALUM. FPC 25X25X1/8	1202812	67
1	1	DIODE 100V 500MA	1100114	66
1	1	TRIPLE 1746A	1104860	65
1	1	TRANSISTOR 2N34D	1503409-00	64
1	1	CAP 100PF 100V 50% 500V	1000016	63
1	1	CAP 500PF 100V 50% 500V	1000025	62
1	1	CAP 0.47M CERAMIC	1009673	61
1	1	CAP 0.01M CERAMIC	1000021	60
1	1	CAP 200PF 100V 5% 500V	1000023	59
1	1	CAP 300PF 100V 5% 500V	1000029	58
1	1	CAP 300PF 100V 5% 500V	1000029	57
1	1	CAP 100PF 100V 5% 500V	1000002	56
30	30	CAP 100V 500PF 50% 500V	1000000-U1	55
1	1	CAP 100V 500PF 50% 500V	1000000	54
1	1	CAP 100V 500PF 50% 500V	1000000	53
1	1	CAP 100V 500PF 50% 500V	1000000	52
1	1	CAP 100V 500PF 50% 500V	1000000	51
1	1	CAP 100V 500PF 50% 500V	1000000	50
1	1	CAP 100V 500PF 50% 500V	1000000	49
1	1	CAP 100V 500PF 50% 500V	1000000	48
1	1	CAP 100V 500PF 50% 500V	1000000	47
1	1	CAP 100V 500PF 50% 500V	1000000	46
1	1	CAP 100V 500PF 50% 500V	1000000	45
1	1	CAP 100V 500PF 50% 500V	1000000	44
1	1	CAP 100V 500PF 50% 500V	1000000	43
1	1	CAP 100V 500PF 50% 500V	1000000	42
1	1	CAP 100V 500PF 50% 500V	1000000	41
1	1	CAP 100V 500PF 50% 500V	1000000	40
1	1	CAP 100V 500PF 50% 500V	1000000	39
1	1	CAP 100V 500PF 50% 500V	1000000	38
1	1	CAP 100V 500PF 50% 500V	1000000	37
1	1	CAP 100V 500PF 50% 500V	1000000	36
1	1	CAP 100V 500PF 50% 500V	1000000	35
1	1	CAP 100V 500PF 50% 500V	1000000	34
1	1	CAP 100V 500PF 50% 500V	1000000	33
1	1	CAP 100V 500PF 50% 500V	1000000	32
1	1	CAP 100V 500PF 50% 500V	1000000	31
1	1	CAP 100V 500PF 50% 500V	1000000	30
1	1	CAP 100V 500PF 50% 500V	1000000	29
1	1	CAP 100V 500PF 50% 500V	1000000	28
1	1	CAP 100V 500PF 50% 500V	1000000	27
1	1	CAP 100V 500PF 50% 500V	1000000	26
1	1	CAP 100V 500PF 50% 500V	1000000	25
1	1	CAP 100V 500PF 50% 500V	1000000	24
1	1	CAP 100V 500PF 50% 500V	1000000	23
1	1	CAP 100V 500PF 50% 500V	1000000	22
1	1	CAP 100V 500PF 50% 500V	1000000	21
1	1	CAP 100V 500PF 50% 500V	1000000	20
1	1	CAP 100V 500PF 50% 500V	1000000	19
1	1	CAP 100V 500PF 50% 500V	1000000	18
1	1	CAP 100V 500PF 50% 500V	1000000	17
1	1	CAP 100V 500PF 50% 500V	1000000	16
1	1	CAP 100V 500PF 50% 500V	1000000	15
1	1	CAP 100V 500PF 50% 500V	1000000	14
1	1	CAP 100V 500PF 50% 500V	1000000	13
1	1	CAP 100V 500PF 50% 500V	1000000	12
1	1	CAP 100V 500PF 50% 500V	1000000	11
1	1	CAP 100V 500PF 50% 500V	1000000	10
1	1	CAP 100V 500PF 50% 500V	1000000	9
1	1	CAP 100V 500PF 50% 500V	1000000	8
1	1	CAP 100V 500PF 50% 500V	1000000	7
1	1	CAP 100V 500PF 50% 500V	1000000	6
1	1	CAP 100V 500PF 50% 500V	1000000	5
1	1	CAP 100V 500PF 50% 500V	1000000	4
1	1	CAP 100V 500PF 50% 500V	1000000	3
1	1	CAP 100V 500PF 50% 500V	1000000	2
1	1	CAP 100V 500PF 50% 500V	1000000	1

DEC NO.	EIA NO.	DEC NO.	EIA NO.
DEC 74161	8	16	-
DEC 1488	7	-	4
DEC UART	3	1	2
DEC 74175	8	16	-
DEC 8271	8	16	-
DEC 74142	8	16	-
DEC 314	1	8	-
DEC 7493	10	5	-
DEC 7492	10	5	-
DEC 74153	8	16	-
DEC 8640	1	8	-
DEC 7490	10	5	-
DEC 74123	8	16	-

IC PIN LOCATIONS  
 GND +5V +V -12V  
 GND AND BY ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE.

REV	DATE	BY	CHKD	APP'D	DESCRIPTION
1	7-27-74	J. JANSON			REVISED
2	8-23-74	J. JANSON			REVISED
3	8-23-74	J. JANSON			REVISED
4	8-23-74	J. JANSON			REVISED
5	8-23-74	J. JANSON			REVISED
6	8-23-74	J. JANSON			REVISED
7	8-23-74	J. JANSON			REVISED
8	8-23-74	J. JANSON			REVISED
9	8-23-74	J. JANSON			REVISED
10	8-23-74	J. JANSON			REVISED

ETCH BOARD REV	H	DATE	BY	CHKD	APP'D	DESCRIPTION
1		7-27-74	J. JANSON			REVISED
2		8-23-74	J. JANSON			REVISED
3		8-23-74	J. JANSON			REVISED
4		8-23-74	J. JANSON			REVISED
5		8-23-74	J. JANSON			REVISED
6		8-23-74	J. JANSON			REVISED
7		8-23-74	J. JANSON			REVISED
8		8-23-74	J. JANSON			REVISED
9		8-23-74	J. JANSON			REVISED
10		8-23-74	J. JANSON			REVISED

EQUIPMENT CORPORATION  
 TITLE: ASYNCHRONOUS LINE INTERFACE  
 SEMICONDUCTOR CONVERSION CHART  
 DEC NO. EIA NO. DEC NO. EIA NO.  
 66340 MPS6539  
 IN746A 11AM33A  
 0668 1N3606

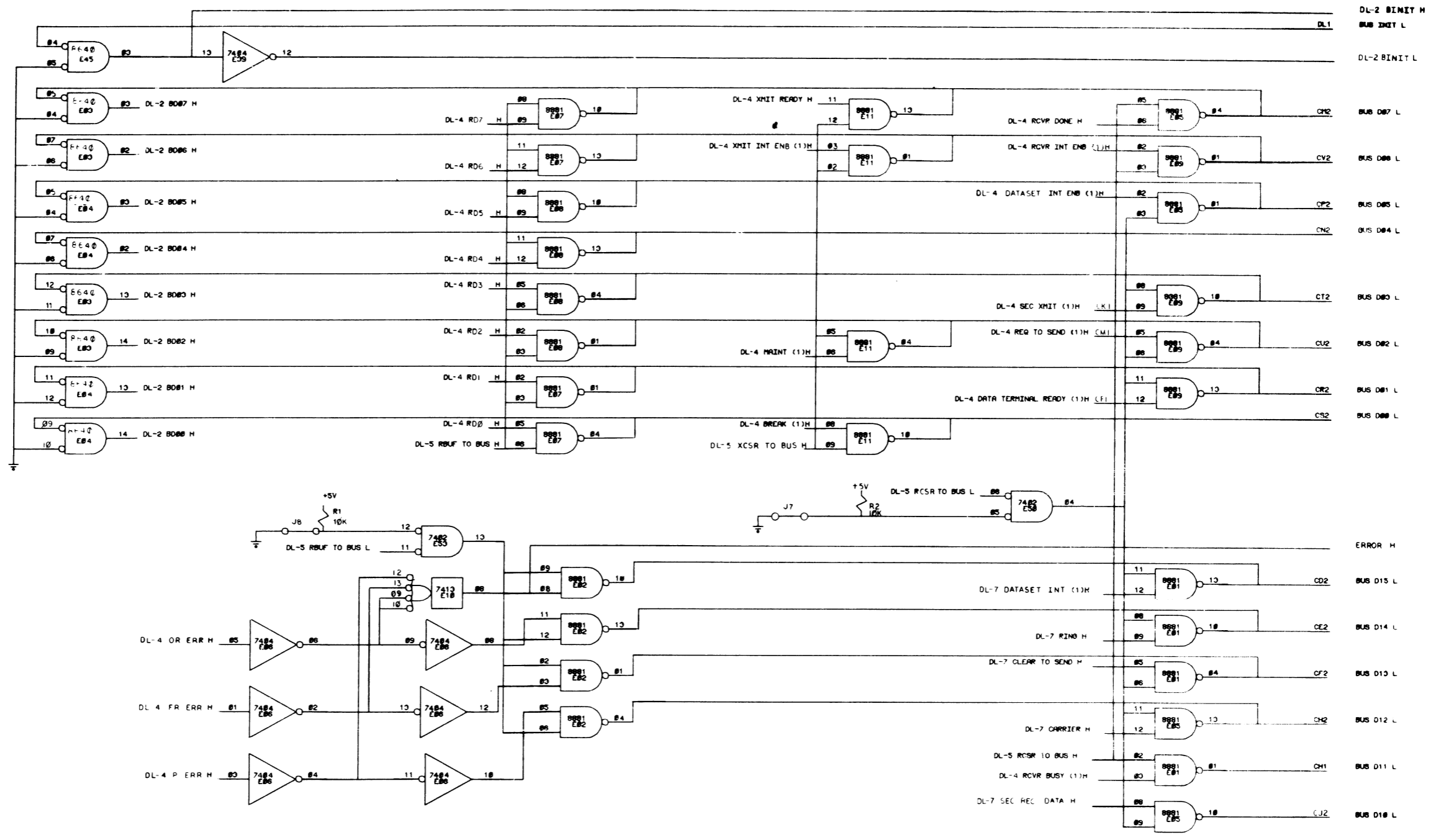
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D

C

B

A



REVISIONS		
REV.	DATE	BY

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.
DL11			
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES			
DECIMALS	ANGLES	PARTS LIST	
.XXX - .000	± 0° 30'	EQUIPMENT CORPORATION	
.XX - .00		TITLE ASYNCHRONOUS LINE INTERFACE (BUS RECEIVERS & DRIVERS) DL-2	
.X - .1		CORNER SURFACE QUALITY	
MATERIAL	NEXT HIGHER ASSY.	REV.	
FINISH	SCALE	D CS M7800-0-1 P	

8

7

6

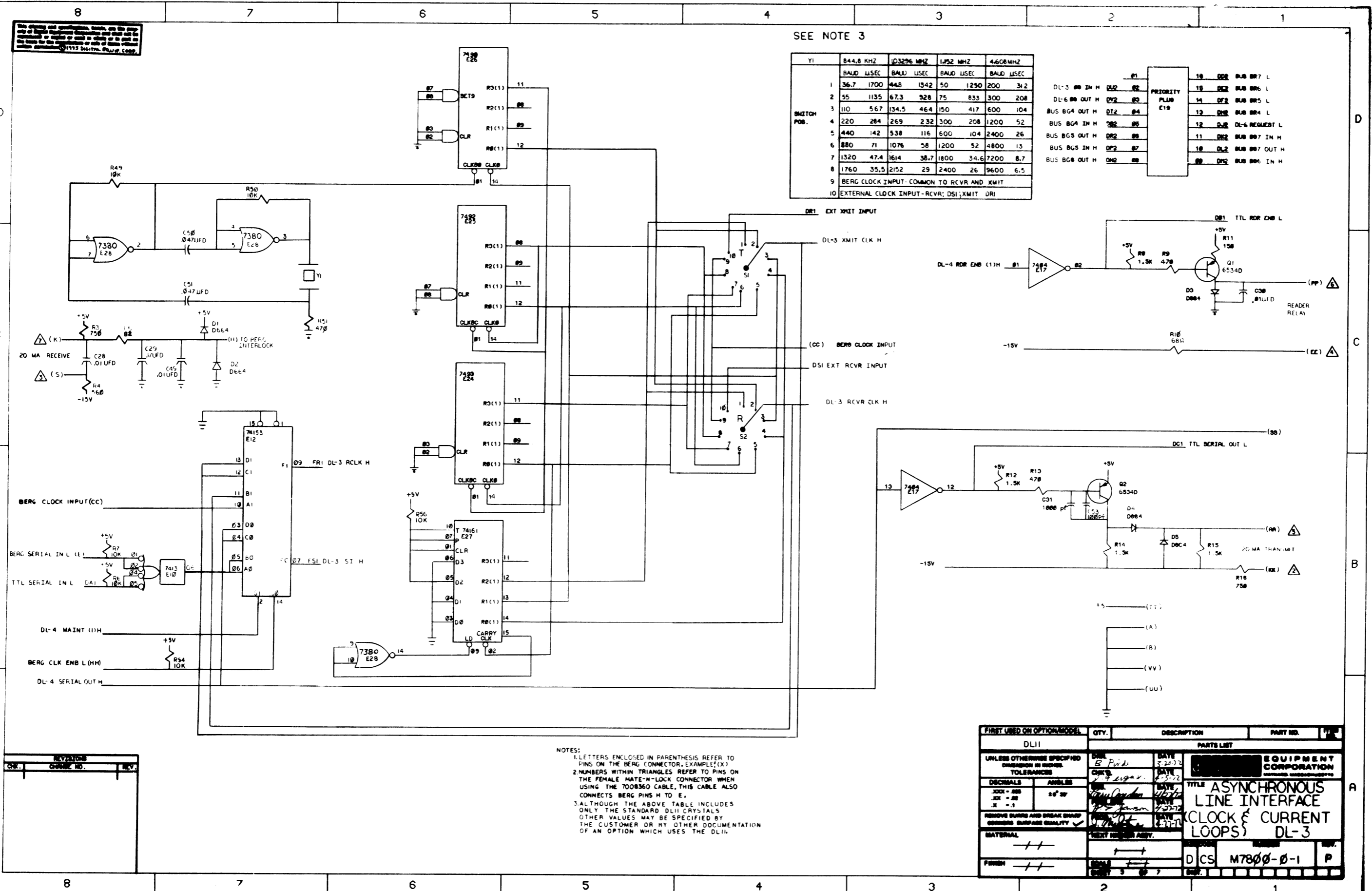
5

4

3

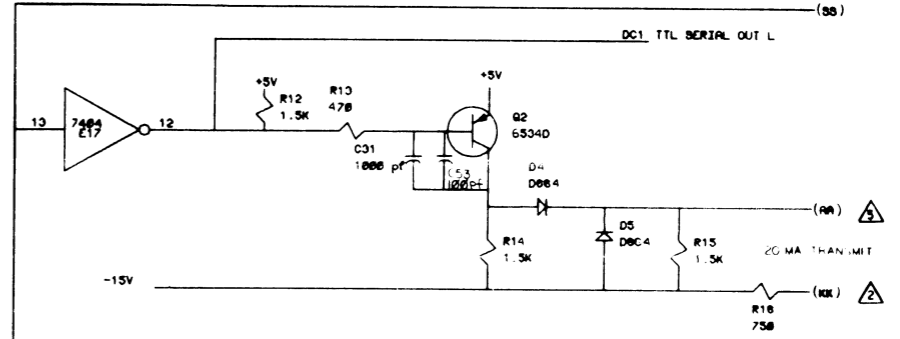
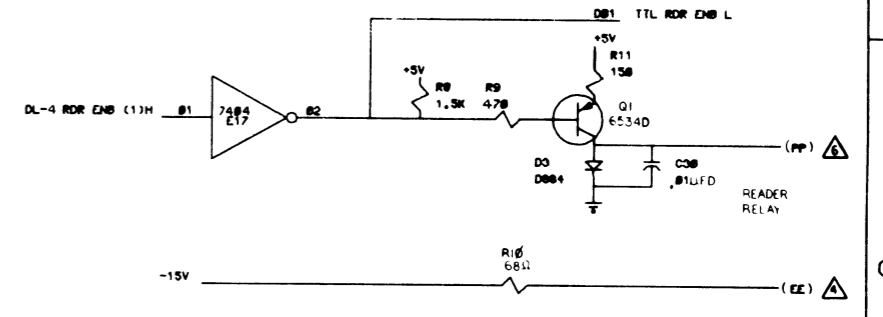
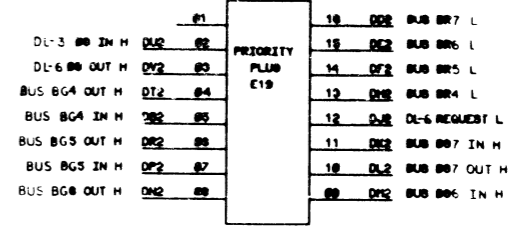
2

1



SEE NOTE 3

Y1	844.8 KHZ	103296 MHZ	1.952 MHZ	4.608MHZ
	BAUD USEC	BAUD USEC	BAUD USEC	BAUD USEC
1	36.7 1700	44.8 1342	50 1250	200 312
2	55 1135	67.3 928	75 833	300 208
3	110 567	134.5 464	150 417	600 104
4	220 284	269 232	300 208	1200 52
5	440 142	538 116	600 104	2400 26
6	880 71	1076 58	1200 52	4800 13
7	1320 47.4	1614 38.7	1800 34.6	7200 8.7
8	1760 35.5	2152 29	2400 26	9600 6.5
9	BERG CLOCK INPUT-COMMON TO RCVR AND XMIT			
10	EXTERNAL CLOCK INPUT-RCVR; DSI; XMIT DRI			



NOTES:  
1. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X)  
2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOCK CONNECTOR WHEN USING THE 7008360 CABLE. THIS CABLE ALSO CONNECTS BERG PINS H TO E.  
3. ALTHOUGH THE ABOVE TABLE INCLUDES ONLY THE STANDARD DLII CRYSTALS OTHER VALUES MAY BE SPECIFIED BY THE CUSTOMER OR BY OTHER DOCUMENTATION OF AN OPTION WHICH USES THE DLII.

REV.	DATE	BY

FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.
DLII			
UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES			
TOLERANCES			
DECIMALS			
ANGLES			
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY			
MATERIAL			
FINISH			

PARTS LIST

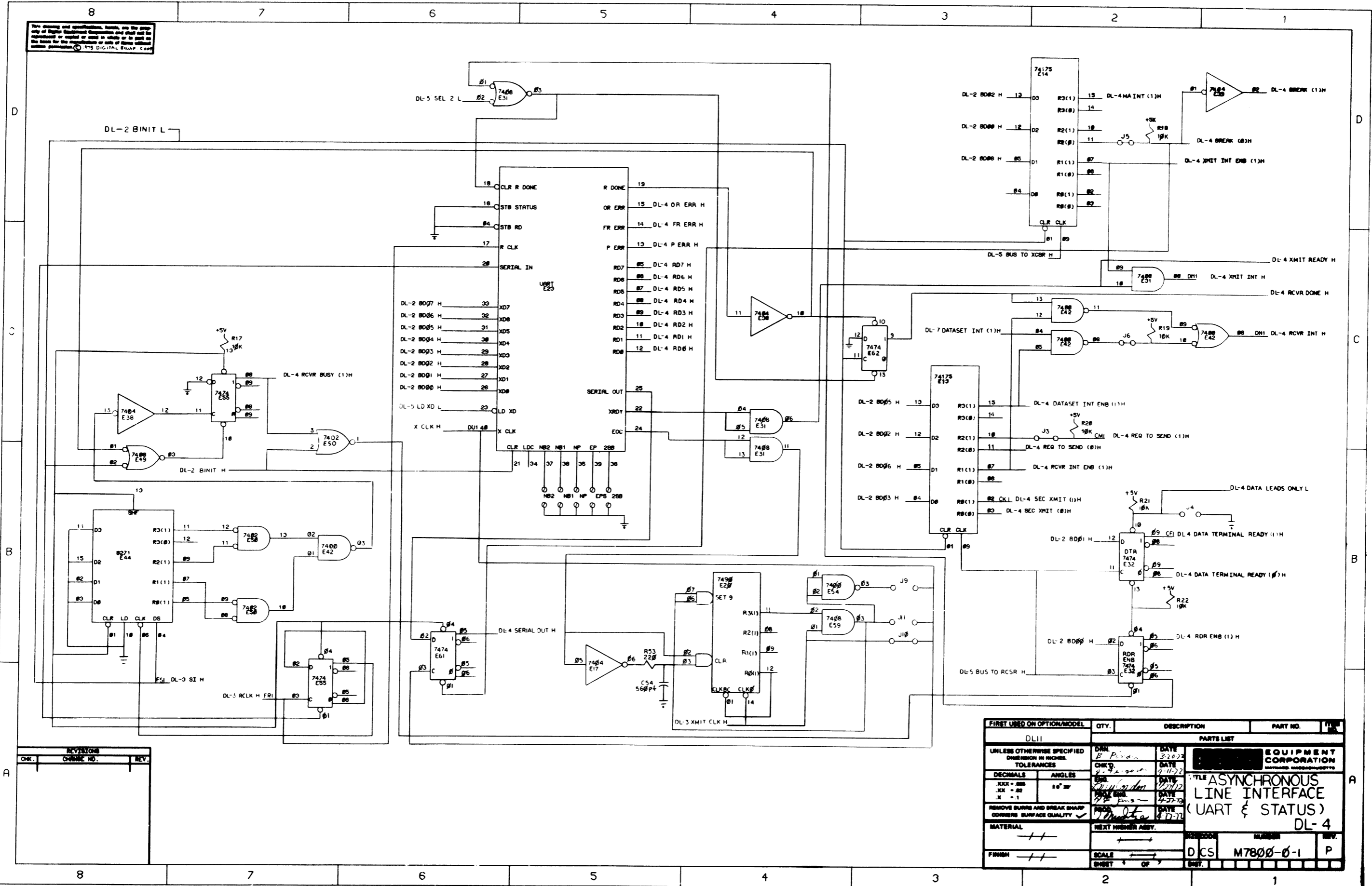
EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE CLOCK & CURRENT LOOPS DL-3

D CS M7800-0-1 P



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REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	REV.
DL11				

UNLESS OTHERWISE SPECIFIED		PARTS LIST	
DIMENSION IN INCHES	DATE	EQUIPMENT CORPORATION	
TOLERANCES	DATE	MILWAUKEE, WISCONSIN 53190	
DECIMALS	DATE	TITLE ASYNCHRONOUS LINE INTERFACE (UART & STATUS) DL-4	
ANGLES	DATE	DRAWN BY P. P. ...	
.XXX - .008	DATE	CHECKED BY ...	
.XX - .02	DATE	DATE 12/12/72	
.X - .1	DATE	DATE 4-27-73	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY	DATE	DATE 12/12/72	
MATERIAL	NEXT HIGHER ASSY.	SCALE	DCS
FINISH	SCALE	SHEET	M7800-0-1

