terminals and communications handbook
DIGITAL EQUIPMENT CORPORATION, Corporate Headquarters: Maynard, Massachusetts 01754, Telephone (617) 897-5111—SALES AND SERVICE OFFICES: UNITED STATES—ALABAMA, Birmingham and Huntsville • ARIZONA, Phoenix and Tucson • CALIFORNIA, Los Angeles, Oakland, Sacramento, San Diego, San Francisco, Santa Ana, Santa Barbara, Santa Clara, Sunnyvale • COLORADO, Denver • CONNECTICUT, Fairfield and Meriden • DISTRICT OF COLUMBIA, Washington, D.C. (Lanham, MD) • FLORIDA, Miami, Orlando, Tampa • GEORGIA, Atlanta • HAWAI, Honolulu • ILLINOIS, Chicago, Peoria, Rolling Meadows • INDIANA, Indianapolis • IOWA, Bettendorf • KENTUCKY, Louisville • LOUISIANA, New Orleans • MASSACHUSETTS, Springfield and Waltham • MICHIGAN, Detroit • MINNESOTA, Minneapolis • MISSOURI, Kansas City and St. Louis • NEBRASKA, Omaha • NEW HAMPSHIRE, Manchester • NEW JERSEY, Cherry Hill, Fairfield, Princeton, Somerset • NEW MEXICO, Albuquerque • NEW YORK, Albany, Buffalo, Long Island, Manhattan, Rochester, Syracuse • NORTH CAROLINA, Charlotte and Durham/Chapel Hill • OHIO, Cincinnati, Cleveland, Columbus, Dayton • OKLAHOMA, Tulsa • OREGON, Portland • PENNSYLVANIA, Harrisburg, Philadelphia (Blue Bell), Pittsburgh • RHODE ISLAND, Providence • SOUTH CAROLINA, Columbia • TENNESSEE, Knoxville and Nashville • TEXAS, Austin, Dallas, El Paso, Houston • UTAH, Salt Lake City • VIRGINIA, Richmond • WASHINGTON, Seattle • WEST VIRGINIA, Charleston • WISCONSIN, Milwaukee • INTERNATIONAL—ARGENTINA, Buenos Aires • AUSTRALIA, Adelaide, Brisbane, Canberra, Melbourne, Perth, Sydney • AUSTRIA, Vienna • BELGIUM, Brussels • BOLIVIA, La Paz • BRAZIL, Rio de Janeiro and Sao Paulo • CANADA, Calgary, Edmonton, Halifax, London, Montreal, Ottawa, Toronto, Vancouver, Winnipeg • CHILE, Santiago • DENMARK, Copenhagen • EGYPT (A.R.E.), Cairo • FINLAND, Espoo • FRANCE, Lyon, Paris, Puteaux • HONG KONG • INDIA, Bombay • INDONESIA, Djakarta • IRAN, Tehran • IRELAND, Dublin • ISRAEL, Tel Aviv • ITALY, Milan, Rome, Turin • JAPAN, Osaka and Tokyo • MALAYSIA, Kuala Lumpur • MEXICO, Mexico City • NETHERLANDS, Amstelveen, Rijswijk, Utrecht • NEW ZEALAND, Auckland and Christchurch • NORTHERN IRELAND, Belfast • NORWAY, Oslo • PUERTO RICO, San Juan • SINGAPORE • SOUTH KOREA, Seoul • SPAIN, Madrid • SWEDEN, Gothenburg and Stockholm • SWITZERLAND, Geneva and Zurich • TAIWAN, Taipei • UNITED KINGDOM, Birmingham, Bristol, Ealing, Epson, Edinburgh, Leeds, Leicester, London, Manchester, Reading • VENEZUELA, Caracas • WEST GERMANY, Berlin, Cologne, Frankfurt, Hamburg, Hannover, Munich, Nurnberg, Stuttgart • YUGOSLAVIA, Belgrade and Ljubljana •
digital terminals and communications handbook

digital equipment corporation
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INTRODUCTION

1.1 SCOPE AND CONTENTS
This handbook is a reference guide to the terminals and communications equipment available for the PDP-11 family of computers. It includes descriptions, specifications, programming and interfacing information. This work also serves as a supplement to the various PDP-11 Processor Handbooks.

It is the intent of this handbook to provide the reader with extensive information on the operation of PDP-11 terminals and communications equipment. It is not intended to be the sole reference for such information. More comprehensive and detailed information can be obtained from the Maintenance and Programming manuals for each of the peripherals.

1.2 TERMINALS
A variety of terminals are available for the PDP-11 family of computers. These terminals range from simple data entry devices, to sophisticated "intelligent" terminals for use in complex data processing systems.

1.2.1 Characteristics and Applications
a) convenient human interface to the computer
b) typewriter-like keyboard for data entry
c) printer or display for output from computer
d) basic input/output device
e) can be local (console terminal), or remote

Products

<table>
<thead>
<tr>
<th>MODEL</th>
<th>DESCRIPTION</th>
<th>OUTPUT SPEED (max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LA35</td>
<td>DECr writes II</td>
<td>30 characters/sec</td>
</tr>
<tr>
<td>LA36</td>
<td>DECr writes II</td>
<td>30 characters/sec</td>
</tr>
<tr>
<td>LA180</td>
<td>DECr printer I</td>
<td>180 characters/sec</td>
</tr>
<tr>
<td>VT52</td>
<td>Video display</td>
<td>960 characters/sec</td>
</tr>
<tr>
<td>VT55</td>
<td>DECr scope</td>
<td>960 characters/sec</td>
</tr>
</tbody>
</table>

1.3 COMMUNICATIONS OPTIONS
In addition to the wide range of terminals available for the PDP-11 family of computers, there is an equally varied selection of communications interfaces. These interfaces cover applications from single local terminals to multiple remote lines. Provisions can be made for auto-dial options and telegraph connections.
1.3.1 Characteristics and Applications

**Asynchronous Interfaces**—Character transmission time is variable, but bits within the character are timed; a character transmission normally includes a start bit, several data bits, one or more stop bits, and an optional parity bit.

**Synchronous Interfaces**—Continuous data stream once the receiver is synchronized; data is generally transmitted in message blocks containing both information and timing signals.

**Other Communications Options**—Provide error detection, auto-calling unit interfacing, signal conditioning, and communication line switching.

### Products

<table>
<thead>
<tr>
<th>MODEL</th>
<th>DESCRIPTION</th>
<th>TYPICAL USE</th>
</tr>
</thead>
<tbody>
<tr>
<td>DL11</td>
<td>Single Asynchronous Line Interface</td>
<td>Connects PDP-11 to local terminals or to remote terminals via modems.</td>
</tr>
<tr>
<td>DH11</td>
<td>16-Line Programmable Asynchronous Multiplexer</td>
<td>Connects PDP-11 to up to 16 local terminals or remote terminals. Transmission speeds and parameters are programmable.</td>
</tr>
<tr>
<td>DZ11</td>
<td>8 and 16-line Asynchronous Multiplexer</td>
<td>Connects PDP-11 to up to 16 local or remote terminals economically. Transmission speeds and formats are programmable.</td>
</tr>
<tr>
<td>DU11</td>
<td>Single Line Synchronous Interface</td>
<td>Connects PDP-11 to modems for medium speed (up to 9600 baud) synchronous transmission.</td>
</tr>
<tr>
<td>DUP11</td>
<td>Single Line Synchronous Interface</td>
<td>Connects PDP-11 to modems for bit or byte oriented operation.</td>
</tr>
<tr>
<td>DUV11</td>
<td>Single Line Synchronous Interface</td>
<td>Connects LSI-11 processor to modems or lines.</td>
</tr>
<tr>
<td>DQ11</td>
<td>Single Line Synchronous Interface</td>
<td>Used for high throughput synchronous transmission.</td>
</tr>
<tr>
<td>DMC11</td>
<td>Network Link</td>
<td>Interconnects computers, local or remote, over serial synchronous link.</td>
</tr>
<tr>
<td>DV11</td>
<td>Communications Preprocessor</td>
<td>Relieves PDP-11 overhead when connected to up to 16 synchronous and/or asynchronous lines.</td>
</tr>
<tr>
<td>DN11</td>
<td>Auto Calling Unit Interface</td>
<td>Interfaces PDP-11 to Bell 801 auto calling units.</td>
</tr>
<tr>
<td>DF01</td>
<td>Acoustic Coupler</td>
<td>Connects terminal to standard telephone for communication with computer via phone lines.</td>
</tr>
<tr>
<td>Model</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>-----------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>H312-A</td>
<td>Null Modem</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Allows direct connection of EIA interfaces.</td>
<td></td>
</tr>
<tr>
<td>KG11</td>
<td>Communication Arithmetic Element</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Used to detect errors in serially transmitted data.</td>
<td></td>
</tr>
<tr>
<td>CS11-M</td>
<td>Manual Communications Line Switch Options</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Provides facilities for switching communication lines from one set of</td>
<td></td>
</tr>
<tr>
<td></td>
<td>communication interfaces to another.</td>
<td></td>
</tr>
<tr>
<td>IMP11-A</td>
<td>Host to IMP Full-duplex NPR Interface</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Provides a direct connection between PDP-11 and the Interface Message</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Processor (IMP) used to connect Host Computers to the Advanced Research</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Projects Agency (ARPA) network.</td>
<td></td>
</tr>
</tbody>
</table>

1.4 PDP-11 EQUIPMENT PHILOSOPHY

The PDP-11 family is a comprehensive set of hardware/software facilities that includes various central processors, a large number of peripheral devices and options, and extensive software. Products are compatible with each other. Thus, the user can choose the system which is most suitable to present applications and be sure that as needs change or grow, equipment can easily be changed or added. Some of the characteristics of PDP-11 equipment are:

- 16-bit word (two 8-bit bytes)
  - direct addressing of 32K 16-bit words or 64K 8-bit bytes \( K = 1024 \)
- Word or byte processing
  - central processors are hardwired for word or byte instructions
- Asynchronous operation
  - systems run at their highest possible speed, replacement with faster devices means faster operation with no other hardware or software changes
- Modular component design
  - extreme ease and flexibility in configuring systems
- Direct Memory Access (DMA)
  - inherent in the architecture is direct memory access for multiple devices
- Automatic Priority Interrupt
  - four-line, multi-level system permits grouping of interrupt lines according to response requirements
- Vectored interrupts
  - fast interrupt response without device polling
- Power Fail & Automatic Restart
  - hardware detection and software protection for fluctuations in the AC power

1-3
1.5 CENTRAL PROCESSOR
The central processor, connected to the UNIBUS as a subsystem, controls the time allocation of the UNIBUS for peripherals and performs arithmetic and logic operations and instruction decoding. It contains multiple high-speed general-purpose registers which can be used as accumulators, address pointers, index registers, and other specialized functions. The processor can perform data transfers directly between input/output (I/O) devices and memory without disturbing the processor registers; does both single- and double-operand addressing and handles both 16-bit word and 8-bit byte data.

Instruction Set
The instruction complement uses the flexibility of the general-purpose registers to provide over 400 powerful hard-wired instructions. Unlike conventional 16-bit computers, which usually have three classes of instructions (memory reference instructions, operate or control instructions and I/O instructions) all operations in the PDP-11 are accomplished with one set of instructions. Since peripheral device registers can be manipulated as flexibly as core memory by the central processor, instructions that are used to manipulate data in core memory may be used equally well for data in peripheral device registers.

1.6 UNIBUS
Most computer system components and peripherals connect to and communicate with each other on a high-speed bus known as the UNIBUS, see Figure 1-1.

![Figure 1-1 PDP-11 System Block Diagram](image_url)

The form of communication is the same for every device on the UNIBUS. The central processing unit (CPU) uses the same set of signals to communicate with main memory as with peripheral devices. Peripheral devices also use this set of signals when communicating with the processor, memory or other peripheral devices. Each device, including memory locations, processor registers, and peripheral device registers, is assigned an address on the UNIBUS.

With bidirectional and asynchronous communications on the UNIBUS, devices can send, receive, and exchange data with minimum processor intervention. Because it is asynchronous, the UNIBUS is compatible with devices operating over a wide range of speeds. Interfaces to the UNIBUS are not time dependent; there are no pulse-width or rise-time restrictions.
Full 16-bit words or 8-bit bytes of information can be transferred on the bus. The information can be instructions, addresses, or data. Direct data transfers can occur between a peripheral device control and memory.

Refer to Chapter 5 for more detailed information about the UNIBUS and data transfers.

1.7 PDP-11 WORD

The 16-bit PDP-11 word can be represented conveniently as a 6-digit octal word. Bit 15, the Most Significant Bit (MSB), is used directly as the Most Significant Digit of the octal word. The other 5 octal digits are formed from the corresponding groups of 3 bits in the binary word. See Figure 1-2.

**Octal Representation**

![](image)

When an extended address of 18 bits is used (shown later in the Handbook), the Most Significant Digit of the octal word is formed from bits 17, 16, and 15. For unsigned numbers, the correspondence between decimal and octal is:

<table>
<thead>
<tr>
<th>Decimal</th>
<th>Octal</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>000 000</td>
</tr>
<tr>
<td>(2^{16} - 1) = 65,535</td>
<td>177 777 (16-bit limit)</td>
</tr>
<tr>
<td>(2^{18} - 1) = 262,143</td>
<td>777 777 (18-bit limit)</td>
</tr>
</tbody>
</table>
CHAPTER 2

DESCRIPTION OF STANDARD PRODUCTS

2.1 INTRODUCTION
This chapter contains detailed descriptions, specifications, programming and operating information for DIGITAL's 11 family terminals and communications equipment. For easy reference, first the group of terminals and then the communications equipment have been arranged alphabetically by model number, with the model number appearing on the top right-hand side of each page.

DIGITAL's Supplies Group maintains a complete line of operating computer supplies such as terminal accessories, paper, printer ribbons, magnetic disk media, tapes, cassettes and cabineting to protect and store supplies. These supplies are designed specifically for use with DIGITAL equipment.

Support specialists located throughout the world can recommend a comprehensive package of starter supplies for efficient and accurate implementation of computer systems. All orders are processed and shipped within 48 hours—24 hours for emergencies. Local sales offices will provide further information on request.
DECWRITER II PRINTER, LA35

FEATURES
- True 30 character per second throughput via the use of a 16 character buffer and 60 cps catch up mode.
- 7 x 7 dot matrix impact technology print head
- Up to 6 part forms (.020 maximum pack thickness)
- Variable width forms handling—from 3" through 14 7/8" (7.6 cm—37.6 cm) wide forms via adjustable width tractor feed
- 132 column print; 10 characters per inch horizontal spacing (20 characters per 10 cm)
- 6 lines per inch vertical spacing (12 lines per 5 cm)
- Extra quiet operation
- Crisp, clear and straight character formation
- Integrated 20 ma current loop interface. Passive mode standard with jumpers to activate the active mode
- Fine vertical adjustment for accurate forms placement
- Adjustable right and left hand tractors for margin positioning
- 90-132 VAC or 180-264 VAC operation to insure reliable operation in brown-out conditions
- Parity check prints replacement character (III). Strappable to odd, even, or none with mark or space
- Last character visibility (after 1300 ms timeout, head moves 4 columns to the right. Returns automatically when printing is resumed)
- Integral stand
- Rear door lock
- Top cover interlock
- Print window
- Power on indicator (Std. character lamp)
- Paper out (straps to send timed break or disconnect line)

OPTIONS AND ACCESSORIES
Paper stacking tray
Caster for rear of cabinet
Ribbons
Paper
EIA interface with timed disconnect, auto answer and modem control
APL/ANSI dual character set

DESCRIPTION
The LA35 DECwriter II is an advanced technology teleprinter designed to offer fast reliable operation. The DECwriter II is equally at home in communications applications or in slave printer applications.

2-2
The DECwriter II includes many practical functional and operator features. Among these are the true 30 cps throughput accomplished by a 60 cps catchup mode which is activated any time more than one character is present in the 16 character buffer. Also featured are quiet 48 db operation, infinitely variable vertical forms adjustment vernier, variable width and up to six part forms handling and countless other features.

The integral stand design provides correct height for easy operator viewing of the printed line.

CARRIAGE SYSTEM
The carriage system quietly transports the print head along a solid bar platen. An operator adjustable print gap allows the print head distance to be tuned for the highest quality print on every forms thickness. The carriage is driven by a quiet direct drive servo motor system at 3 or 6 inches (7.6 cm or 15.4 cm) per second (6" /second for catchup mode). A photo cell and slotted disk encoder system located right on the motor shaft provide oscillation free feed-back control to the micro-processor controlled servo system. Upon power up, the servo system is initialized by seeking out the left hand carriage stop and positioning .2 inches (.5 cm) to the right to establish the location of column 1.

PAPER FEED
The DECwriter II paperfeed system uses a stepper motor drive system for positive line location. A direct gear drive linkage drives the two adjustable width pin feed paper tractors to straight line drive up to 6 parts of continuous forms with no loss of registration between the first and the sixth copies. Fine positioning of the paper is possible by pushing in on the line feed knob to release the gear drive linkage and rotating the knob to move the paper in the desired direction. A paper out sensor is also standard equipment on the DECwriter II. With the LAXX-EIA option, a paper out condition can be strapped to send a break signal or disconnect the telephone line.

PRINT HEAD
The print head uses a ruby jewel head bearing to guide the seven solenoid driven print wires that make up the 7 x 7 character matrix. The DECwriter II's print head is designed to last a long time. Typical head life is of 5-7 years under average usage. Such reliability is possible because of sophisticated design details such as designing the curvature of the print wire guide tubes to match the natural curvature of the print wire.

RIBBON FEED SYSTEM
To prevent the ribbon from smudging the paper when the DECwriter II is not printing, the ribbon feed system is driven from the carriage servo system. Thus, ribbon motion only takes place with head motion. The DECwriter II's single plane ribbon travel system makes the long lasting 40 yard spool of nylon ribbon easy to remove and replace. Ribbon reversing is automatically accomplished by the sensing of a metal eyelet located at either end of the ribbon.
POWER SUPPLY ASSEMBLY
The option upgradable DECwriter II’s use a constant voltage transformer (CVT) to insure reliable operation over a wide voltage swing to allow continued operation under brown-out conditions. All 60 Hz upgradable DECwriter II’s use the same transformer with simple tap changes to change from the 90-132V range to the 180-264 range. Likewise, all 50 Hz upgradable DECwriter II’s use a dual voltage range transformer. The heavy duty supplies contain adequate power to handle all of the DECwriter II options.

OPERATOR CONTROLS
Power ON/OFF This rocker switch located on the operator’s control panel applies or removes AC power to the entire machine.

Line/Local This pushbutton on the operator’s control panel selects the on line or off line (local) mode of the DECwriter II.

Baud Rate 110, 150, 300 The two pushbuttons labeled 110 and 300 baud on the operator’s panel are used to select the communications line speed at which the DECwriter II will receive data. As indicated on the bezel above the keys, both depressed will select 150 baud operation.

Head of Form This pushbutton located on the operator’s panel is active only when one of the forms control options are installed in the DECwriter II. With one of the options installed, depressing this button will cause the forms to advance to the beginning of the next form as defined by the forms length control switch which is part of the forms control option.

Forms Thickness Adjustment Located on the right side of the print head carriage, this adjustment selects the proper gap for 1 through 6 part form.

Tractor Position Adjustment Located on each paper tractor assembly, these thumb screw adjustments allow movement of the paper tractors to set up margins and paper widths.

Fine Vertical Tractor Release The line feed knob may be depressed inward and rotated in the appropriate direction for precise location of printing with respect to vertical zones.

CONTROL PANEL INDICATORS
Paper Out This lamp indicates that the DECwriter II has run out of paper.
SPECIFICATIONS

Main Specifications

Printing Speed: 10, 15 or 30 characters/second asynchronous
Number of Print Columns: 132
Printing Characters: 63/95 character ASCII (Excludes space)

Printing
Type Font: Impact 7 x 7 dot matrix technology
Vertical Spacing: 6 lines per inch (12 lines per 5 cm.)
Horizontal Spacing: 10 characters per inch (20 characters per 10 cm)

Paper
Type: 3"—14/8" (7.6 cm—37.6 cm) wide continuous forms tractor driven. One to six parts (up to 20 mils maximum pack thickness).
Slew speed: 30 lines per second

Mechanical
Mounting: Self-contained unit with integral stand
Size: 33.2 inches H x 27.5 inches w x 24 inches D (84.3 cm x 69.9 cm x 61 cm)
Weight: 102 lbs. (46.3 kg) uncrated—140 lbs. (63.5 kg) crated

Power
Input Current: Maximum no options—2A
Maximum with options—5.5A
Heat dissipation: 300 watts printing maximum (no options)
700 watts printing maximum (options)
160 watts non printing (no options)
350 watts non printing (options)

Environment
Operating temperature: 10°C to 40°C
Relative humidity: 10% to 90%
Altitude: 0 Ft. to +8,000 ft. mean sea level
Ribbon: Digital-specification nylon fabric, spool assembly 0.5 inches wide x 40 yds (1.27 cm x 36.5 m). Supply item #36-10558.

COMMUNICATIONS

Receive Only DECwriter II Models
LA35-CE DECwriter II, 20 ma interface 90-132 VAC, 60 Hz
LA35-CJ DECwriter II, 20 ma interface 180-264 VAC, 50 Hz
LA35-HE DECwriter II, EIA interface 115 VAC 60 Hz
LA35-HJ DECwriter II, EIA interface 230 VAC 50 Hz

2-5
CODE  ANSI
Bit Structure  110 baud 1 start, 7 data, 1 parity, 2 stop bit
               150 baud 1 start, 7 data, 1 parity, 1 stop bit
               300 baud 1 start, 7 data, 1 parity, 1 stop bit
Parity  Parity. ODD, EVEN and no parity bit 8 marking or no parity with bit 8 spacing are number choices. A character with bad parity will force a substitute character (III) to be printed.

OPTIONS
The following options are available for use with the LA35. Refer to the LA36 section for descriptions of the options.

LAXX-KA  Casters, Paper tray and Shelf Kit
LAXX-KB  Casters kit
LAXX-KC  Shelf
LAXX-KD  Paper tray
LAXX-LG  EIA/CCITT Interface Option
LAXX-NC  Deep paper basket
DECWRITER II PRINTER TERMINAL, LA36

FEATURES

- True 30 character per second throughput via the use of a 16 character buffer and 60 cps catch up mode.
- 7 x 7 dot matrix impact technology print head
- Up to 6 part forms (.020 maximum pack thickness)
- Variable width forms handling—from 3” through 14 7/8” (7.6 cm—37.6 cm) wide forms via adjustable width tractor feed.
- 132 column print; 10 characters per inch horizontal spacing (20 characters per 10 cm)
- 6 lines per inch vertical spacing (12 lines per 5 cm)
- 128 character ASCII upper/lower case set (95 printable characters)
- Extra quiet operation
- Crisp, clear, and straight character formation
- Integrated 20 ma current loop interface. Passive mode standard with jumpers to activate the active mode.
- Fine vertical adjustment for accurate forms placement
- Adjustable right and left hand tractors for margin positioning
- 90-132 VAC or 180-264 VAC operation to insure reliable operation in brown-out conditions.
- Half or full duplex control on operators control panel
- Parity check on output prints replacement character (III). Strappable to odd, even, or none with mark or space.
- Last character visibility (after 1300 ms timeout, head moves 4 columns to the right. Returns automatically when printing is resumed).
- Integral stand
- ANSI—standard multi-key rollover typewriter-like keyboard
- 14 key numeric pad; 0-9, . , ', —, enter (CR).
- Column scale, line pointer, and column pointer
- Rear door lock
- Top cover interlock
- Print window
- Power on indicator (Std. character lamp)
- Paper out (straps to send timed break or disconnect line)

OPTIONS AND ACCESSORIES

Paper stacking tray
Caster for rear of cabinet
Right and/or left work surface
Ribbons
Paper
Document holder
EIA interface with timed disconnect, auto answer and modem control
APL/ANSI dual character set

DESCRIPTION
The LA36 DECwriter II is an advanced technology teleprinter designed to offer fast reliable operation with the best price/performance ratio of any 30 cps teleprinter in the industry. The DECwriter II is equally at home in communications applications or computer console applications.

The DECwriter II includes many practical, functional and operator features. Among these are the true 30 cps throughput accomplished by a 60 cps catchup mode which is activated any time more than one character is present in the 16 character buffer. Also featured are quiet 48 db operation, infinitely variable vertical forms adjustment vernier, variable width and up to six part forms handling and countless other features.

The integral stand design provides correct height for easy operator use of the typewriter-style keyboard.

OPERATION
Simple, elegant design subassemblies allow the DECwriter II to perform like the precision machine it is.

CARRIAGE SYSTEM
The carriage system quietly transports the print head along a solid bar platen. An operator adjustable print gap allows the print head distance to be tuned for the highest quality print on every forms thickness. The carriage is driven by a quiet direct drive servo motor system at 3 or 6 inches (7.6 cm or 15.4 cm) per second (6"/second for catchup mode). A photo cell and slotted disk encoder system located right on the motor shaft provide oscillation free feedback control to the micro-processor controlled servo system. Upon power up, the servo system is initialized by seeking out the left hand carriage stop and positioning 0.2 inches to the right to establish the location of column 1.

PAPER FEED
The DECwriter II paperfeed system uses a stepper motor drive system for positive line location. A direct gear drive linkage drives the two adjustable width pin feed paper tractors to straight line drive up to 6 parts of continuous forms with no loss of registration between the first and the sixth copies. Fine positioning of the paper is possible by pushing in on the line feed knob to release the gear drive linkage and rotating the knob to move the paper in the desired direction. A paper out sensor is also standard equipment on the DECwriter II. With the LAXX-LG EIA option, a paper out condition can be strapped to send a break signal or disconnect the telephone line.
PRINT HEAD
The print head uses a ruby jewel head bearing to guide the seven solenoid driven print wires that make up the 7 x 7 character matrix. The DECwriter II’s print head is designed to last a long time. Typical head life is of 5-7 years under average usage. Such reliability is possible because of sophisticated design details such as designing the curvature of the print wire guide tubes to match the natural curvature of the print wire.

RIBBON FEED SYSTEM
To prevent the ribbon from smudging the paper when the DECwriter II is not printing, the ribbon feed system is driven from the carriage servo system. Thus, ribbon motion only takes place with head motion. The DECwriter II’s single plane ribbon travel system make the long lasting 40 yard spool of nylon ribbon easy to remove and replace. Ribbon reversing is automatically accomplished by the sensing of a metal eyelet located at either end of the ribbon.

KEYBOARD ASSEMBLY
The DECwriter II features a multi-key rollover keyboard. The gold plated quadfurred contact keyswitch array uses the experience learned from calculator keyboard designs to produce 100 million key strobe operations of reliability. Other features include a 14 key numeric pad. The caps lock feature permits the operator to lock the alpha keys in uppercase mode while leaving the numerics and special symbols in lower case. This feature is not possible on conventional terminals using the shift lock technique.

POWER SUPPLY ASSEMBLY
The option upgradable DECwriter II’s use a constant voltage transformer (CVT) to insure reliable operation over a wide voltage swing to allow continued operation under brown-out conditions. All 60 Hz upgradable DECwriter II’s use the same transformer with simple tap changes to change from the 90-132V range to the 180-264 range. Likewise, all 50 Hz upgradable DECwriter II’s use a dual voltage range transformer. The heavy duty supplies contain adequate power to handle all of the DECwriter II options.

OPERATOR CONTROLS
<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power ON/OFF</td>
<td>This rocker switch located on the operator’s control panel to the left of the main keyboard applies or removes AC power to the entire machine.</td>
</tr>
<tr>
<td>Line/Local</td>
<td>This pushbutton on the operator’s control panel selects the on-line or off-line (local) mode of the DECwriter II.</td>
</tr>
<tr>
<td>Half/Full Duplex</td>
<td>This pushbutton located on the operator’s control panel selects the communications mode of the DECwriter II. In full duplex mode, the keyboard is logically separated from the printer. In half duplex mode, the printer will copy all printable characters keyed on the keyboard.</td>
</tr>
</tbody>
</table>
Baud Rate 110, 150, 300

The two pushbuttons labelled 110 and 300 baud on the operator's panel are used to select the communications line speed at which the DECwriter II will send or receive data. As indicated on the bezel above the keys, both depressed will select 150 baud operation.

ALT. CHAR SET

This pushbutton located on the operator's control panel is functional only when the dual character set option is installed in the machine. Operation of this pushbutton manually selects either the standard character set or the alternate set that is supplied as part of the dual character set option.

Char Set Lock

This pushbutton located on the operator's control panel is functional only when the dual character set option is installed in the DECwriter II. Its function is to either allow manual only or program only control of which character set is selected.

Auto LF

This pushbutton located on the operator's control panel is functional only when the auto line feed option is installed in the DECwriter II. When depressed, it will cause a CR and LF character to be transmitted whenever the CR key is depressed on the main keyboard.

Here is

Depressing this pushbutton, which is active only when the autoanswerback option is installed in the DECwriter II, will cause the contents of the answerback memory to be transmitted.

Forms Thickness Adjustment

Located on the right side of the print head carriage, this adjustment selects the proper gap for 1 through 6 part form.

Tractor Position Adjustment

Located on each paper tractor assembly, these thumb screw adjustments allow movement of the paper tractors to set up margins and paper widths.

Fine Vertical Tractor Release

The line feed knob may be depressed inward and rotated in the appropriate direction for precise location of printing with respect to vertical zones.

CONTROL PANEL INDICATORS

STD Char. Set

This indicator is used as a power on indication when the dual character set option is not present. With the option, either the standard character set or the alternate character set option are lit at all times to indicate the power on conditions.
**ALT Char Set**  This indicator when lit indicates that the dual character set option is installed in the DECwriter II and that the machine is under control of the second character set.

**Paper Out**  This lamp indicates that the DECwriter II has run out of paper.

**Device Selected**  This lamp, active only with the selective address option installed, indicates that the DECwriter II has been selected.

**Select Available**  This lamp, active only with the selective address option installed, indicates that the multiparty line is not in use and that the DECwriter II may become the master and select one or more slaves on the line to transmit and/or receive a message.

### SPECIFICATIONS

**Main Specifications**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Printing Speed:</td>
<td>10, 15 or 30 characters/second asynchronous</td>
</tr>
<tr>
<td>Number of Print Columns:</td>
<td>132</td>
</tr>
<tr>
<td>Printing Characters:</td>
<td>63/95 character ASCII set (Excludes space)</td>
</tr>
<tr>
<td>Keyboard Characters:</td>
<td>96 or 128 selectable by caps lock switch</td>
</tr>
<tr>
<td>Printing Type Font:</td>
<td>Impact 7 x 7 dot matrix technology</td>
</tr>
<tr>
<td>Vertical Spacing:</td>
<td>6 lines per inch (12 lines per 5 cm)</td>
</tr>
<tr>
<td>Horizontal Spacing:</td>
<td>10 characters per inch (20 characters per 10 cm)</td>
</tr>
</tbody>
</table>

**Paper**

| Type:                  | 3"-147/8" (7.6 cm—37.6 cm) wide continuous forms tractor driven. One to six parts (up to 20 mils maximum pack thickness). |
| Slew speed:            | 30 lines per second                        |

**Mechanical**

| Mounting:              | Self-contained unit with integral stand     |
| Size:                  | 33.2 inches H x 27.5 inches W x 24 inches D (84.3 cm x 69.9 cm x 61 cm) |
| Weight:                | 102 lbs. (46.3 kg) uncrated—140 lbs (63.5 kg) crated |

**Power**

| Input Current:         | Maximum no options—2A                      |
| Heat dissipation:      | Maximum with options—5.5A                   |
| 300 watts printing maximum (no options) |
| 700 watts printing maximum (options)    |
| 160 watts non printing (no options)      |
| 350 watts non printing (options)          |

**Environment**

| Operating temperature: | 10°C to 40°C |
| Relative humidity:     | 10% to 90%   |
| Altitude:              | 0 Ft to ±8,000 ft. mean sea level            |
Ribbon
Digital-specified nylon fabric, spool assembly
0.5 inches wide x 40 yds (1.27 cm x 36.5 m).
Supply item #36-10558

COMMUNICATIONS

Models
LA36-CE  DECwriter II, 20 ma interface 90-132 VAC 60 Hz
LA36-CJ  DECwriter II, 20 ma interface 180-264 VAC 50 Hz
LA36-HE  DECwriter II, EIA interface 115 VAC 60 Hz
LA36-HJ  DECwriter II, EIA interface 230 VAC 50 Hz

CODE  ANSI

Bit Structure  110 baud 1 start, 7 data, 1 parity, 2 stop bit
150 baud 1 start, 7 data, 1 parity, 1 stop bit
300 baud 1 start, 7 data, 1 parity, 1 stop bit

Parity
Input and output parity. ODD, EVEN and no parity bit
8 marking or no parity with bit 8 spacing are number
choices. An output character with bad parity will force
a substitute character (III) to be printed.

OPTIONS

LA3X-LG—EIA/CCITT Interface option
This option provides an EIA RS232-C or CCITT-V24 interface for any
LA36. The option includes auto answer, timed disconnect and half/full
duplex logic to provide earlier LA36's with half duplex. A 9 foot cable
with 25 pin data set type connector is also supplied with this option.

LA3X-PK—APL/ANSI dual character set
The APL/ANSI dual character set option allows the DECwriter II to be
used as a bit paired ASCII APL terminal. With this option installed, the
DECwriter II has two character sets and selection of the desired set is
possible via the receipt of Switch In (SI) and Switch Out (SO) ASCII con-
trol codes or via the ALT. character set switch on the operator's control
panel. The character set lock switch is used to either lock out manual
control or host computer control of character set selection.

ACCESSORIES

LA3X-KA—Casters, Paper tray and Shelf Kit
This accessory provides a DECwriter II with two rear casters to allow the
terminal to be easily moved, a paper stacking tray to catch the printer
paper behind the DECwriter II and a right and or left shelf area to pro-
vide operator work space.

LA3X-KB—Casters kit for DECwriter II
Kit of two casters as described in the LA3X-KA option.

LA3X-KC—Shelf for DECwriter II
This accessory provides the operator work area as described in the
LA3X-KA option. Two shelves can be mounted on the DECwriter II at one
time.
LAXX-KD—Paper tray for DECwriter II
This accessory provides only the paper catcher as described in the LAXX-KA.

LAXX-NC—Deep paper basket for DECwriter II and DECprinter I.

H981-A
This accessory provides the operator of a DECwriter II with an adjustable position document holder.
DECPRINTER I, LA180

FEATURES

- 180 characters per second
- Parallel interface
- Handles variable-width forms, 3 through 14\(\frac{7}{8}\) inches (7.6 cm—37.6 cm) wide
- 132-column print; 10-characters-per-inch horizontal spacing (20 characters per 10 cm)
- 6-lines-per-inch vertical spacing (12 lines per 5 cm)
- 128-character ASCII upper/lower case set
- 7 x 7 dot matrix
- Backspace capability
- Quiet operation
- Excellent character readability
- Fine vertical adjustment for accurate forms placement
- Paper-out switch
- Paper-out override
- Switch-selectable forms length (11 lengths)
- Drives 100-foot (30.5 m) cable

Optional

- Paper stacking tray
- Casters for rear of cabinet

DESCRIPTION

The LA180 DECprinter I is a high-speed printer with an extensive array of standard features. DECprinter I extends the field-proven technology of the LA36 DECwriter II into applications demanding higher speed capabilities.

DECprinter I has many operator features which enhance its ease of use. Included are a forms-length switch which sets the top-of-form to any of 11 common lengths, paper-out switch and alarm, and high reliability printhead. Also featured are quiet operation, infinitely variable forms adjustment, variable forms width, and multipart forms capability.

Operation

Seven solenoid-driven wires form the characters by scanning the page from left to right. The scanning motion is servo controlled, thereby assuring accurate dot placement and quiet, reliable operation. The machine prints a line at a time and automatically performs a carriage return upon receipt of a CR, LF, or FF command.
**Power-Up**
Upon power-up, the DECprinter I is initialized to execute incoming data. The head moves to the left and stops at column 1.

**Carriage System**
The carriage system transports the head along the horizontal axis of the machine, provides accurate horizontal positioning for character placement, and provides printhead adjustment for clean impressions on a variety of forms.

The carriage is controlled by a servo system which assures accurate dot placement. The servo operates in the forward direction at 18 inches per second and has a carriage return time of less than 275 ms.

**Ribbon Feed System**
The ribbon feed system is driven by the carriage motion only when the carriage is moving from left to right. This prevents ribbon smudging when the DECprinter I is not printing.

**Paper Feed System**
The paper feed system is a stepping-motor-driven tractor feed. The tractor design provides 3-to-4-pin engagement of the form and a flat bed for control and positive feeding of multipart forms. Paper may be fine-positioned vertically by pushing the line feed knob inward and rotating it in the direction desired.

**OPERATOR CONTROLS**

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power ON-OFF</td>
<td>Applies and removes AC power to entire machine.</td>
</tr>
<tr>
<td>Line/Off Line</td>
<td>Enables or disables communications.</td>
</tr>
<tr>
<td>Head of Form</td>
<td>Feeds form to the next top-of-form or single lines, if forms switch is set in single-line position. If paper is out, printing can be continued to next top-of-form by keeping Head-of-Form button depressed.</td>
</tr>
<tr>
<td>Length of Form</td>
<td>Selects any of 11 forms lengths.</td>
</tr>
<tr>
<td>Set VFU</td>
<td>Used in conjunction with Length-of-Form switch to reset forms length.</td>
</tr>
<tr>
<td>Test</td>
<td>Will run test pattern locally if set in this position.</td>
</tr>
<tr>
<td>Forms Thickness</td>
<td>Located on right side of printhead carriage. Selects proper gap for 1-through-6-part form. Approximately 1 click for each part.</td>
</tr>
<tr>
<td>Adjustment</td>
<td>Thumb screw may be loosened to allow movement of both tractors for various forms widths.</td>
</tr>
<tr>
<td>Fine Vertical</td>
<td>Line-feed knob may be depressed inward and rotated in the appropriate direction for precise location of printing with respect to vertical zones.</td>
</tr>
<tr>
<td>Tractor Release</td>
<td></td>
</tr>
</tbody>
</table>

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REGISTERS
Control and Status Register (LPS) 777 514

BIT  NAME  FUNCTION
15  Error  ERROR asserted indicates the inclusive OR of one of the
         following line printer error conditions:

   0  1  2  3  4  5  6  7  8  9  10  11  12  13  14  15
        ERROR  DONE  INTERRUPT ENABLE

   a. Paper Empty
   b. Hardware Alarm
   c. Light Detection
   d. Select

   ERROR is Read Only, and is reset only when the error
   condition is removed. If interrupt Enable is also set, the
   LA180 starts an interrupt sequence.

7  Done  DONE is asserted when the line printer is ready to
        accept another character. DONE is set by INIT and
        cleared by loading the LPB. If interrupt Enable is also
        set, the LA180 starts an interrupt sequence.

6  Interrupt Enable
    Interrupt Enable is set or cleared by the program and
    cleared by INIT. Either DONE or ERROR set when IE is
    set initiates an interrupt sequence.

Data Buffer Register (LPB) 777 516

BIT  NAME  FUNCTION
6-0  Data  The Data bits are the 7-bit characters transferred to the
         line printer. The characters are coded in ASCII and are
         Write Only.

SPECIFICATIONS
Main Specifications
Printing speed: 180 characters/second
Number of columns: 132
Printing characters: 96 characters ASCII set
LA180

Printing
Type: Impact 7 x 7 dot matrix
Vertical spacing: 6 lines/inch (12 lines per 5 cm)
Horizontal spacing: 10 characters/inch (20 characters per 10 cm)

Paper
Type: 3 through 14½ inches wide (7.6 cm—37.6 cm), continuous business form, original and 5 copies (.020 inch (.5 mm) maximum pack thickness)

Single-line skip: 32 ms
Slew speed: 7.5 inches (19 cm)/second; 45 lines/second

Mechanical
Mounting: 1 free-standing unit
Size: 33.2 inches (84.3 cm) high x 27.5 inches (69.9 cm) wide x 20 inches (50.8 cm) deep
Weight: 102 lbs. (46.3 kg)

Power
Input current: 3.0A at 115 Vac
1.5A at 230 Vac
Heat dissipation: 400 W printing
200 W non printing

Environment
Operating temperature: 10°C to 40°C
Relative humidity: 10% to 90% noncondensing, maximum wet bulb 29°C

Ribbon
DIGITAL-specified nylon fabric, spool assembly, (.5 inches wide x 60 yards long) Order #3612153

SPECIFICATIONS FOR CONTROL
Register Addresses
Control and Status 777514
Data Buffer 777516

UNIBUS Interface
Interrupt vector address: 200
Priority level: BR4
Bus loading: 1 bus load

Mechanical
Size: 1 SPC slot (quad module)
Input Current: 1.5A at +5V

Models
LA180-CA Serial 20mA DECprinter, 115V, 60 Hz
LA180-CD Serial 20mA DECprinter, 230V, 50 Hz

2-17
<table>
<thead>
<tr>
<th>Model Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LA180-EA</td>
<td>Serial EIA DECprinter, 115V, 60 Hz</td>
</tr>
<tr>
<td>LA180-ED</td>
<td>Serial EIA DECprinter, 230V, 50 Hz</td>
</tr>
<tr>
<td>LA180-PA:</td>
<td>Parallel I/O DECprinter, 115V, 60 Hz</td>
</tr>
<tr>
<td>LA180-PD:</td>
<td>Parallel I/O DECprinter, 230V, 50 Hz</td>
</tr>
<tr>
<td>LA11-PA:</td>
<td>Printer and control, 115V, 60 Hz</td>
</tr>
<tr>
<td>LA11-PD:</td>
<td>Printer and control, 230V, 50 Hz</td>
</tr>
</tbody>
</table>
DECScope Video Display Terminal, VT52

DESCRIPTION
The VT52 is an upper-and-lower-case ASCII video terminal whose display holds 24 lines of 80 characters.

The VT52's human-engineering features include the following: A clicking sound provides feedback to the operator when keys are typed; a rollover feature lets the terminal get the message straight even if two or three keys are pressed at once; the keyboard follows the standard typewriter layout.

The VT52 also provides a "two-way" keypad. In one mode, the keypad is used to generate program-compatible numeric codes. Applications which require much numeric input can use the VT52 without modifying hardware or software, while the operator uses the convenient "numeric pad." Or, software may place the VT52 in the alternate mode, in which each key on the keypad transmits a unique Escape Sequence. This allows the host computer to distinguish between keys typed on the auxiliary keypad and similar keys on the main keyboard. In this mode, each key on the keypad can be used to invoke a user-defined function.

The VT52 has a wide range of cursor-positioning functions. As well as moving the cursor one position in any direction, software can move the cursor to any position on the screen with a Direct Cursor Addressing command which specifies the destination for the cursor. The VT52 also offers fixed horizontal tabs, a "Cursor-to-Home" command, and two screen-erasure functions. Data on the screen scrolls up when a Line Feed function is performed with the cursor on the bottom line; it scrolls down when a Reverse Line Feed function is performed with the cursor on the top line.

APPLICATIONS
A Window on a File. The VT52's full character set (upper-and-lower-case) makes it an excellent terminal for text entry and editing. Its design suggests a new method of editing text: a method in which the operator, rather than having to learn a new command language for text-editing, simply arranges text on the screen the way the file is to read. The computer, which maintains an image of the text displayed on the VT52's screen in memory, responds to special commands from the operator and performs advanced features involving text compression or expansion.

The VT52, with 24 lines, lets the operator view a large portion of the file. To move about in files containing more than 24 lines, the VT52 can scroll the information on its screen up and down.

When the operator gives the host a command to end the editing session, the host writes its screen image onto a storage device. This text-editing system is "error-proof," since there is never any doubt as to what the file contains at any time.
A Dynamic Display System. The 24 lines of the VT52's screen can be used to monitor 24 separate processes, or more. Consider a situation in which the VT52 is displaying the status of 24 scheduled airline flights, one on each line. If some of the information changes, it is possible to change the field on the screen which displays that information without rewriting the whole screen.

The VT52 fits this application with its Direct Cursor Addressing, a feature which allows software to move the cursor from any position on the screen to any other position with a single command.

To replace any information on the screen, the host sends the Direct Cursor Addressing command, two characters which select the line and column number, and the new data.

A File Display System. In its Hold-Screen Mode, the VT52 allows the operator to control the flow of data onto the screen. With most terminals, whatever the host sends to the terminal goes on the screen immediately. But the VT52 can operate at such a rapid speed that 12 full lines of data could be scrolled off the top of the screen every second, as new data enters the screen at the bottom. In Hold-Screen Mode, the VT52 will not perform a scroll until requested to do so by the operator. In a situation where any data would be scrolled off the screen, the VT52 buffers incoming data rather than processing or displaying it, and sends signals to the host telling it to stop or resume transmitting.

If the operator types the SCROLL key, the terminal will allow one line of data through to the screen. The operator can also use the SCROLL key to request the VT52 to accept 24 new lines, one new screenful, from the host.

Business Data Entry. In addition to providing keys for the numerals and decimal point, the VT52's 19-key numeric pad contains an ENTER key (which transmits the control code CR), and three blank keys. These keys transmit unique, multiple-character Escape Sequences which can be interpreted by software. The four remaining keys are labeled with arrows pointing up, down, right, and left. The host can respond to these keys by positioning the cursor, or, since these keys transmit Escape Sequences as the blank keys do, they can be relabeled and used to transmit special commands to software. If these Escape Sequences are echoed back literally, the cursor will move one position in the corresponding direction on the screen. Software can place the VT52 in a mode where all 19 keys on the numeric pad transmit unique Escape Sequences.

A key-click sound system, the layout of the keyboard, and 2½-key rollover are all designed to give the VT52 the look and feel of a regular typewriter. This improves the efficiency of the typist and minimizes training time.
**Changing Configurations.** The VT52 is plug-compatible and functionally upward-compatible with the VT50. When VT52s and VT50s are used in the same computer system, software can send each terminal a command to identify itself. The VT52 will automatically transmit a three-character Escape Sequence which identifies it as a VT52. The host thus determines which features can be used with the terminal presently attached.

The significance of this feature is that VT50s, VT52s and future VT models can be freely interchanged within a system, with the software responding correctly to each different type of terminal.

### TECHNICAL INFORMATION

#### Commands

The following table lists the actions which the terminal takes upon receipt of the corresponding codes from the host computer.

<table>
<thead>
<tr>
<th>Character(s) and Octal Code(s)</th>
<th>Action Taken</th>
</tr>
</thead>
<tbody>
<tr>
<td>BEL (007)</td>
<td>Sounds the audible alarm.</td>
</tr>
<tr>
<td>BS (010)</td>
<td>Moves the cursor left one position, unless it was at the start of a line to begin with.</td>
</tr>
<tr>
<td>TAB (011)</td>
<td>Moves the cursor rightward to the next TAB stop, unless the cursor was at the end of a line to begin with. (TAB stops are fixed in columns 9, 17, 25, 33, 41, 49, 57, 65, 73, 74, 75, 76, 77, 78, 79, and 80.)</td>
</tr>
<tr>
<td>LF (012)</td>
<td>Moves the cursor down one line—performs an upward scroll if the cursor was on the bottom line.</td>
</tr>
<tr>
<td>CR (015)</td>
<td>Moves the cursor to the start of the same line it was on.</td>
</tr>
<tr>
<td>ESC (033)</td>
<td>Serves as a signal that the following character is to be interpreted rather than displayed; ESC introduces multicharacter commands—&quot;Escape Sequences&quot;—which are listed below.</td>
</tr>
<tr>
<td>Space (040) and the displayable characters (041-176)</td>
<td>The character is displayed at the cursor position; then the cursor is moved right one column, unless it was at the end of a line to begin with. In particular, Space (040) blanks the character at the cursor position and moves the cursor right.</td>
</tr>
<tr>
<td>NUL (000) and DEL (177)</td>
<td>The terminal does not respond to NUL or DEL, in order to be compatible with slower electromechanical devices that use these characters as fillers.</td>
</tr>
</tbody>
</table>
Escape Sequences | Effect
---|---
ESC = (033 075) | ENTERs Alternate-Keypad Mode.

In Alternate-Keypad Mode, keys on the numeric pad transmit unique Escape Sequences to distinguish them from similar keys on the main keyboard, and to invoke user-defined functions.

ESC > (033 076) | EXITs Alternate-Keypad Mode—returns to Numeric-Keypad Mode. (Alternate-Keypad Mode remains in effect until this command disables it.)

ESC A (033 101) | Moves the cursor up one line, unless it was already on the top line—does not perform a scroll.

ESC B (033 102) | Moves the cursor down one line, unless it was already on the bottom line—does not perform a scroll.

ESC C (033 103) | Moves the cursor right one column, unless it was already at the end of a line—does not erase the character at the old cursor position.

ESC D (033 104) | Moves the cursor left one column, unless it was already at the start of a line—same as BS (010).

ESC H (033 110) | Moves the cursor HOME: to the start of the top line.

ESC I (033 111) | Moves the cursor up one line—performs a downward scroll if the cursor was on the top line.

ESC J (033 112) | Erases all data from the cursor position to the end of the screen.

ESC K (033 113) | Erases all data from the cursor position rightward on the same line.

ESC Y (033 131) | Direct Cursor Addressing feature—moves the cursor to any specified position on the screen, regardless of where it was before. (The format of this command is shown below.)

ESC Z (033 132) | Requests the terminal to identify itself. The terminal will respond with a three-character Escape Sequence unique to its own configuration.

ESC [ (033 133) | Enters Hold-Screen Mode. In Hold-Screen Mode, data will not be scrolled off the screen until the operator requests it by typing the SCROLL key.

ESC \ (033 134) | EXITs Hold-Screen Mode. (Hold-Screen Mode remains in effect until this command disables it.)

**Direct Cursor Addressing Command**

Format:

```
ESC Y Line# Column#
```

Line# is one character; octal code 040 to refer to the top line, 041 to refer to the second line,
... 067 to refer to the bottom line. Column# can legally range from 040 (leftmost column) to 157 (rightmost column). The cursor is moved to the specified column of the specified line.

033 110 (move the cursor HOME) is equivalent to
033 131 040 040 (move the cursor to column 1 of line 1)

Summary of Basic Cursor Movements

| UP:     | ESC A | does not scroll | scrolls text down* |
| DOWN:   | ESC B | does not scroll | scrolls text up*   |
| RIGHT:  | ESC C | does not erase  | erases            |
| LEFT:   | ESC D | (these two are equivalent) |

**The BREAK Key**

Typing the BREAK key causes the transmission line to be forced to its zero state for as long as the BREAK key is held down.

The BREAK function is commonly used to forcible interrupt the flow of data coming to the terminal. It is provided for users with older software written to operate in Half Duplex. In Half Duplex, only one data communication line exists between terminal and computer. If the computer has control of this line, BREAK is the only means of forcing an interrupt. However, because DECsoscopes have both input and output lines, the forcible BREAK is normally unnecessary.

**The REPEAT Key**

Any key which transmits a code (or codes) to the computer will transmit that code (or codes) repeatedly if pressed while the REPEAT key is down. The keys on the numeric pad which transmit more than one character apiece will transmit their sequence repeatedly, if pressed with the REPEAT key down. The rate of repetition may attain 30 characters per second (on 50 Hz models, 25 characters per second), or it may be limited to a slower rate if the baud rate is not set to accommodate such rapid transmission.

**The SHIFT Keys**

On keys which have more than one symbol, the code for the top symbol will be transmitted if either or both of the SHIFT keys are pressed; the code for the bottom symbol will be transmitted if neither SHIFT key is down.

Typing any alphabetic key when either or both of the SHIFT keys are down will cause an upper-case code to be transmitted. Typing an alphabetic key when neither SHIFT key is down will cause a lower-case code

*If the cursor cannot move any further in the specified direction.

2-23
to be transmitted. The SHIFT keys also affect the function of the SCROLL key.

The CAPS LOCK Key
When the CAPS LOCK key is down, typing any alphabetic key (A through Z) will cause an upper-case code to be transmitted, regardless of whether a SHIFT key was down. But unlike a typewriter’s SHIFT LOCK key, CAPS LOCK does not affect the codes transmitted by keys other than the alphabetic keys.

The CONTROL Key
When the CONTROL key is pressed, the two high-order bits of each character are masked out, allowing “control codes”—in the range 000-037—to be generated from the keyboard.

The Keypad
The VT52’s keypad operates in one of two modes. Software can place the terminal in a mode in which the keypad can be used for data entry, just as the main keyboard’s numeral keys can be used. If it is desired to distinguish between the typing of keys on the keypad and keys on the main keyboard, software can select a mode in which each key on the keypad transmits a unique Escape Sequence.

<table>
<thead>
<tr>
<th>Typing the key labeled...</th>
<th>IN NUMERIC-KEYPAD MODE, transmits the following code(s)</th>
<th>IN ALTERNATE-KEYPAD MODE, transmits the following code(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>ESC ? p</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>ESC ? q</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>ESC ? r</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>ESC ? s</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>ESC ? t</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>ESC ? u</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>ESC ? v</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>ESC ? w</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>ESC ? x</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td>ESC ? y</td>
</tr>
<tr>
<td>.</td>
<td>.</td>
<td>ESC ? n</td>
</tr>
<tr>
<td>ENTER</td>
<td>CR</td>
<td>ESC ? M</td>
</tr>
<tr>
<td>(up arrow)</td>
<td>ESC A</td>
<td>ESC A</td>
</tr>
<tr>
<td>(down arrow)</td>
<td>ESC B</td>
<td>ESC B</td>
</tr>
<tr>
<td>(right arrow)</td>
<td>ESC C</td>
<td>ESC C</td>
</tr>
<tr>
<td>(left arrow)</td>
<td>ESC D</td>
<td>ESC D</td>
</tr>
<tr>
<td>(left blank key)</td>
<td>ESC P</td>
<td>ESC P</td>
</tr>
<tr>
<td>(center blank key)</td>
<td>ESC Q</td>
<td>ESC Q</td>
</tr>
<tr>
<td>(right blank key)</td>
<td>ESC R</td>
<td>ESC R</td>
</tr>
</tbody>
</table>

If the codes transmitted by the “arrow” keys are echoed back to the terminal, they will cause the cursor to move one position in the direction the arrow points in.

The CONTROL, SHIFT, and CAPS LOCK keys do not affect the codes transmitted by the keys on the keypad, in either Keypad Mode.
The SCROLL Key
(Significant only with the terminal in Hold-Screen Mode.)

UNSHIFTED  Directs the terminal to allow one scroll to occur, admitting one new line of data to the screen.

SHIFTED  Directs the terminal to allow 24 scrolls to occur, admitting one new screenful of data to the screen.

Hold-Screen Mode

Host is transmitting data to VT52—transmits proper codes to place VT52 in Hold-Screen Mode.

Host transmits LF to VT52. Cursor is on the bottom line, but VT52 may not perform a scroll.

VT52 buffers LF and subsequent characters. Since it cannot process them without scrolling the display, it sends XOFF (023) to request that the host suspend transmission.
Operator, having finished reading the display, types the SCROLL key to see more lines.

Data from the buffer is now processed. In particular, LF is processed, causing a scroll. Line 1 leaves the screen; line 25 begins to appear at the bottom.

If the entire buffer is exhausted without encountering a second LF, the VT52 sends XON (021) to the host to request it to resume transmission. XOFF, XON, and the VT52 buffer are completely transparent to the user.

**SPECIFICATIONS**

**Dimensions:**
- Height: 36 cm (14.1 in.)
- Width: 53 cm (20.9 in.)
- Depth: 69 cm (27.2 in.)
- Minimum Table Depth: 45 cm (17.7 in.)

**Weight:**
- 20 kg (44 lbs)

**Operating Environment:**
- 10°C to 40°C (50°F to 104°F)
- Relative humidity 10% to 90%
- Maximum wet bulb 28°C (82°F)
- Minimum dew point 2°C (36°F)

**Line Voltage:**
- (US model) 100-126 volts
- (European model) 191-238 volts or 209-260 volts

**Line Frequency:**
- (US model) 60 ± 1 Hz
- (European model) 60 ± 1 Hz or 50 ± 1 Hz

**Power Consumption:**
- 110 Watts

**Power Line Hash Filter:**
- Low Leakage Balun type

**Display:**
- Format: 24 lines x 80 characters
- Character Matrix: 7 x 7
- Character Size: 2.0mm x 4.0mm (0.08 in. x 0.16 in.)
Screen Size: 21 cm x 10.5 cm (8.3 in. x 4.1 in.)
Character Set: 96-character displayable ASCII subset (upper and lower-case, numeric, and punctuation).

Keyboard:
Character Set: Complete 7 bit ASCII set (128 codes)
Key layout: Typewriter—rather than keypunch—format, 63 keys.
Auxiliary keypad: 19-keys: numerals, cursor-movement, 3 user-definable function keys.
CAPS LOCK Key: Locks alphabetic keys to upper-case state, but does not affect non-alphabetic keys.

Audible Signals:
Key-click: Switch-controlled
Bell: Sounds (a) upon receipt of control characters BEL; (b) when Keyboard input approaches right margin (output from host approaching right margin does not cause bell to ring).

Page Overflow:
LF causes upward scroll; Reverse Line Feed causes downward scroll.

Parity:
Even or mark (no parity) switch-selectable. Odd or space possible with rewiring.

Cursor:
Type: Blinking underline.
Control: Up or down one line; right or left one character; home; tab (fixed tab stops every 8 spaces); direct cursor addressing (allows cursor to be moved to any character position on the screen).

Functions:
Erase display from cursor position to end of line; erase to end of screen; scroll up; scroll down.

Hold-Screen Mode:
Allows operator to halt transmission from host, preserving data on display. Operator can request new data, line- or screenful-at-a-time. Enabled/disabled by Escape sequences sent by system software.

Terminal Self-Identification:
Terminal transmits on command a sequence unique to its model; software can identify features available on any terminal it is in contact with.

Communications:
20mA current loop or EIA interface; specify at time of order.
Code: USASCII extended through Escape Sequences.
Speed: Switch-selectable.
Transmission rates, full duplex (switch selec-
VT52

Switch-selectable local copy.

Synchronization: Automatically transmits control codes to host, requesting suspension and resumption of transmission, when unable to process data.

Operator Controls: Power On/Off, Intensity Control, Baud Rate Switch, Terminal Mode Switch, Key-Click On/Off, Even/No Parity.

Overload Protection: Thermal cutout.

Case Material: Injection molded Noryl thermoplastic.

Screen Phosphor: P4
DECGRAPHIC SCOPE TERMINAL, VT55

FEATURES

- 96-character ASCII upper/lower case set may be displayed on the CRT and printed on the copier output
- Direct cursor addressing in alphanumeric mode
- Displayable graphics—two individually chosen graphs or histograms with 512 points along the horizontal axis
- Graph grid composed of as many as 512 vertical lines and 236 horizontal lines, all individually selectable
- Display area—eight inches (20.3 cm) horizontal by five inches (12.7 cm) vertical
- Displayable alphanumerics—24 lines, 80 characters per line
- Key pad for direct cursor addressing and numeric entry
- ANSI-standard keyboard with control keys similar to office typewriters
- 7x7—point character font
- Microprocessor internal electronics
- Lightweight cabinet of high-impact, injection-molded design

TECHNOLOGY

The VT55 uses a unique combination of technologies. The internal electronics is a microprocessor design. A specialized computer program is constantly running within the terminal, waiting to service a request to transmit data from the keyboard to the serial line output, enter data into the internal semiconductor memories, service a copier request, etc. A separate memory is allotted to alphanumeric data, graph data, and terminal control information.

The display of alphanumeric and graphic data is performed by the raster scan method. It is reliable and produces bright, flicker-free information output. The generation of the raster scans and intensification information are synchronized to the microprocessor, thus eliminating the need for vertical and horizontal hold controls.

The copier option uses a scanning technique similar to methods utilized in facsimile picture transmission systems. This technique, in conjunction with the use of modern recording paper, generates high-quality copy in a minimum-size package with a minimum number of moving parts.

DESCRIPTION

The VT55 DECscope is a serial line interfaced computer terminal that features alphanumeric and graphic display in a single unit with upper and lower case characters. When interfaced to a host computer, the VT55 can display one or two graphs or histograms supported by programmable grid and programmable graph markers. With added alphanumeric information, a completely defined graph is displayed.
VT55

The VT55 may be used as a 24 line programmer's terminal, using only the DECscope alphanumeric capability with the console keyboard and keypad.

Some models of the VT55 also include a copier unit that generated a paper copy of the screen's contents, both alphanumeric and graphic.

The VT55 is packaged in a compact desktop cabinet. Information is displayed on a 12-inch (28.8cm) (diagonal measurement) cathode ray tube on the front of the unit along with the console keyboard. All electronics are housed within the VT55 cabinet. On models with copiers, the copier mechanics and the hard copy output are located at the top right side of the cabinet.

OPERATOR CONTROLS

Power/Logic/Reset  This switch is located on the right side of the unit.

Intensity control  Adjust slide control at the rear, near the top of the unit. Slide control toward the center to reduce intensity.

Copy key  Depress to produce hard copy output of video screen display. Use pinch roller release lever to release paper copy.

Baud rate  Tilt the VT55 on its back to set S1 and S2 to the desired baud rate and full duplex mode.

Keyboard  The standard typewriter keyboard contains the keys that generate the 96-character set, a control key for generating 32 control codes, plus unique VT55 function keys. These separate function keys are duplicates of control codes that may be generated from combinations of other keys on the keyboard. They represent frequently used operations such as TAB, BACKSPACE, RETURN, etc.

Keypad  The keypad contains three blank keys which transmit 2-character escape sequences for which a user can define meanings to tailor the keypad to an application. Four other keys labeled with arrows in each of four directions are used to move the cursor one character position. The remaining keys transmit codes for numerals and decimal point.

MODELS AND OPTIONS

DECscope with copier

VT55-FA, 20mA with Mate-N-Lok connector, 115VAC, 60Hz
VT55-FB, 20mA with Mate-N-Lok connector, 220/240VAC, 50Hz
VT55-FE, EIA with RS-232-C connector, 115VAC, 60Hz
VT55-FF, EIA with RS-232-C connector, 220/240VAC, 50Hz
VT55-JA, 20mA with 283B connector, 115VAC, 60Hz
VT55-JB, 20mA with 283B connector, 220/240VAC, 50Hz

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DECScope without copier

VT55-EA, 20mA with Mate-N-Lok connector, 115VAC, 60Hz
VT55-EB, 20mA with Mate-N-Lok connector, 220/240VAC, 50/60Hz
VT55-EC, 20mA with Mate-N-Lok connector, 100/127VAC, 50/60Hz
VT55-EE, EIA with RS-232-C connector, 115VAC, 60Hz
VT55-EF, EIA with RS-232-C connector, 220/240VAC, 50/60Hz
VT55-EH, EIA with RS-232-C connector, 100/127VAC, 50/60Hz
VT55-HA, 20mA with 283B connector, 115VAC, 60Hz
VT55-HB, 20mA with 283B connector, 220/240VAC, 50/60Hz
VT55-HC, 20mA with 283B connector, 100/127VAC, 50/60Hz

COMMUNICATIONS

For most applications the VT55 will be interfaced to a host computer with a serial line cable and operated in full duplex communication mode. Data transmitted by the VT55 is received by the host computer. Data received by the VT55 is determined solely by the host computer. This is a typical interface for an interactive man-machine environment.

The VT55 may also be set to local mode or to full duplex with local copy mode of operation. The latter is useful when the host computer does not generate an immediate echo or response to a keyboard transmission, and a visual verification of the information being sent is desired.

The VT55 is capable of sending and receiving at rates from 75 to 9600 baud. Data is sent in serial digital format for the 20mA interface models. The EIA interface models allow the use of the VT55 with RS-232-C signals.

VT55 models with Mate-N-Lok connectors are primarily intended for interfacing with 20mA DIGITAL serial line communications interfaces. Units with RS-232-C connectors are compatible with RS-232-C Standard Dataphone and Modem connectors. Connector 283B is a telephone-type plug compatible with DECSYSTEM-10 installations.

INTERFACE CHARACTERISTICS

Type 20mA current loop or EIA, depending on model

Speed 75, 110, 150, 300, 600, 1200, 2400, 4800, and 9600 baud
       110, 150, 300, 600, 1200, 2400, 4800, and 9600 baud
       Transmission at 75, 150, 300, or 4800 baud with reception at 110, 600, 1200, 2400, 4800, or 9600 baud

Transmission 75, 150, 300, 600, 1200, 2400, 4800, and 9600 baud
       110 baud only
       Generated on transmission as odd or even parity or a mark. (Parity suppression is switch-selectable.) Parity is not checked on reception.

10-Bit Length 75, 150, 300, 600, 1200, 2400, 4800, and 9600 baud

11-Bit Length 110 baud only

Parity Generated on transmission as odd or even parity or a mark. (Parity suppression is switch-selectable.) Parity is not checked on reception.

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VT55

Supplied Cable Length
20 mA models 7.6m (25 ft)
EIA models 7.6m (25 ft)

Maximum Cable Length
20 mA models 304.8 m (1000 ft)
EIA models 15.2 m (50 ft)

VT55 OPTIONS

There are three cable options available for the VT55.
1. BN52C-7F 7.6-m (25 ft), current loop cable with a 283B telephone type plug
2. BN52B-7F 7.6-m (25 ft), 20mA adapter cable with an 8-pin Matern-Lok connector
3. BN52A-7F 7.6-m (25 ft), EIA cable with the standard 25-pin EIA connector

These optional cables allow the user to convert a VT55 for use with either a 20mA current loop interface or an EIA interface in the event interface requirements change.

SPECIFICATIONS

Video Display
Size 30.5 cm (12 in) diagonal
Active Screen Size 20.3 x 12.7 cm (8 x 5.0 in)
Method Raster scan, roll-free
Phosphor P4
Linearity ± ½ point

Alphanumericics
Character Lines 24
Character Columns 80
Control Blinking alpha cursor
Character Set 96-Character, upper and lower case ASCII subset
32 control characters, and graphic characters
Special Features Upward and downward scroll, bell, erase, tabulate, cursor control
Character Format 7 x 7 matrix

Graphics
Resolution 512 horizontal x 236 vertical points
Graphs or Two single-valued functions of x, each individually controlled
Histograms
Grid 512 vertical lines and 236 horizontal lines, each individually controlled
Graph Markers 512/graph, total of 1024. Each graph marker is individually controlled
Special Features Individual blanking and unblanking of all graph features, clear all graphs
VT55

Special Features

Hold Screen Mode
Terminal Identifier
Allows interruption of data transmission for extended display viewing
Terminal will respond with ESC/E when receiving ESC/Z.

Keyboard

Format
Keyclick
Error Correction
ANSI X4.14-1971 standard typewriter keyboard
Audible feedback on each keystroke
Three-key rollover to reduce errors caused by fast typing

Special Keys
Extra control keys for special and commonly used control functions include ESC, TAB, SCROLL, BACKSPACE, BREAK, LINE FEED, RETURN, COPY, REPEAT

Auxiliary Keypad
Extra control keys for transmitting 2-character escape sequences and special character codes

User Controls

Intensity
Parity
Power/Logic Reset
Baud Rate/
Interface Mode
Variable to adjust character and graph brightness
Even or no parity, switch selectable; odd parity, jumper-selectable
Turns line voltage on and off and resets unit to Alphanumeric mode
Allows choice of baud rate, full duplex, full duplex with local copy, and local mode with rotary switches

Copier

Image Copied
Time/Print
Copy Size
Paper Roll Size
Character Format
Graph Field
User Controls
Display on screen less the alphanumeric cursor
Approximately 25 seconds/copy
Approximately 76.2 mm (3 in) high x 177.8 mm (7 in) wide
36.5 m (120 ft) long x 216 mm (8½ in) wide
7 x 7 dot matrix
512 points horizontal x 236 points vertical
Variable character width adjustment
MECHANICAL

Cabinet Dimensions

Height 36 cm (14.1 in)
Width 53 cm (20.9 in)
Depth 69 cm (27.2 in)
Minimum Table Depth 45 cm (17.7 in)

System Weight

With Copier 25.8 kg (57 lb)
Without Copier 22.2 kg (49 lb)

ENVIRONMENT

Temperature

Operating Environment

With Copier 15° to 32°C (58° to 90°F)
Without Copier 10° to 40°C (50° to 104°F)
Nonoperating —40° to 66°C (—40° to 151°F)

Humidity (Noncondensing)

Operating Environment

With Copier 20 to 80%
Without Copier 10 to 90%
Nonoperating 0 to 95%
ACOUSTIC TELEPHONE COUPLER, DF01-A

FEATURES
- Data rates up to 300 Baud
- Acoustic coupling
- TTY and EIA RS-232-C output
- Half- and full-duplex operation
- Integral acoustic shielding
- Impact-resistant case

The DF01-A acoustic coupler can be used to connect DIGITAL and other terminals to remote computing systems via ordinary telephone sets and the public switched telephone network.

Both 0-20 millampere teletype current loop and EIA RS-232-C interfaces are standard in the DF01-A.

Through slide switches, the user may choose either full- or half-duplex operation.

"Sound-seal" cushions on the DF01-A hold the telephone handset firmly in position and provide excellent acoustic shielding. Good durability is provided by an injection-molded case made of special impact-resistant material. All electronic circuitry, switches and connectors are mounted on a single printed circuit board.

SPECIFICATIONS
Operating Modes: Originate-only, in half- or full-duplex.
Data Rate: Up to 300 Baud.
Receiver Sensitivity: —35dBm in acoustic mode.
Frequencies:

<table>
<thead>
<tr>
<th></th>
<th>Send</th>
<th>Receive</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mark</td>
<td>1270 Hz</td>
<td>2225 Hz</td>
</tr>
<tr>
<td>Space</td>
<td>1070 Hz</td>
<td>2025 Hz</td>
</tr>
<tr>
<td>Frequency Stability:</td>
<td>0.3%</td>
<td>0.4%</td>
</tr>
</tbody>
</table>

Modulation Technique: Audio Frequency—Shift Keyed (AFSK)
Transmit Power Level: —21dBm ± 3dBm
Line Coupling: Acoustic coupling to telephone line.
Interface: 0 to 20 millampere teletype levels or EIA RS-232-C (both available on the same unit; both outputs can be used simultaneously if desired).
Compatibility:
Used with remote terminals (teleprinter, typewriter, CRT display, plotter, card reader) to provide information transfer to/from a Bell 103A2 (or
equivalent) dataset. CANNOT BE USED with 230V, 50 Hz, nor is it compatible with European modems.

**Power Requirement:** 115V, 60 Hz (less than 10W)

**Operating Temperature:** 32° to 140°F (0° to 60°C)

**Size:**
- Width 7.5" (18 cm)
- Height 3" (7.6 cm)
- Length 12" (30.4 cm)

**Weight:**
6 lbs. (2.72 Kg)

**Mounting:**
Tabletop case

**Controls and Indicators:**
- Power ON/OFF
- Full-Duplex/Half-Duplex (slide switch)
- Carrier ON indicator light

**Cables:** Supplied with 8 ft. (2.27 m) cable.

**Ordering Information:**

<table>
<thead>
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<th>OPTION</th>
<th>PREREQ.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF01-A</td>
<td>None</td>
<td>Acoustic Telephone Coupler</td>
</tr>
</tbody>
</table>

A cable may be ordered (DEC No. BC05D-25) to connect the DF01-A to EIA terminals already supplied with a cable.
16-LINE PROGRAMMABLE ASYNCHRONOUS SERIAL LINE MULTIPLEXER, DH11

Features
- Speed—Each line of the DH11 may run at program-selectable speeds up to 9600 Bauds.
- Flexibility—complete program control of each line for:
  - Data Rate—14 standard speeds, plus two external inputs
  - Character Size—5, 6, 7, or 8 bits
  - Stop Code Length—1, 1-1/2, (5-bit data only) or 2 bits
  - Transmission Mode—full-duplex, half-duplex or echo-plex
  - Parity generation and checking
• Program-controlled hardware echo of received characters
• 64-character hardware buffer for received characters
• DMA transmitter for each line, with byte count & address registers in hardware
• Split speed—transmitter and receiver of each line may run at different speeds
• Hardware break detection and program-controlled break generation
• Capacity—up to 256 lines per PDP-11

APPLICATIONS
The excellent price/performance ratio of the DH11 allows it to serve in many communications applications. These include remote concentrators, front-end preprocessors, and store and forward message switches. The DH11 interfaces to a variety of local and remote terminal types.

Line Concentrators
A cluster of remote low-speed data terminals can often be interfaced more economically to a remote interactive computer via a data concentrator than by using a separate line per terminal. Communication line costs can be reduced by concentrating several low-speed terminals into a single medium-speed communication line using a data concentrator. Typically, a data concentrator performs the following functions:

  Character-to-message assembly/disassembly
  Communication line control
  Message buffering
  Error control
  Code conversion
  Automatic answering

Front-End Processors
Front ends handle routine tasks for large central computers, such as message input-output to remote terminals and local and remote peripherals. They perform most of the functions of line concentrators, but are connected directly to the host processor.

Store-and-Forward Message Switches
This type of system has a number of data terminals connected locally or via communications lines to a central computer. Any terminal can originate a message and transmit it to the central computer. Here the message is stored until it can be forwarded to the destination terminal. Typical functions performed by a store-and-forward message switch are:

  Assembly/disassembly of messages
  Polling and addressing of terminals
  Line control
  Error control
  Code and speed conversion
  Message header analysis

* Except for DH11-AD and DH11-AE
Sequence number of messages
Time and date stamping of messages
Message routing

DESCRIPTION
The DH11 multiplexer connects the PDP-11 with 16 asynchronous serial communications lines operating with individually programmable parameters. These parameters are:

Character length: 5, 6, 7, or 8 bits
Number of stop bits: 1 or 2 for 6-, 7-, 8-bit characters
Parity generation and detection: Odd, Even, or None
Operating mode: Half Duplex or Full Duplex
Transmitter speed (Baud): 0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, Ext A, Ext B.
Receiver speed (Baud): 0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, Ext A, Ext B.

Breaks may be detected and generated on each line.

The DH11 Multiplexer uses 16 double-buffered MOS/LSI receivers to assemble the incoming characters. An automatic scanner takes each received character and the line number and deposits that information in a first-in, first-out buffer memory referred to as the “silo.” The bottom of the silo is a register which is addressable from the UNIBUS.

The transmitter in the DH11 also uses double-buffered MOS/LSI units. They are loaded directly from message tables in the PDP-11 memory by means of single cycle direct memory transfers (NPR). The current addresses and data byte counts for each line’s message table are stored in semi-conductor memories located in the DH11. This reduces the UNIBUS time required for NPR transfers to one NPR cycle per character transmitted.

As many as 16 DH11’s may be placed on a single PDP-11 processor, creating a total capacity of 256 lines.

Models Available
The DH11-AA consists of a double system unit, all modules necessary to implement a 16 line asynchronous multiplexer, an externally mounted 14 cm (5 1/4 inch) level conversion and distribution panel with its own power supply that can be mounted on the rear of the rack, and a data cable between the logic in the double system unit and the level conversion/distribution panel.
The modules for level conversion are not included, so that the type and quantity of lines may be customized to the customer's requirements.

The DH11-AC is the same as the DH11-AA, except that the power supply for the level conversion/distribution panel is arranged for 240 V, 50 Hz operation.

All of the above versions of the DH11 include pre-wired slots in the double system unit for the insertion of the DM11-BB modem control (not included in the basic DH11).

The DH11-AD consists of a double system unit, all modules necessary to implement a 16-line asynchronous multiplexer, including modem control (programming is same as DM11-BB programming), necessary level converters for EIA RS232-C interfacing and an externally mounted distribution panel. This is a self-contained unit for applications where line interfacing flexibility is not needed.

The DH11-AE is the same as the DH11-AD except it does not include modem control. Includes EIA level conversion for data leads only.

Operation-Receiver
Reception on each line is effected by means of Universal Asynchronous Receiver/Transmitters (UARTs). These are 40-pin MOS/LSI circuits which perform all the necessary functions for double buffered asynchronous character assembly.

The receiver section of the UART samples the line at 16 times the bit rate of the signals to be received on that line. Upon detection of a Mark-to-Space transition, the UART counts 8 clock pulses and checks the line. This sampling will occur in the center of a normal start bit. If the sample is a Mark, the receiver returns to its idling state, ready to detect another Mark-to-Space transition. If the sample is a Space, the receiver samples the line at subsequent sample points spaced 16 clock ticks from the center of the start bit. The number of samples taken is determined by the "character length" information entered into the UART via the Line Parameter Register. If parity checking has been enabled for this line, the receiver logic computes the parity of the character just received and compares it with the parity sense specified for reception on that line. If the parity sense differs, the parity error bit will be set.

The character length, parity sense, number of stop bits, etc. that will be used by the UART to perform the above operations are stored within
each UART in a Control Bits Holding Register. The Control Bits Holding Registers are addressable on a write-only basis from the UNIBUS, by first setting the "line selection bits" of the System Control Register and then loading the desired line parameters into the Line Parameter Register. Then they will automatically be transferred to the Control Bits Holding Register of the designated UART. It is important that no interrupt handling routine intervene and change the contents of the System Control Register during the above operation.

The Silo
The silo is a MOS/LSI digital storage buffer that is 16 bits wide and 64 words deep. A 16-bit word is entered at the top, and automatically shifted down to the lowest location that does not already contain an entry. The bottom of the silo is the Next Received Character Register.

There are three registers associated with the silo. The Next Received Character Register is a read-once register and is the bottom of the silo. Reading it extracts a character from the silo and causes all other entries to shift down one more position.

The other two registers are byte-size registers and are contained within the Silo Status Register. The high byte is read only and contains the status of an up-down counter giving the actual fill level of the silo. The low byte (bits 7-0) is read/write, and contains the number of characters which must be loaded into the silo before an interrupt request will be generated. Details of these registers can be found in the Section on Programming under the heading "Silo."

Received Character Distortion
Received characters may contain up to 43.75% distortion on any bit, due to the sampling rate. However, the overall bit rate must be accurate. Specifically, errors in bit rate are cumulative such that when the receiver samples the first stop bit to see if it is a mark (if not, it's a "framing error") the error accumulated by that time must not exceed 43.75% of a bit time. The accumulated error (called "gross start-stop distortion") is calculated as clock error x number of data bits plus one, plus the bias distortion of the final character. Assuming the reception of eight data bits, or seven data bits plus parity, 4.8% speed distortion would be permissible. Speed distortion (clock error, bit rate error) of any amount poses severe problems in an echo situation, however. If a terminal sends to the DH11 at a slightly fast rate and the DH11 sends the exact same characters back to the terminal at the correct rate, the DH11 silo will eventually fill with un-echoed characters. This problem would not occur with keyboard terminals, but high speed tape senders should have their transmission speeds carefully checked before use with the DH11 or any other asynchronous communications interface. The acceptable tolerance is ± 0. - 4%. In computing speeds, one may assume the DH11 receiver clock to be accurate within .05%.
Operation-Transmitter
Transmission on each line is also effected by means of UARTs. These 40-pin MOS/LSI chips perform all the necessary functions for double-buffered asynchronous character transmission. The transmitter section of the UART holds the serial output line at a Marking state when idle. When the transmitter loading leads have been conditioned with the character to be transmitted and the data strobe lead has been brought high (these functions are performed by the NPR control), the UART will generate a start space within one sixteenth of a bit time. The start space and all subsequent data bits are a full bit time each. The start space is followed by 5, 6, 7, or 8 data bits, as determined by the control bits holding register. (See Receiver Hardware for a description of the UART control bits holding registers and how they are loaded from the Line Parameter Register). The data bits are presented to the lines least significant bit first. The parity bit, if parity generation is enabled, is calculated by the transmitter and affixed after the last data bit, but before the stop marks.

The number of stop bits depends upon the setting of the control word. If the transmission of 6, 7, or 8 bits has been selected, the program may select either one or two stop bits. If the transmission is in 5-bit code, the program may select either one or one and a half stop bits.

If the transmitter's holding register has been loaded while a character was being transmitted, that second character will have its start bit commence immediately at the end of the preceding character's stop bit(s).

The transmitter timing circuit is driven by the same crystal clock as the receiver, and is accurate to .05%.

The Auto-Echo Feature
The DH11 hardware is capable of echoing received characters without software intervention. The feature may be enabled on any line by conditioning the line selection bits in the System Control Register and then setting the appropriate bits in the Line Parameter Register.

The auto-echo hardware is part of the receiver scanner and operates as follows:

1) If the receiver scanner finds a received character for a line on which auto-echo is NOT enabled, it loads that character into the silo and resumes scanning.

2) If the receiver scanner finds a received character for a line on which auto-echo IS enabled, it examines the error flags associated with that character.

a) If a framing error is detected, the remote terminal may be trying to gain the attention of the processor by sending a "Break." In this case, the auto-echo hardware dumps the received character and associated flag into the silo so that the system software will be alerted. The Break is not echoed to the remote terminal.
b) If an overrun error is detected, this may mean that the remote terminal is trying to gain the attention of the processor by typing characters. This case is treated identically to 2a.

3) If the receiver scanner finds a received character from a line upon which auto-echo is enabled and there are no error flags of the type mentioned above, the receiver scanner and auto-echo logic will attempt to echo the character. First, however, certain tests of internal logic conditions will be made.

a) The UART transmitters are all loaded from a common internal data bus. Therefore, the auto-echo hardware must first check to see that no NPR cycles are in progress loading a UART transmitter from that bus. If a conflict is indicated, the receiver scanner is restarted and the process will be tried again on the scanner's next rotation.

b) If the above test indicates no problem, the one remaining check is to see if the Transmitter Holding Register for the line on which the character was received is available. If it is not, the scanner is restarted. If it is available, auto-echo commences.

It should be noted that it is not advisable to transmit messages on a line and auto-echo characters received on that line simultaneously. The auto-echo hardware will interlock these functions to some degree, but if more than two characters are received on a line while the scanner is waiting for the transmitter holding buffer to become available, a data overrun will occur and characters will be lost. In short, auto-echo and software-driven transmission should not be attempted on the same line simultaneously if input from that line is expected.

**SILO INTERRUPT HANDLING**

The DH11 provides increased received character throughput by averaging the received character interrupt routine entry/exit time over a number of received characters. If it takes 30 microseconds to enter and exit an interrupt routine and 30 microseconds to process a character, the average time per character in a conventional character interrupt device would be 60 microseconds. If it takes 30 microseconds to enter and exit an interrupt routine and 960 microseconds to process 32 characters in a silo, the average time per character in a DH11 would be 31 microseconds or roughly half that of a conventional device.

The above example of increased throughput suggests that the DH11 received character silo alarm level be set at 32. Certain cautions should be observed in doing this in an interactive system, however. Specifically, a real time clock should be used to insure that terminal users receive a response within a guaranteed maximum time interval. The operating program would service the silo whenever the alarm occurred or the clock ticked, whichever came first.

Alternately, the alarm level can be set at zero and still obtain many of the advantages of silo operation. Obviously, the silo permits a high de-
gree of latency by storing received characters whenever the operating program is unable to service the silo due to demands of other devices. Furthermore, when the operating program does service the silo there will be a great many characters stored there and the interrupt averaging effect described earlier will be used to full advantage. Thus the silo helps throughput the most in those situations when the most help is needed.

DMA Transmission

In a DMA transfer system, a computer peripheral, such as the DH11, obtains data from (or deposits data in) computer memory without the aid of the computer processor. This process is commonly called Direct Memory Access (DMA), although in the case of a PDP-11, it is referred to as a Non-Processor Request (NPR).

All that is required from a programming standpoint to perform NPR's is an indication of which memory location is desired, whether one wishes to read from that location or write into it, and to how many consecutive memory locations one wishes access.

For example, if one wished to transmit the letters A, B, C from computer memory to some distant location, one would prepare a message table in memory:

00 000 000 11 000 011 (Location 5002)
11 000 010 11 000 001 (Location 5000)

In this example, a sixteen bit PDP-11 word is shown containing two eight bit “bytes”. The byte at location 5000 is the ASCII code for “A”. The byte at location 5001 is the ASCII code for “B”. (Note that the odd numbered locations are the left hand byte of the even numbered locations.) Finally, the byte at location 5002 is an ASCII “C”. The all-zeroes byte at location 5003 is not to be sent.

In the DH11 or a similar device, one would load the transmitter “current address” register for the appropriate line with “5000” and the transmitted “byte count” register with “−3”. Then one should set the BAR bit for the line on which transmission is to occur. The DH11 hardware would gain control of the Unibus, read the 11 000 001 from location 5000, transmit the “A”, increment the current address to 5001, increment the byte count to -2, wait for the “A” to finish going out onto the line and then repeat this process. The process would continue until the byte count was incremented to “zero” and would then stop. It is because “zero” is an easy number for computer hardware to recognize that byte counts are usually loaded as negative quantities by the program and up-counted to zero by the hardware.

In the DH11, any memory location, including those with extended addresses may be used and message tables can cross extended address boundaries if desired. Any message length up to 32,768 bytes may be transmitted.
Since no processor action is required for each character transferred by the NPR cycles, a very high data transfer rate is possible if message lengths are long enough to make the program time necessary to load the current address and byte count small relative to the number of characters transmitted.

Modem Control Multiplexer DM11-BB
In cases where the DH11 is used in public switched networks such as DDD, or TWX, the modem control multiplexer DM11-BB should be used. The control multiplexer provides the necessary control leads to interface with the Bell 103 and 202 type modems or equivalent. All leads meet EIA RS-232-C and CCITT electrical specifications. The DM11-BB is not required with the DH11-AD and cannot be used with the DH11-AE.

Channel Interfaces
Multiplexer Distribution Panel and Power Supply for DH11-AA, AC.

The DH11 provides a panel for level conversion and cabling of the individual lines. The panel uses a standard H911 style rack, with 6 connector blocks.

Note that the slot assignments follow the DF11 (standard level conversion and cable slot for all PDP-11 communications products) format. Slot A6 through A21 is used for level conversion and slot B6 through B21 is used for cabling out. Other slots provide inputs or special purpose outputs. The unit mounts on the standard 48.3 cm (19 in.) cabinet and connects to the PDP-11 via the BC08-S data cable.

Power for the distribution panel is provided by the H751-C power supply mounted on the rear door of the cabinet.

The H751-C provides the following voltages:

- + 5 V at 4 A
- + 15 V at 2 A
- — 15 V at 2 A
**LEVEL CONVERSION OF CONTROL LEADS. ONE SLOT PER LINE. USE M594 ONLY WHEN DM11-BB IS IMPLEMENTED. IF DM11-DB IS USED REPLACE M594 WITH W404-A (SUPPLIED WITH DM11-DB). IF DM11-DA IS USED LEAVE BLANK.**

**USE M594 FOR DM11-DB**

**USE M596 FOR DM11-DA**

*USE ONLY IF DM11-BB IS IMPLEMENTED*

**DATA CABLE FROM DH11-AA CONTROL LOGIC**

▲16 CABLE SLOTS ONE PER LINE FOR DM11-DA USE M973, FOR DM11-DB USE BCDIR-25

▲▲JUMPER CARD USED FOR DIAGNOSTIC PROGRAMS ONLY, REMOVE FOR NORMAL OPERATION.
Power drain of the distribution panel depends on the type of level conversion used. The maximum draw occurs when EIA levels are used with modem control (DM11-BB is implemented).

For this configuration the following power is used:

\[
\begin{align*}
+ & \ 15 \text{ V at } 1.4 \text{ A} \\
- & \ 15 \text{ V at } 1.4 \text{ A} \\
+ & \ 5 \text{ V at } 1.7 \text{ A}
\end{align*}
\]

Note that level converter types can be mixed on a 4-line basis by using different converters in slots A4, A5, B4 and B5. Also level converter types can be mixed on a single line basis by using slots A6 through A21 for level conversion on a single-line basis.

**Programming**

**Double-Buffered Receivers—General**

Double-buffered receivers contain two registers, one of which is a Shift Register. The character being received from the communications line is shifted into this register a bit at a time. The second register is a Holding Register. When the Shift Register has assembled a complete character, that character is transferred in a parallel fashion into the Holding Register. At that time a flag is set and the hardware or software using the double-buffered receiver can access the Holding Register and remove or copy the data stored there. When the Shift Register has assembled another character, that character will be transferred into the Holding Register, obliterating the character previously stored there. If this action takes place before the data in the Holding Register has been accessed, a Data Overrun flag will be set, indicating that data was lost.

**Double-Buffered Receivers—DH11**

The UARTs used in the DH11 are MOS/LSI units, each containing a double-buffered receiver and a double-buffered transmitter. In the DH11, the flags indicating presence of data in the receiver's Holding Registers are scanned by an automatic hardware scanner which copies data from the Holding Registers into the silo if storage space is available. (If that space is not available, and the scanner finds a flag indicating a holding register with data in it, the Storage Overflow bit (System Control Register, bit 14) is set, and an interrupt is generated. The setting of this bit does not necessarily mean that data has been lost. Rather, it indicates that data will be lost if the hardware scanner is unable to service (i.e., dump into the silo) the data in one or more Holding Registers before additional characters arrive on those lines. Actual data loss will become evident to the program when characters are received with the Data Overrun bit set. (See the description of the Next Received Character Register.)

**Silo**

The silo, actually more similar in operation to a granary, is a first-in first-out buffer store. A parallel-loaded 16-bit word (see Next Received Character Register for the format) automatically propagates downward into
the first location not already containing a word. In the case where the silo is empty, this means that the word would propagate directly into the Next Received Character Register.

The propagation time from the top of the silo to the bottom may be as much as 32 microseconds. For this reason, the hardware is arranged such that the Receiver Interrupt is not generated until the number of characters in the silo exceeds the silo alarm level AND there is at least one character in the bottom of the silo. This arrangement is necessary because the up-down counter that indicates the number of characters in the silo counts both those resting in the bottom and those propagating downward. While the hardware arrangement protects the case where the silo is empty and the alarm level is zero, the fact still remains that the number of characters in the silo and the number actually available to be serviced may differ due to the propagation time. For this reason, character handling programs should not assume there is some particular number of characters in the silo when servicing begins. Rather, the program should extract a character, check the Valid Data Present bit (bit 15) and handle the character; then the program should extract the next character and repeat the process until bit 15 no longer tests as "1." At that time, the silo may be assumed to be empty (although there may be another character propagating downward) and the character handling routine may be terminated until another Receiver Interrupt is received.

On very fast processors, such as the PDP-11/45 and PDP-11/70, the program should avoid reading the Next Received Character Register more often than once per microsecond, as it takes one microsecond for characters in the silo to shift downward one position. Since the typical program will be checking bit 15 and moving the character to some location in memory, it is not anticipated that this speed restriction will present a problem.

Zero Bauds
A speed selection of zero bauds is provided so that the program may turn off any line. This is useful if excessive circuit noise on an unused line causes annoying quantities of bogus characters.

BREAK Signals
When the Break Control Register has been conditioned to transmit a break signal on a particular line, DH11 logic immediately forces the output on that line to the SPACE (0) condition. The duration of this signal may be timed as described below.

The generation of a Transmitter Interrupt occurs when the last character of a message is loaded into a UART transmitter from a message table in PDP-11 core. At that time the program sets up a new message in core and loads the appropriate current address and byte count so that the new message can begin when the old one is finished.

It is important to note that the former message is not finished when the Transmitter Interrupt is given. Rather, the use of the core table is finished. In terms of the serial communications line, there are two more
characters left. One of these characters is in the UART transmitter’s Shift Register; the other is in the UART transmitter’s Holding Register.

Therefore, sending a Break signal requires loading two nulls and waiting for a transmitter interrupt before setting the appropriate bit in the Break Control Register. In this way, generation of a Break will not interrupt the transmission of any valid characters. In like manner, nulls should be used to time the transmission of a Break signal so that when the Break condition is terminated, no valid characters will be produced from the UART Shift and Holding Registers.

**Interrupts**

There are two kinds of receiver interrupts:

**Receiver Interrupt (System Control Register, bit 7)**

This interrupt, when enabled, occurs whenever the number of entries in the silo exceeds the silo status alarm level. (The program can determine the actual silo fill at any time by examining the high byte of the Silo Status Register.)

**Storage Overflow Interrupt (System Control Register, bit 14)**

This interrupt, when enabled, occurs whenever the character storage silo is full and the DH11 hardware needs to store an additional character. This does not necessarily mean that data has been lost. (See the section on “Programming.”)

There are two kinds of transmitter interrupts; both are enabled by bit 13 of the System Control Register:

**Transmitter Interrupt (System Control Register, bit 15)**

This interrupt, if enabled, occurs when one or more lines finish the transmission of a complete string of characters. Specifically, it occurs after the NPR cycle that loads the last character to be transmitted (and hence that increments the byte count to zero).

**Non-Existential Memory Interrupt (System Control Register bit 10).**

This interrupt, when enabled, occurs whenever the DH11 addresses non-existent memory; specifically, this interrupt occurs if the DH11 enters an NPR cycle, places an address on the Unibus, and fails to receive a slave sync response for that request within 20 microseconds.

**Address and Vector Assignment**

The DH11 uses floating addresses and is located after DJ11’s in the floating address space that begins at location 760 010. Because the DH11 has eight registers, it must be assigned an address that is a multiple of 20 (octal). All DH11’s in a system should have consecutive addresses.

Example #1: A system with no DJ11’s but two DH11’s:

760 010 Cannot use for DH11’s because not multiple of 20.
DH11

760 020  First DH11
760 040  Second DH11
760 060  DH11 Gap (Indicates that there are no more DH11’s).

Example #2: A system with one DJ11, two DH11’s:

760 010  First DJ11
760 020  DJ11 Gap (Indicates that there are no more DJ11’s).
760 030  Cannot use for DH11’s because not multiple of 20.
760 040  First DH11
760 060  Second DH11
760 100  DH11 Gap (Indicates that there are no more DH11’s).

The DH11 vectors (2) follow those of the DJ11 in the floating vector space that starts at address 300. The vectors starting at 300 are used in the following order: DC11; DL11-WA/DL11-A; DL11-WB/DL11-B; DP11; DN11; DM11-BB; DR11-C; PA611 Readers; PA611 Punches; DT11; DX11; DL11-C, D, E; DJ11; DH11.

The receiver vector is the lower numbered vector. The priority of the receiver and transmitter interrupts are individually selectable by means of two standard PDP-11 priority jumper plugs. BR level 5 is standard.

Register Definition

The following chart presents the bit assignments within each register. Bits marked Unused and Write Only are always read as zero. Attempting to write into Unused or Read Only bits has no effect on those bits. INIT refers to the Initialize signal generated by the processor (e.g., upon execution of a RESET instruction.) Transmit and Receive are with respect to the DH11. All bits in the accompanying diagrams are shown in the state they assume on POWER CLEAR or INIT.

The System Control Register—Address X00

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The System Control Register is a byte-addressable register. The bit assignment is as follows:

BITS DESCRIPTION

00-03  Line Selection

Each of the 16 lines served by the DH11 has its own storage for line parameter information, current address, and byte count. These storage locations are loaded by the program via the Line Parameter Register, Current Address Register, and Byte Count Register, but the hardware must first be told which line is to have its line parameters, current address, or byte count changed. This routing is accomplished by setting the Line Selection bits to the binary address (0000-1111) of the desired line. These bits are read/write.

2-50
04, 05 Memory Extension
The information stored in these bits becomes bits 16 and 17 respectively of any current address loaded by the program into the Current Address Register. These bits are read/write but, when read, represent only the status of bits 4 and 5 of the System Control Register, NOT the status of address bits 16 and 17 of the selected line. See the Silo Status Register for further information. This arrangement permits interrupt service routines to save the contents of the System Control Register accurately.

06 Receiver Interrupt Enable
This bit, when set, enables receiver interrupts (bit 7)

07 Receiver Interrupt
This bit, when set, indicates that the number of characters stored in the silo exceeds the "alarm level" specified by the low byte of the Silo Status Register. This bit is read only, except in maintenance mode, where it is read/write. Setting of this bit will generate an interrupt request if bit 6 (above) is also set.

08 Clear Non-Existent Memory Interrupt
This bit, when set, clears the non-existent memory interrupt flip-flop (bit 10) and clears itself. This bit is read/write.

09 Maintenance
This bit, when set, places the DH11 in maintenance mode.

10 Non-Existent Memory
This bit is set whenever the NPR hardware places the addresses of a memory location on the UNIBUS and no slave sync is received in 20 \( \mu s \). This indicates that the addressed location or device does not exist. This bit causes an interrupt request if set while Transmitter and Non-Existent Memory Interrupt Enable is set. This bit is read only, except in maintenance mode, where it is read/write.

11 Master Clear
This bit, when set, generates "Initialize" within the DH11, clearing the silo, the UARTs, and the registers. The exact bits cleared are discussed in the section on initialization. Read/Write.

12 Storage Interrupt Enable
This bit, when set, permits the setting of bit 14 to generate an interrupt request. This bit is read/write.

13 Transmitter and Non-Ex-Mem Interrupt Enable
This bit, when set, permits the setting of bit 10 or 15 to generate an interrupt request. This bit is read/write.

14 Storage Interrupt
This bit is set when the receiver scanner finds a receiver holding buffer with a character in it, tries to store that character in the silo, and cannot do so because of a lack of space. When set this
bit will cause an interrupt request if bit 12 is set. This bit is read only, except in Maintenance Mode, where it is read/write.

15 Transmitter Interrupt
This bit is set when the DH11 concludes an NPR cycle that incremented a byte count to zero, indicating the last character in a message buffer was loaded into a UART transmitter Holding Register. This bit will cause an interrupt request if bit 13 is set. This bit is read/write. (It is set during an NPR cycle.)

Next Received Character Register Address X02

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
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<td>00</td>
<td>00</td>
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<td>00</td>
</tr>
</tbody>
</table>

RECEIVED DATA   RECEIVED DATA PARITY ERROR   OVERRUN
LINE NUMBER     FRAMING ERROR
DATA PRESENT

BITS DESCRIPTION

00-07 Next Received Character
These bits contain the next received character, right justified. The least significant bit is bit 00.

08-11 Line Number
These bits indicate the line number on which the next received character was received. Bit 8 is the least significant bit.

12 Parity Error
This bit is set if the parity of the received character does not agree with that designated for that line.

13 Framing Error
This bit is set if the receiver samples a line for the first stop bit, and finds the line in a spacing condition (logical 0). This condition usually indicates the reception of a Break.

14 Data Overrun
This bit is set when the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer. Refer to the section on Programming for further details on double-buffered reception.

15 Valid Data Present
This bit indicates that the data presented in bits 14-00 is valid. It permits a character handling program to take characters from the silo until it is empty. This is done by reading this register and checking bit 15 until a word is obtained for which bit 15 is a zero.
The entire Next Received Character Register is read-only and is addressable only on a word basis.

Line Parameter Register  Address X04

This register should be loaded only after the line selection bits of the System Control Register have been set to select the line to which these parameters apply. This register is write only.

**BITS**  **DESCRIPTION**

00-01  **Character Length**

These bits should be set as shown to receive and transmit characters of the length (excluding parity) shown:

<table>
<thead>
<tr>
<th>bit</th>
<th>01 00</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>5 bit</td>
</tr>
<tr>
<td>0 1</td>
<td>6 bit</td>
</tr>
<tr>
<td>1 0</td>
<td>7 bit</td>
</tr>
<tr>
<td>1 1</td>
<td>8 bit</td>
</tr>
</tbody>
</table>

02  **Two Stop Bits**

This bit, when set, conditions a line transmitting with 6-, 7-, or 8-bit code to transmit characters having two stop marks. If the line is transmitting 5-bit code, assertion of this bit causes the characters to be transmitted with 1.5 stop marks. If this bit is not asserted, 1 stop mark is sent.

03  **Not Used.**

04  **Parity Enabled**

If this bit is set, characters transmitted on this line will have an appropriate parity bit affixed, and characters received on this line will have their parity checked.

05  **Odd Parity**

If this bit and bit 4 are set, characters of odd parity will be generated on this line and incoming characters will be expected to have odd parity. If this bit is not set, but bit 4 is set, characters of even parity will be generated on this line and incoming characters will be expected to have even parity. If bit 4 is not set, the setting of this bit is immaterial.

06-09  **Receiver Speed**

The state of these bits determines the operating speed for this line's receiver. The speed table below is applicable.
10-13 Transmitter Speed

The state of these bits determines the operating speed for this line’s transmitter. The speed table below is applicable.

Speed Table for Receiver and Transmitter Speeds:

<table>
<thead>
<tr>
<th>Bit</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
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<td>9</td>
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</tbody>
</table>

14 Half Duplex/Full Duplex

If this bit is set, this line will operate in half-duplex mode. If not set, this line will operate in full-duplex mode.

In this application half-duplex means that the DH11 receiver is blinded during transmission of a character.

15 Auto-Echo Enable

When this bit is set, characters received on this line will be hardware echoed. See the discussion of Auto-Echo for further details.

Current Address Register Address X06

This register should be loaded only after the System Control Register (SCR) has had the appropriate bits set to select the desired line number. When this register is loaded, address bits 00-15 are transferred into semiconductor memories in the DH11 from bits 00-15 of this register. Address bits 16-17 are transferred into semiconductor memories in the DH11 from bits 4-5 of the System Control Register.

2-54
Interrupts must be inhibited or the SCR saved between the setting of the SCR bits 0-3 and the read or write of the Current Address Register.

When this register is read, it will indicate the current address of the line selected by the System Control Register. Bits 16 and 17 will appear in the Silo Status Register, bits 6 and 7.

**Byte Count Register**  Address X10

In the same fashion as the Line Parameter and Current Address registers, this register should not be loaded or read without first selecting a line number by means of the lower-order four bits of the System Control Register. This register should be loaded with the two’s complement of the number of characters (bytes) to be transmitted on that line. The byte count register is read/write.

Interrupts must be inhibited or the SCR saved between the setting of the SCR bits 0-3 and the read or write of the Byte Count Register.

**Buffer Active Register (BAR)**  Address X12

![Diagram of Buffer Active Register (BAR)]

This register contains one bit for each line. The bits are individually set using BIS instructions. Setting a bit initiates transmission on the associated line. The bit is cleared by the hardware when the last character to be transmitted is loaded into the transmitter Data Holding Register of the UART for that line. It should be noted that while the clearing of a BAR does indicate that a message may be sent, it does not indicate that the last characters from the preceding message have been completely sent. Specifically, two more characters will be sent after the BAR bit clears. These are the last two characters of the message; one of them was just starting when the BAR was cleared and one was that final character that was loaded into the holding register, thus clearing the BAR bit. This effect is a normal consequence of double-buffered transmission and is mentioned here for the benefit of programmers who want to write programs that control such modem leads as Request to Send. Request to Send (RTS) should not be dropped until at least two character times after the BAR bit for a given line clears.

This timing may be effected by sending two extra (null) characters in a message and dropping RTS when BAR clears.

Clearing a BAR bit should not be used to abort transmission on a line. Rather, the byte count for that line should be set to zero. The Buffer Active Register bits are read/write.
Break Control Register  Address X14

This register contains one bit for each line. Setting a bit in this register will immediately generate a Break condition on the line corresponding to that bit number. Clearing the bit will terminate the Break condition. The Break condition may be timed by sending characters during the Break interval, since these characters will never actually reach the line. Further comments concerning the transmission of Break signals may be found in the Break Signals Section.

Silo Status Register  Address X16

00-05  Silo Alarm Level

The program may load an integral power of 2 between 0 and 63 into this location (e.g., 0, 1, 2, 4, 8, 16 or 32). When the number of characters stored in the silo exceeds that number, an interrupt request (System Control Register bit 7) is generated, if System Control Register bit 6 is set. These bits are read/write.

**NOTE:**

On silo alarm settings above 8, two interrupts will occur. The first interrupt occurs when silo exceeds alarm level, and the second interrupt occurs when the silo is unloaded. Software should take account of this fact.

06-07  Read Extended Memory

These bits are read only and contain the A16 and A17 bits of the current line address to which the line selection bits of the System Control Register are pointing.

08-13  Silo Fill Level

These bits are an up-down counter that indicates the actual number of characters in the silo. It should be noted that there are six bits, hence numbers between 0 and 63 can be represented. A full silo has 64 entries and the fill level appears as 000000, but one may easily tell the difference between an empty silo (000000) and a full silo (000000) by checking the Storage Overflow bit (bit 14 of System Control). These bits are read only.
Unused

Reserved for Maintenance

**MODEM CONTROL MULTIPLEXER DM11-BB**

In cases where the DH11 is used in public switched networks such as DDD, or TWX, the modem control multiplexer DM11-BB should be used. The control multiplexer provides the necessary control leads to interface with the Bell 103 and 202 type modems or equivalent. All leads meet EIA RS-232-C and CCITT electrical specifications.

**DM11-BB Modem Control Option**

Each DM11-BB modem control multiplexer contains two registers and requires two addresses. Address space has been assigned for 16 DM11-BB modem control multiplexers. The first DM11-BB is at 770500. The second starts at 770510, etc. to the 16th at 770670. The two registers and their addresses are listed below for DM11-BB unit xx.

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control and Status Register</td>
<td>770xx0</td>
</tr>
<tr>
<td>Line Status Register</td>
<td>770xx2</td>
</tr>
</tbody>
</table>

Each DM11-BB requires one interrupt vector. The vector addresses are assigned from 300 to 777.

All units are shipped with the bus request line set to BR4.

**Control and Status Register (770XX0)**

<table>
<thead>
<tr>
<th>BIT</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>Ring Flag</td>
<td>When DONE is set, this flag indicates that a Ring OFF to ON transition has been detected at line #--. This bit is read only and is cleared by Initialize and Clear Scan.</td>
</tr>
<tr>
<td>14</td>
<td>Carrier Flag</td>
<td>When DONE is set, this flag indicates that a Carrier Flag transition has been detected at line #--. This bit is read only and cleared by Initialize and Clear Scan.</td>
</tr>
<tr>
<td>13</td>
<td>Clear to Send</td>
<td>When DONE is set, this flag indicates that a Clear to Send transition has been detected at line #--. This bit is read only and cleared by Initialize and Clear Scan.</td>
</tr>
<tr>
<td>12</td>
<td>Secondary Receive Flag</td>
<td>When DONE is set, this flag indicates that a Secondary Receive transition has been detected at line #--. This bit is read only and cleared by Initialize and Clear Scan.</td>
</tr>
<tr>
<td>11</td>
<td>Clear Scan</td>
<td>Clears all Read/Write functions. Additionally, the Scan Decoder is set to 0 and the Scan Memory Logic is cleared. This function is useful for having</td>
</tr>
</tbody>
</table>
The Hardware Test and Interrupt on all lines that have an On condition (CO, CS, Sec T). Clear occurs when a ONE is written into this bit position.

Clear Multiplexer clears the request to Send, Terminal Ready, Secondary Transmit, and Line Enable flip flops when a ONE is written into this bit position.

The Scan Input (Ring, Clear to Send, Carrier, and Sec Rx) to a ONE or ON state Utilizing Step or SCAN EN with MAINT MODE will exercise 100% of the Scan Logic (not the data multiplexers). This includes the Interrupt Circuits (M7820) and the Address Selector (M105). This mode provides a diagnostic feature, as well as an on line test facility for the DM11-BB’s interaction with the Unibus. This bit is Read/Write and cleared by Initialize and by Clear Scan.

STEP, when set to a ONE, causes the Scan to increment the Line Number and test that line for interrupts causing transitions. Step may be used in place of Scan Enable but care should be exercised that the Scan rate is great enough (milliseconds) such that double carrier transitions will be detected. Additionally, DONE does not inhibit STEP. A STEP requires 1 μsec ± 10% to execute. This bit is Write One’s only.

The DONE flag set to a ONE indicates that the hardware SCAN has detected a transition requiring an Interrupt to the program. An Interrupt will occur if Interrupt Enable is on (a ONE). Additionally, DONE set to a ONE inhibits the SCAN clock and makes available to the programmer: (a) the Line Number that caused the Interrupt; (b) the status of the flags (4 bits); (c) modem status (8 bits). The SCAN will be released again when DONE is reset. This bit is Read/Write and cleared by Initialize and Clear Scan.

Allow Interrupts on Priority four if set to a ONE. This bit is Read/Write and cleared by Initialize and Clear Scan.

A ONE allows the scan to test all lines for Ring, Carrier, Clear to Send, and Sec. Receive Interrupts. If the SCAN EN flip flop is negated while the Ring Counter is cycling (i.e., DONE not set), the Ring Counter will come to rest in 1 μsec.
### DH11

<table>
<thead>
<tr>
<th>BIT</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>± 10% (max). The LINE register must not be changed until BUSY (Bit 4) is cleared, or line number transitions may be lost. This bit is Read/Write and cleared by Initialize and Clear Scan.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>BUSY</td>
<td>Set when Scan is cycling, Reset at end of Clear Scan or Init. Read Only. Must be tested for 0 before changing the registers.</td>
</tr>
<tr>
<td>3-0</td>
<td>Line Number</td>
<td>The LINE NUMBER bits are the Binary Addresses for the DM11-BB's 16 lines (0-15) as follows:</td>
</tr>
<tr>
<td></td>
<td>Bit 3210</td>
<td>Line #</td>
</tr>
<tr>
<td></td>
<td>0000</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0001</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>etc</td>
<td>etc</td>
</tr>
<tr>
<td></td>
<td>1111</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If the Scan is cleared by Initialize or Clear Scan, the Line Number Register will settle in 16 μsec 10%. When settled, the Line Number Register will be set to Line #0 (0000). NOTE: When the Scan is Enabled (or STEP) the next line to be tested will always be Line #1. These bits are Read/Write and cleared by Initialize and Clear Scan.</td>
</tr>
</tbody>
</table>

### Line Status (770XX2)

<table>
<thead>
<tr>
<th>BIT</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Ring</td>
<td>Modem status of the Ring lead. This bit is Read Only.</td>
</tr>
<tr>
<td>6</td>
<td>Carrier</td>
<td>Modem status of the Carrier lead. This bit is Read Only.</td>
</tr>
<tr>
<td>5</td>
<td>Clear to Send</td>
<td>Modem status of the Clear to Send lead. This bit is Read Only.</td>
</tr>
<tr>
<td>4</td>
<td>Secondary Receive</td>
<td>Modem status of the Secondary Receive lead. This bit is Read Only.</td>
</tr>
<tr>
<td>3</td>
<td>Secondary Transmit</td>
<td>When set, presents a MARK to the modem's Secondary Transmit lead. This lead is Read/Write and is cleared by Initialize and Clear Mux.</td>
</tr>
<tr>
<td>2</td>
<td>Request to Send</td>
<td>This lead is used to condition the modem to transmit if all other conditions are met. This bit is Read/Write and cleared by Initialize and Clear Mux.</td>
</tr>
<tr>
<td>1</td>
<td>Data Terminal Ready</td>
<td>This lead allows the modem to enter and maintain data mode. This bit is Read/Write and cleared by Initialize and Clear Mux.</td>
</tr>
</tbody>
</table>

2-59
0 Line Enable
This bit enables the state of Ring, Carrier, Clear to Send and Sec Rx to be sampled by the program and to be tested for transitions. This bit is Read/Write and cleared by Initialize and Clear Mux.

Maintenance Bits and Their Function
Setting of SCR 09 (Maintenance) does the following:

1.) It enables the program to write SCR07 (Receiver Interrupt), SCR 10 (Non-Ex-Memory Interrupt), and SCR 14 (Storage Overflow Interrupt) bits. This write capability is normally not enabled as it can produce hardware/software synchronization problems unless carefully done.

2.) It loops the Transmitted Data leads (Serial Out, line 00-15) to the Received Data leads (Serial In, line 00-15).

Setting of Silo Status Register 15 (Silo Maintenance):
The setting of bit 15 in SSR causes the inputs of the silo to be set to a 1010101010101010 bit pattern, and a single 16-bit character made up of this pattern to be loaded into the silo. Successive clears and sets of SSR 15 will repeat this procedure. All receiver speeds should be set to 0 and the silo emptied before this is done, so that no data from the incoming serial lines will be placed in the silo while it is under test.

Specifications
Function: The DH11 is a program-controlled interface between the PDP-11 UNIBUS and 16 asynchronous bit serial communications channels. The DH11 receiver section provides conversion of binary serial asynchronous (start-stop) signals to parallel binary data, and temporary buffering of that data. The DH11 transmitter section provides retrieval of parallel binary data from PDP-11 memory and conversion of that data to binary serial asynchronous (start-stop) signals for transmission over data communications channels.

Operating Modes: Each individual channel may be set to operate in half- or full-duplex mode, under program control. In half-duplex, the receiver for a channel is disabled during transmission of a character on that channel.

Any individual channel may be set, under program control, to echo (retransmit) received characters automatically.
Individual receivers may be continuously disabled under program control.

Data Format: Asynchronous, serial-by-bit to/from the communications channel. Parallel-by-character to/from the UNIBUS. The serial data format is one start bit; 5, 6, 7, or 8 data bits; none or 1 parity bit (odd or even); and 1, 1 1/2 (5 level codes only), or 2 stop bits per character. All data format parameters are individually program selectable for each channel. The data format for the receiver and transmitter on a given channel, however, is the same.

A one in any bit of a character presented by the program to the DH11 for transmission will cause a Marking (logical 1) condition to appear on the Transmitted Data lead during the corresponding bit interval. A zero presented by the program will cause a Spacing (logical 0) condition to appear. A Marking condition on the Received Data lead during any data bit sampling interval will be presented to the program as a one in the Next Received Character Register, and a Spacing condition will be presented as a zero.

Order of Bit Transmission and Reception: Low order bit first

Data Rates: The operating data rate (Baud rate) of the receiver and transmitter on each channel is independently program selectable from among the following 14 rates:

0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, and 9600 Baud. In addition, any two other speeds between 40 and 110 Baud, and between 312.5 and 9600 Baud may be added as options, by ordering an M405 or M401 clock module at the proper frequency (desired bit rate x 16).

Distortion: The DH11 receiver will operate properly in the presence of up to 43% distortion between any two code elements (intersymbol distortion). The long term (within any one character) speed variation of the received data may not exceed ± 4.3%, provided that the auto-echo feature is not used. If auto-echo is used, the long term (greater than one character time) speed variation of the received data may not exceed 0 to − 4%. The DH11 receiver clock is accurate to within ± .05% of the nominal data rate. The DH11 transmitter will introduce less than 2% intersymbol distortion, with a long term stability of ± .05%.
DH11

Physical Arrangement: The DH11-AA and DH11-AC are comprised of a pre-wired, double PDP-11 system unit and all logic cards necessary to implement a 16-line multiplexer. Also included is an externally mounted distribution panel, 14 cm by 48.3 cm (5½ x 19 in.), with separate power supply for individual channel termination. The DH11-AA and -AC system unit and distribution panel are pre-wired for plug-in installation of the DM11-BB 16-line Data set Control Multiplexer.

Environmental Information: The DH11 will operate at temperatures between +5° and +45° C, and at relative humidities between 0% and 95%, noncondensing.

Bus Loading: Each DH11 presents 2 unit loads to the PDP-11 UNIBUS. The DM11-BB Data set Control Multiplexer, if present, represents one additional unit load.

The DH11-AD is three loads and the DH11-AE is two loads.

Power Consumption: The DH11 logic draws 8.4 A of +5 Vdc, and 240 mA of −15 Vdc. If the DM11-BB Data set Control Multiplexer is added, the total current drain is 11.2 A at +5 Vdc. The DH11-AD and DH11-AE use 10.8 A at +5 V, 0.4 A at +15 V, and 0.65 A at −15 V.

Electrical Interface: Connection between the DH11 logic and the distribution panel is via a cable containing 16 input and 16 output data lines at Transistor-Transistor Logic levels (0, +5 Vdc). The logic levels are: Mark (logical 1) = 0V, Space (logical 0) = +3 V. Input leads from the distribution panel are equipped with pull up resistors which clamp open input lines in a logical 0 (space) condition. However, logic in the DH11 receiver section prevents this from assembling continuous all-zero characters.

The electrical and physical interface to the external channels is provided by optional level conversion module sets (DM11-DA, -DB, -DC) that plug into the distribution panel. These options are described in the next section.

Models

Connection to Switched Network Data sets

<table>
<thead>
<tr>
<th>DEC No.</th>
<th>PREREQUISITE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>DH11-AA</td>
<td>PDP-11</td>
<td>Programmable 16-line asynchronous serial line multiplexer and distribution panel, includes space for mounting up to four line adapters (16 line interfaces). Power requirement is 115 Vac, 60 Hz, 600 W.</td>
</tr>
</tbody>
</table>

2-62
DH11

DH11-AC  PDP-11  Same as DH11-AA except 230 V, 50 Hz, 600 W.

DM11-BB  DH11-AA or DH11-AC  16-line modem control multiplexer provides program operation of control leads for 103, 202 or equivalent data sets. Mounts in DH11-AA or DH11-AC.

DM11-DC  DM11-BB  Line adapter which implements four EIA/CCITT-compatible lines equipped with data set control features. Includes 25-foot data set cables.

or

DH11-AD  PDP-11  Programmable 16-line asynchronous multiplexer and distribution panel with built-in level conversion for EIA/CCITT compatible lines equipped with data set control features. (Cables are not included).

Private Line Modems (No Control) or Local EIA Terminals

| DH11-AA | PDP-11 | See above -AA |
| DH11-AC | PDP-11 | See above -AC |
| DM11-DB | DH11-AA or DH11-AC | Line adapter which implements four EIA/CCITT lines (data only). Includes four 25-foot modem cables. Note that the -DB can be used on a switched network system. This requires that the data set have Auto Answer strapped on. The data set will answer a call automatically. Not provided in this type of operation is the ability to not answer a call, the ability to initiate a disconnect by the computer, and the ability to sense an intermittent carrier. |

or

DH11-AE  PDP-11  Programmable 16-line asynchronous serial line multiplexer and distribution panel with built-in level conversion for EIA/CCITT compatible lines (data only). Cables are not included).

Local Teletypes

| DH11-AA | PDP-11 | See above DH11-AA |
| DH11-AC | PDP-11 | See above DH11-AC |
| DM11-DA | DH11-AA or DH11-AC | Line adapter for four 20 mA Teletype lines (data only). 2-63 |
DL11

SINGLE ASYNCHRONOUS SERIAL LINE INTERFACES, DL11

Interfacing a Remote Terminal

Interfacing a Remote PDP-11
INTERFACING A LOCAL TERMINAL

DESCRIPTION

The DL11 series of asynchronous single line interfaces handle full or half duplex communication between a wide variety of serial communication channels and a PDP-11 computer.

With a DL11 interface, a PDP-11 computer can communicate with a local terminal such as a console teleprinter, with a remote terminal via data sets and private line or public switched telephone facilities, or with another local or remote PDP-11 computer.

DL11 systems provide wide flexibility. The user can specify data rate from a selection of standard rates between 40 and 9600 Baud, or he can order a non-standard rate device. With most of the standard rates, the interface can offer split-speed operation for faster, more efficient handling of computer output.

For additional flexibility, character size, parity checking (even, odd, or none), and stop code length (1, 1.5, or 2 bits) are switch or strap selectable.
Remote Communication via Private Lines

Each DL11 module represents one unit to the UNIBUS and plugs into a standard small peripheral controller slot in a PDP-11 system. There are three DL11 models.

Model DL11-WA is a serial line 20 mA interface and real-time line frequency clock. It provides the flexibility of a wide choice of speeds, character size, and stop bit configurations. Switches allow modification to replace the DL11-A and DL11-C in most applications.

Model DL11-WB is a serial line EIA interface and real-time line frequency clock. It is capable of handling either local or remote terminals (data only). With local devices, this model requires a null modem; in private line communication, modems are required. Switches allow modification to replace DL11-B and DL11-D in most applications. The DL11-WB gives the same wide range of operating parameters as the DL11-WA.

Model DL11-E meets the EIA and CCITT interface specifications cited for Models B and D. This interface provides the user with the full range of data rates as well as with complete dataset control for remote communication with either a terminal or another PDP-11 computer.
OPERATION

General
The DL11 is an interface between a single Asynchronous Serial Communication Channel and the PDP-11. It performs serial-to-parallel and parallel-to-serial conversion of serial start-stop data with a double character buffered MOS/LSI circuit called a UART (for Universal Asynchronous Receiver-Transmitter). This 40-pin dual-in-line package includes all of the circuitry necessary to double buffer characters in and out, serialize-deserialize data, provide selection of character length and stop code configuration, and present status information about the unit and each character.

Receiver
The receiver section performs serial to parallel conversion of 5, 6, 7 or 8-level codes. The character length is selectable by split-lug jumpers on the DL11-E and by switches on the DL11-WA and DL11-WB, and is specified by the customer at the time of the order. Each character appears right justified in the Receiver Data Buffer Register (RBUF), stripped of start, stop, and parity bits.

The data rate may lie anywhere in the range between 40 baud and 10,000 baud, and in many cases need not necessarily be the same for the receiver as for the transmitter. The receiver samples the line at 16 times the data rate.

A complete character is formed in the UART and is transferred to the Receiver Data Buffer Register (RBUF) at the time the center of the first stop bit is sampled. At that time, the Receiver Done Bit (Bit 7) is set in the Receiver Status Register (RCSR). If the Receiver Interrupt Enable Bit (Bit 6) is also set in RCSR, an interrupt request is generated. The BR level is set by jumper plug. BR4 is standard.

The program then reads the RBUF. The character appears right justified in bits 7-0 of RBUF, stripped of start, stop, and parity (if odd or even is selected) bits. Unused high order bits (6 and 7 in the case of a 6-level code) are zero-filled. Bits 8-11 are always zero and bits 12-15 contain status information about the character supplied by the UART. (See section on PROGRAMMING.)

Transmitter
The transmitter section performs parallel to serial conversion of data supplied to it from the UNIBUS. The character length and stop code (number of units of mark at the end of each character) are the same as for the receiver section. The transmitter section is also fully double buffered. Any time the Transmitter Ready Bit (bit 7) is set in the Transmitter Status Register (XCSR), the program may load the low-order eight bits of the Transmitted Data Buffer Register (XBUF) with a right justified data character. The Transmitter Ready Bit will be set any time the XBUF
is available, whether or not a character is currently being transmitted. This is a natural result of the double buffering and means that if a character is not currently being transmitted and XBUF is empty, the program may provide two characters in succession (within less than one character time) to the transmitter.

**Dataset Control**
The DL11-E is supplied with an electrical and physical interface the same as the DL11-WB, however it is equipped with full dataset control.

**PROGRAMMING**

**General**
The interface between a program running in the PDP-11 processor and the DL11 is via four device registers. They are the 1) Receiver Status Register (RCSR); 2) Receiver Data Buffer Register (RBUF); 3) Transmitter Status Register (XCSR); and 4) Transmitter Data Buffer Register (XBUF). The functions of the bits provided in each register are described below. Each register is assigned an 18-bit memory address, and may be read from or written into using any processor instruction which references these addresses, with the exceptions noted.

**Interrupts**
The DL11 has two channels of interrupts: one for the receiver section (vector = XX0) and one for the transmitter section (vector = XX4). These two circuits operate independently, except that receiver takes priority on simultaneous interrupt requests (is closer to the processor on the bus).

However, it is very important to note that in the DL11-E (dataset operation), the receiver section handles a multiple source interrupt: RCVR DONE and DSET INT. Furthermore, DSET INT is set by several conditions (RING, CARRIER, etc.). If while servicing an interrupt for one condition, a second interrupt condition occurs, a unique second interrupt (and all subsequent ones as well) may not occur. To prevent this: 1) all possible interrupt conditions should be checked after servicing one particular condition, or 2) both interrupt enables (bits 5 and 6) should be cleared upon entry to the service routine for vector XX0, and set again at the end of service.

**Address and Vector Assignments**
The DL11-WA and DL11-WB follow the same address and vector assignments as the DL11-A and DL11-B.
DL11

<table>
<thead>
<tr>
<th>Address</th>
<th>Vector</th>
<th>Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock</td>
<td>777 546</td>
<td>100</td>
</tr>
<tr>
<td>Console</td>
<td>777 560</td>
<td>60/64</td>
</tr>
<tr>
<td></td>
<td>777 562</td>
<td></td>
</tr>
<tr>
<td></td>
<td>777 564</td>
<td></td>
</tr>
<tr>
<td></td>
<td>777 566</td>
<td></td>
</tr>
<tr>
<td>Additional Units</td>
<td>776 XX0</td>
<td>Floating</td>
</tr>
<tr>
<td></td>
<td>776 XX2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>776 XX4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>776 XX6</td>
<td></td>
</tr>
</tbody>
</table>

Where XX = 50 to 67

<table>
<thead>
<tr>
<th>Address</th>
<th>Vector</th>
<th>Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>77XXX0</td>
<td>Floating</td>
</tr>
<tr>
<td></td>
<td>77XXX2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>77XXX4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>77XXX6</td>
<td></td>
</tr>
</tbody>
</table>

Where XXX = 561 to 617.

**Receiver Status Register (RCSR) 77XXX0**

**BIT**

**DESCRIPTION AND OPERATION**

15* Dataset Status Change. Read only. This bit is set (1) by any change in the state of bits 10 (Secondary Receive Data), 12 (Carrier Det.), and 13 (Clear to Send) in RCSR, and by an off to on (0 to 1) change in the state of bit 14 (Ring Ind.) in RCSR. It is cleared (0) by INIT and by reading from RCSR. If bit 5 (Dataset Int. Enable) is set, the setting of bit 15 will cause an interrupt request to be generated.

2-69
14* Ring Indicator. Read only. The state of this bit follows the state of the Ring Indicator lead (Circuit CE, pin 22) from the dataset. It is set when the signal on Circuit CE is high, and cleared when that signal is low. A transition of this bit from 0 to 1 will cause bit 15 in RCSR to be set, and if bit 5 in RCSR is set, will cause an interrupt request to be generated.

13* Clear to Send. Read only. The state of this bit follows the state of the Clear to Send lead (Circuit CB, pin 5) from the dataset. It is set when the signal on Circuit CB is high, and cleared when that signal is low. Any transition of bit 13 will cause bit 15 in RCSR to be set, and if bit 5 in RCSR is set, will cause an interrupt request to be generated.

12* Carrier Detector. Read only. The state of this bit follows the state of the Received Line Signal Detector (Carrier) lead (Circuit CF, pin 8) from the dataset. It is set when the signal on Circuit CF is high, and cleared when that signal is low. Any transition of bit 12 will cause bit 15 in RCSR to be set, and if bit 5 in RCSR is set, will cause an interrupt request to be generated.

11 Receiver Active. Read only. This bit is set when the receiver section of the UART detects a valid start bit on the Received Data lead. In the case of the DL11B, D, and E, this lead will be Circuit BB, pin 3 from the dataset. It is cleared when bit 7 in RCSR (Receiver Done) is set, and by INIT.

10* Secondary Received Data. Read only. The state of this bit follows the state of the Secondary Receive Data lead (Circuit SBB, pin 12) from a Bell 202 dataset. It is set when the signal on circuit SBB is high (spacing) and cleared when that signal is low (marking). Any transition of bit 10 will cause bit 15 in RCSR to be set, and if bit 5 in RCSR is set, will cause an interrupt request to be generated.

7 Receiver Done. Read only. This bit is set when the receiver section of the UART has transferred an incoming character to the Receiver Data Buffer Register (RBUF). It is cleared by setting bit 0 (Reader Enable) in RCSR, by addressing (read or write) RBUF, or by INIT. If bit 6 in RCSR is set, the setting of bit 7 will cause an interrupt request to be generated.

6 Receiver Interrupt Enable. Read/Write. This bit, when set, causes an interrupt request to be generated each time bit 7 in RCSR is set. It is cleared by INIT, or by the program.

5* Dataset Interrupt Enable. Read/Write. This bit, when set, causes an interrupt request to be generated each time bit 15 in RCSR is set. It is cleared by INIT, or by the program.

Note that all signals from the dataset will appear negated (low) to the program if the dataset is disconnected or loses power. This affects bits 14, 13, 12, and 10, all of which will appear as cleared under such conditions.
2* Request to Send. Read/Write. This bit, when set, causes the signal on Circuit CA, pin 4, to the dataset to go high, and when cleared causes that signal to go low. There is a Jumper on the DL11-E Card such that this bit may be made to control the Forced Busy lead (pin 25) to the dataset instead of Circuit CA. It is cleared by INIT, or by the program.

1* Data Terminal Ready. Read/Write. This bit, when set, causes the signal on Circuit CD, pin 20 to the dataset to be asserted (high), and when cleared causes that signal to be negated (low). This bit is not cleared by INIT, and may be set/reset only by the program. It must be set or cleared as appropriate by the program after power is applied to the machine, since its state at that time is undefined.

0 Reader Enable. Write only. This bit, when set, causes the Reader Run Relay on certain DIGITAL-supplied teleprinters to advance the paper tape reader. It also clears Receiver Done (bit 7) in RCSR. It is cleared by INIT, or when bit 11 in RCSR is set.

Receiver Data Buffer Register (RBUF) 77XXX2

BIT DESCRIPTION AND OPERATION

15* Error. Read only. This bit is set if bit 14, 13, or 12 (or any combination of these bits) in RBUF is set (logical OR of bits 14, 13, 12). It is cleared only if none of the above bits are set.

14* Overrun. Read only. This bit is set if bit 7 in RCSR (Receiver Done) is not cleared before the UART attempts to present a new character to RBUF, i.e., if the UART attempts to set bit 7 in RCSR, and it is already set. The previous character in RBUF is lost, and the new character replaces it.
13° Framing Error. Read only. This bit is set if the UART, at the time it samples the received data line in the center of the first stop bit, finds the line in a spacing (0) condition. This may indicate an open input line, "BREAK" signal, or excessive distortion of the received character.

12° Receive Data Parity Error. Read only. This bit is set by the UART if the parity of the received data character does not agree with the parity specified to the UART (odd or even). This bit is always zero if the "no parity check" option is specified. Bits 14, 13, and 12 are updated each time a character is received.

7-0 Received Data. Read only. These bits contain the last complete character assembled by the UART. If the character length specified to the UART is less than 8 bits, the character will appear right justified (low order bit in bit 0). The unused high order bits will contain 0.

* NOTE The state of bits 14, 13, and 12 applies to the character currently in RBUF, bits 7-0. It is not necessary to clear them in order to receive the next character. Error conditions remain present until the next character is received, at which time the error bits are updated. INIT does not necessarily clear the error bits. In the DL11-WA and DL11-WB error bits may be disabled by a switch.

Transmitter Status Register (XCSR) 77XXX4

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<td>TRANSMITTER READY</td>
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<td>TRANSMITTER INTERRUPT ENABLE</td>
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<td></td>
<td>BREAK</td>
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</table>

BIT DESCRIPTION AND OPERATION

15-8 Unused

7 Transmitter Ready. Read only. This bit is cleared when a data character is loaded into XBUF. It is set when XBUF can accept another data character, and by INIT. If bit 6 in XCSR is set, this bit, when set, will cause an interrupt request to be generated. Note that this bit is set, not cleared, by INIT.
6 Transmitter Interrupt Enable. Read/Write. This bit, when set, will cause an interrupt request to be generated whenever bit 7 in XCSR is set. This bit is cleared by INIT and by the program.

5, 4, 3 Unused

2 Maintenance. Read/Write. This bit, when set, causes data emitted at the serial output of the UART transmitter section to appear at the serial input of the receiver section. In addition, it forces the receiver to run at the same data rate as the transmitter, and disconnects the external serial line input to the receiver. It is cleared by INIT, and by the program.

1 Unused

0 BREAK. Read/Write. This bit, when set, clamps the serial data output of the UART transmitter to a spacing (logical 0) condition. The transmitter will appear to the program to function normally if characters are presented to XBUF, but a continuous spacing signal will appear on the Transmitted Data lead (Circuit BA). This bit is cleared by INIT, and by the program.

Transmitted Data Buffer Register (XBUF) 77XXX6

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<thead>
<tr>
<th>15</th>
<th>14</th>
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<th>0</th>
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<tr>
<td>TDM 07</td>
<td>TDM 06</td>
<td>TDM 05</td>
<td>TDM 04</td>
<td>TDM 03</td>
<td>TDM 02</td>
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</table>

BIT DESCRIPTION AND OPERATION

7-0 Transmitted Data. Write only. These bits contain the data character to be transmitted by the UART. If the data character contains fewer than 8 data bits, the character must be right justified when loaded into XBUF. The bits of the character are presented to the serial line low-order bit (bit 0) first. A bit set to one in XBUF will cause a marking condition to appear on the transmitted data lead for one bit time. Cleared by INIT.

Clock Status Register (LKS)*

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<th>15</th>
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<tbody>
<tr>
<td>MONITOR</td>
<td>INIT</td>
<td>ENB</td>
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LINE CLOCK MONITOR LINE CLOCK INTERRUPT ENABLE
BIT MEANING AND OPERATION

15-8 Unused.

7 LINE CLOCK MONITOR—Read/Clear. Set only by the line frequency clock signal and cleared only by the program. Set by INIT.

6 LINE CLOCK INTERRUPT ENABLE—Read/Write. Cleared by INIT. When set, Starts an interrupt sequence if Line Clock monitor is also set.

5-0 Unused.

* DL11-WA and WB only.

NOTE
Line Clock circuit must be disabled via a switch when serial line portion is used as other than console interface (Address 77756X).

Priorities are hardwired and are not selectable.

Floating vectors for serial line interface portion are switch selectable.

SPECIFICATIONS

Function: Provides an interface between the PDP-11 UNIBUS and a single asynchronous bit serial communications channel.

Mechanical: The DL11 consists of one quad module and a connecting cable terminated in a plug appropriate to the data communications equipment to be connected.

Operating Mode: Full or half duplex under program control.

Data Format: Asynchronous, serial by bit. One start and one, one and one-half (5-level codes only), or two stop bits, supplied by the hardware. The DL11-WA, WB, and E will accommodate characters of 5, 6, 7, or 8 bits, with or without even or odd parity. The data format must be the same for transmitted and received data. The data format must be specified at the time of order.

A one (1) presented by the program to any bit in the Transmitted Data Register will cause a Marking (logical 1) condition to appear on the Transmitted Data lead during the corresponding bit interval. A zero (0) presented by the program will cause a Spacing (logical 0) condition to appear on the Transmitted Data lead during the corresponding bit interval.
DL11

cal 0) condition to appear. A Marking condition on the Received Data lead during any data bit sampling interval will be presented to the program as a one (1) in the Received Data Register, and a Spacing condition will be presented as a zero (0).

**Order of Bit Transmission:** Low order bit first.

**Distortion:** The DL11 receiver will operate properly in the presence of 40% space-to-mark or mark-to-space distortion between any two received data bits, and up to ± 4.5%, long-term speed distortion, provided the data format contains at least one and one-half stop units. If the data format contains only one stop unit, the speed tolerance is ± 4%. The DL11 transmitter operates with less than 3% bit-to-bit or long-term distortion.

**Bus Loading:** One DL11 presents one unit load to the PDP-11 UNIBUS.

**Electrical Interface:** DL11-WA provides a 20 mA active current loop for both send and receive leads for connection to local teleprinters.

The DL11-WA is supplied with a 2 1/4 ft., 6-conductor cable terminated with a female MATE-N-LOC connector.

The DL11-WB provides a voltage level interface and connector whose signal levels and connector pinning conform to Electronic Industries Association Standard RS-232-C and CCITT Recommendation V.24. The leads supported are:

- Protective Ground, Circuit AA, pin 1.
- Transmitted Data, Circuit BA, pin 2.
- Received Data, Circuit BB, pin 3.
- Signal Ground, Circuit AB, pin 7.
- Data Terminal Ready, Circuit CD, pin 20*.
- Request to Send, Circuit CA, pin 4*.

* These leads are held ON (logical 1) by the hardware.

The DL11-E provides a voltage level interface as described above for the DL11-WB but in addition supports the following leads, giving full dataset control capability to the computer program:

Data Terminal Ready, Circuit CD, pin 20.
Clear to Send, Circuit CB, pin 5.
Request to Send, Circuit CA, pin 4.
Received Line Signal Detector (Carrier), Circuit CF, pin 8.
Ring Indicator, Circuit CE, pin 22.
Secondary Transmitted Data, Circuit SBA, pin 11*.
Secondary Received Data, Circuit SBB, pin 12*.

* Note that the pin assignment of these two leads conforms to that of the Bell 202 Dataset, rather than to the cited EIA/CCITT standard.


**Power Requirements:**

The DL11 requires 1.8 amps of $+5 \text{v}$, .05 amps of $+15 \text{v}$, and .15 amps of $-15 \text{v}$.

DL11-WA, WB

2.0amps at $+5 \text{V}$

.05 amps at $+15 \text{V}$

.15 amps at $-15 \text{V}$

DL11-E

1.8amps at $+5 \text{V}$

.05 amps at $+15 \text{V}$

.15 amps at $-15 \text{V}$

**Data Rate:**

The DL11-E is supplied to customer order with 13 standard data rates in four groups.

Group 1. 110 Baud receive and transmit.

Group 2. 134.5 Baud receive and transmit.

Group 3. Following 8 speeds, which may be different for receive and transmit: 50, 75, 150, 300, 600, 1200, 1800, 2400 Baud.
Group 4. Following 8 speeds, which may be different for receive and transmit: 200, 300, 600, 1200, 2400, 4800, 7200, 9600 Baud.

The DL11-WA, WB is supplied with eight switch selectable speeds: 110, 150, 300, 600, 1200, 2400, 4800, 9600 Baud.


DL11-E: Single Asynchronous Serial Line Interface. Supports full dataset control interface, including Data Terminal Ready, Clear to Send, Request to Send. Carrier, Ring, Secondary Received and Secondary Transmitted leads.
NETWORK LINK, DMC11

HIGHLIGHTS

- Local or remote interconnection of computers over a serial synchronous link.
- DDCMP communications protocol implemented by hardware for reliable data transmission, high throughput, low processor overhead and ease of programming.
- Pipelined operation for high throughput by overlapping data transmissions, program operation and propagation delays.
- Local operation at 1,000,000 bits per second (full- or half-duplex) over coaxial cable up to 6,000 ft long.
- Local operation at 56,000 bits per second (full- or half-duplex) over coaxial cable up to 18,000 ft long.
- Remote operation over synchronous modems at speeds up to 19,200 bits per second (half- or full-duplex) using CCITT V.24/EIA RS-232-C interface.
- Remote operation at speeds up to 250,000 bits per second (full- or half-duplex) using CCITT V.35/DDS interface.
- Half-duplex local operation using a single coaxial cable.
- Private wire or switched network remote operation.
- Communication between DMC-11's or between a DMC11 and other synchronous interfaces that can support the DDCMP protocol.
- Down-line loading of satellite computer systems.
- Ability to initialize an incorrectly functioning satellite computer system by command over the link (Remote Load Detect).
- Same PDP-11 software supporting local or remote, full- or half-duplex configurations.
- Recovery from power failures at either or both ends of a link without loss of data.
- 16-bit NPR (DMA) transfers for minimum interference with processor operation.

GENERAL DESCRIPTION

The DMC11 Network Link is designed for high-performance interconnection of PDP-11 computers in network applications. Where the computers are located in the same facility, DMC11's can be configured for high-speed operation (56,000 or 1,000,000 bits per second) over inexpensive coaxial cable. The necessary modems are built-in. Where the computers are located remotely and connected via common carrier facilities, DMC11's can be configured to interface to synchronous modems such as the Bell Models 208 and 209, or Bell 500A LI/5 and equivalent synchronous modems conforming to the EIA RS-232-C and the CCITT V.35/DDS standards respectively.

Two PDP-11 computers can be connected by a pair of DMC11's. For remote operation, a DMC11 can communicate with a different type of synchronous interface or even a different type of computer, provided...
That the remote system has implemented the DDCMP (DIGITAL Data Communication Message Protocol) protocol.

The DMC11 ensures reliable data transmission by implementing the DDCMP protocol in hardware using a high-speed microprocessor. The DDCMP protocol detects errors on the channel interconnecting the systems by using a 16-bit Cyclic Redundancy Check (CRC-16). Errors are corrected, when necessary, by automatic retransmissions. Sequence numbers in message headers ensure that messages are delivered in proper order with no omissions or duplications.

Errors are commonplace on cables or other communications channels more than a few feet in length. Reliable data transmission requires a protocol. The DMC11 takes care of the details of protocol operation including character and message synchronization, header and message formatting, error checking and retransmission control. The PDP-11 program need not worry about these details.

The DMC11 offers a number of advantages over conventional interfaces which require a combination of hardware and software to implement a protocol. Programming is greatly simplified. Programming the DMC11 does not require extensive communications expertise. PDP-11 memory and processor time are not wasted with instructions implementing the protocol. Throughput is enhanced because the DMC11 microprocessor operates at high speed and is not delayed when the processor has to perform high-priority tasks.

**FULL-DUPLEX OPERATION**

The DMC11 supports full- or half-duplex operation. Full-duplex operation offers the highest throughput and is used when the communications facilities permit two-way simultaneous operation. Data and/or control messages can be exchanged between the two computer systems simultaneously in both directions. The DDCMP protocol permits continuous simultaneous transmission of data messages in both directions when buffers are available and there are no errors on the channels.

In order to take advantage of this pipeline capability, the DMC11 permits the PDP-11 program to queue as many as seven buffers containing messages for transmission and as many as seven empty buffers for reception. By queuing up multiple buffers, the programs can effectively overlap PDP-11 processing with data transmission.

Transmissions do not have to stop while the program responds to an end-of-message interrupt. The DMC11 will interrupt the PDP-11 when a message has been successfully transmitted or received. All this time the program can supply a new buffer to keep the pipeline filled.

**HALF-DUPLEX OPERATION**

Half-duplex operation is used where throughput requirements do not justify the added cost of cables or communications lines capable of simultaneous operation in both directions. Local operation requires two coaxial cables for full-duplex operation but only one coaxial cable for half-duplex operation. This is particularly important for dial-up operation when two calls would need to be placed for full-duplex operation.
The PDP-11 program does not have to worry about the details of half-duplex operation. All it needs to do is specify half-duplex operation at device initialization. The DMC11 ensures that both ends of the link are coordinated: one listening while the other is transmitting. The program queues transmit and receive buffers exactly as for full-duplex operation. The same program can be used for local and remote operations, private wire and dial-backup operation, because of this feature.

DOWN-LINE LOADING AND REMOTE LOAD DETECT
The DMC11 supports down-line loading of computer system software. Down-line loading is used when software is centrally stored (in a host system) and distributed over the network links to other systems (the satellite systems). These satellites are often small systems with no peripherals available for program loading. Sometimes the satellite systems have disks, but down-line loading is desired to maintain central control over the software.

The DMC11 can send and receive down-line loading messages in the DDCMP Maintenance format. DMC11’s can be used for down-line loading at the host, satellite, or both ends of a link. A special ROM (read-only memory) bootstrap is needed for down-line loading when a DMC11 is used at the satellite end of a link (M9301-YJ).

Unattended operation of satellite systems in a network requires the host systems to be able to initialize an incorrectly-functioning satellite system and force it to execute a new program loaded down the communications link. A special DDCMP maintenance message is used for this purpose. A DMC11 at the satellite end of a link can recognize this message and initialize the associated computer system.

PHYSICAL DESCRIPTION
A DMC11 consists of two modules, a microprocessor module and a line unit module. The two modules are interconnected by a one-foot cable. The microprocessor and line unit modules are ordered separately. Two versions of the microprocessor module are available. Four versions of the line unit module are available: local operation at 1,000,000 bps (bits per second), local operation at 56,000 bps, remote operation with RS-232-C compatible synchronous modems (up to 19,200 bps) and remote operation with CCITT V.35/DDS compatible synchronous modems (up to 250,000 bits per second).

The DMC11-AR/AL microprocessor modules are hex-sized single PC boards that fit into a hex small peripheral controller (SPC) slot. They include a 300 ns bipolar microprocessor, a Read-Only Memory implementing the DDCMP protocol, local scratch pad memory (RAM), and a UNIBUS interface.

The DMC11-AL microprocessor is used with local line units type DMC11-MA and DMC11-MD. The DMC11-AR microprocessor is used with remote line units type DMC11-DA and DMC11-FA.

The DMC11-MA, DMC11-MD, DMC11-DA, and DMC11-FA line unit modules are hex-sized PC boards for use in SPC slots. They have a cut-out
DMC11

to fit over a UNIBUS connector so they can also be located in the end slots of a DD11 system unit, but not in the case where an 8½ in. high UNIBUS terminator or cable connector is used. Each includes a one foot cable for connection to the microprocessor module.

The DMC11-MA line unit module includes serial-to-parallel conversion and a built-in modem for local operation at 1,000,000 bps over coaxial cable up to 6,000 ft in length. Coaxial cables are not included.

The DMC11-MD line unit module includes serial-to-parallel conversion and a built-in modem for local operation at 56,000 bps over coaxial cable up to 18,000 ft in length. Coaxial cables are not included.

The DMC11-DA line unit module includes serial-to-parallel conversion and a CCITT V.24/EIA RS-232-C interface for use with Bell 208 and 209 synchronous modems or equivalent. Clocking is supplied by the modem and speeds up to 19,200 bps can be used. The DMC11-DA includes data set control for full-duplex or half-duplex, private wire or switched operation. A 25-foot cable with 25-pin EIA connector is included.

The DMC11-FA line unit module includes serial-to-parallel conversion and a CCITT V.35/DDS interface for use with Bell 500A L1/5 synchronous modems or equivalent. Clocking is supplied by the modem and speeds up to 250,000 bps can be used. The DMC11-FA includes data set control for full-duplex or half-duplex, private wire operation. A 25-foot cable with connector is included.

CONFIGURATIONS

Where two PDP-11's are to be interconnected locally by coaxial cable, a DMC11 is required at each end of the link. For operation at 1,000,000 bps, each DMC11 would include a DMC11-AL and a DMC11-MA. For operation at 56,000 bps, each DMC11 would include a DMC11-AL and a DMC11-MD. In addition, one coaxial cable is needed for half-duplex operation, two for full-duplex operation.

When two PDP-11's are to be interconnected remotely by synchronous modems and common carrier facilities, DMC11's can be used at each end of a link. Each DMC11 would include a DMC11-AR and a DMC11-DA or a DMC11-FA.

A PDP-11 can be interconnected remotely to another computer system that can interface to synchronous modems and support the DDCMP protocol. The configuration would include a DMC11-AR, DMC11-DA, or a DMC11-FA, synchronous modems and compatible communications facilities. At the remote end would be the appropriate communication interface and the computer system software implementing the DDCMP protocol.

CABLES

Local operation uses inexpensive coaxial cable and standard connectors. One cable is used for half-duplex operation, two for full-duplex operation. The required cable, complete with connectors, is available from DIGITAL in a 100 foot length (BC03N-A0). When longer lengths are needed, or
the systems are not located in the same room, the customer is responsible for supplying and installing the cable. It is suggested that the cable be installed well before delivery of the DMC11s.

MAINTENANCE FEATURES
The DMC11 contains a number of features that ensure reliable operation and ease of maintenance. During normal operation, the DMC11 keeps count of communication errors and retransmissions. These counts are recorded in PDP-11 memory. Occasional retransmissions are handled automatically by the DMC11, but repeated errors will result in an interrupt to the PDP-11 to inform the program that action is needed (such as calling the common carrier).

The DMC11-AR/AL microprocessors can be single-stepped by a diagnostic program to verify correct operation. The diagnostic program can supply special micro-instructions to thoroughly exercise the DMC11 logic. It can also verify the contents of the ROM program.

The DMC11-MA, DMC11-MD, DMC11-DA, and DMC11-FA line units can be single-stepped by a diagnostic program to verify correct operation. Programmable loopback prior to the built-in modem or level convertors, together with a free-running maintenance clock, enable the majority of DMC11 logic to be exercised without disconnecting any cables. Special turnaround connectors are supplied to provide a complete test of a DMC11.

DMC11 OPERATION
All communications between the PDP-11 and the DMC11 are through eight bytes of control and status registers. Four bytes of these registers are multipurpose. Their meaning is controlled by the other registers and their use is governed by the DMC11 microprocessor. All commands, command completions and status information pass through these registers.

The PDP-11 program is completely insulated by the DMC11 from the communications link and the DDCMP protocol. When the program initializes the DDCMP protocol it defines the characteristics of the link with a single command. From that point on, the DMC11 will perform all data-link control activities, notifying the user of failures only after an error threshold has been exceeded.

The program initializes the DMC11 by supplying the address of a core memory area which the DMC11 uses to keep a snapshot of protocol activity for power fail recovery and defining the characteristics of the data link.

From that point on, all the program needs to do is to request and then use the multipurpose registers to provide the bus address and byte count of messages to be transmitted or buffers to be filled on reception. The DMC11 is multiple buffered. Up to seven messages for the transmitter and seven buffers for the receiver can be queued by the DMC11.

After a bus address/byte count has been assigned, the DMC11 assures error-free sequential message transfer by use of the DDCMP protocol. Transmit commands will be reported as completed when successfully
DMC11

acknowledged. Receive commands will be reported as completed when an entire message has been successfully received in correct sequence. Successful command completion will interrupt the PDP-11 processor, if enabled.

POWER FAIL RECOVERY
The DMC11 may be programmed to either cold start or warm start on powerfail recovery. Cold starting initiates the DDCMP startup sequence to make certain that the remote system is aware of the restart. A cold start resets all the DDCMP sequence numbers so the status of previously transmitted but unacknowledged messages is indeterminate.

To warm start, the DMC11 utilizes the snapshot of protocol operation kept in core memory. Restarting proceeds at the state indicated. Messages being transmitted at the time of power failure will be retransmitted as necessary. By using the DDCMP sequence numbers (stored in the core memory area) correct recovery of all messages without loss or duplication is assured, providing that neither end of the link does a cold start. Should only one end of a link experience a lengthy power failure, the other end will exceed an error threshold and cause a status interrupt. However, a remote DMC11 will not initiate a cold start unless commanded by the remote PDP-11 program. Recovery from lengthy power failures or communications outages is possible.

MULTIPLE DMC11s ON A SYSTEM
Up to 16 DMC11s may be connected to a system for operation at 56Kb or lower speeds. At 1Mb, two DMC11s may be connected for full-duplex operation, four for half-duplex operation.

DMC11 PROGRAMMING
Programming the DMC11 is best described at two levels. The first level describes how a PDP-11 program uses the DMC11 control and status registers together with the interrupt system for transfer of control and status information between the PDP-11 program and the DMC11 microprogram. The second level describes details of these transactions, including formats, details of device and protocol initialization, data transfer and unusual cases.

In order to successfully program the DMC11 it is not necessary to be familiar with the details of DDCMP protocol operation. These are handled by the DMC11 microprogram. However some familiarity with the protocol operation will be useful in interpreting the significance of the various error counters provided to assess the quality of the circuit connecting the two computers. If a DMC11 is to communicate with a different interface which uses a software implementation of DDCMP, the person programming the software implementation should consult the DDCMP protocol standard document.

CONTROL AND STATUS REGISTERS
Communication of control and status information between the PDP-11 and the DMC11 uses eight bytes of control and status registers (CSR's). These are addressed as 76XXX0, 76XXX1, 76XXX2, 76XXX3, 76XXX4,
76XXX5, 76XXX6, and 76XXX7. These device addresses will be subsequently referred to as Byte Select 0 to 7 (BSEL0-BSEL7) for indicating individual bytes and as SEL0, SEL2, SEL4, and SEL6 for indicating words.

NOTE
The Control and Status Registers are implemented with Random Access Memory (RAM). Thus at power on, the CSR's will come up in random states. As part of the microprocessor initialization the CSR's (BSEL0, 1, 2) will be cleared with the exception of bit 15 of SEL0 (RUN) which will be set. The lower order 8 bits of SEL0 (BSEL0) will be cleared first.

BSEL4-7 comprise a 32 bit data port used to pass information between the microprocessor and the PDP-11. When the data port is used to transfer information from the PDP-11 to the microprocessor this will be called an Input Transfer, often abbreviated "IN" or "I". When the data port is used to transfer information from the microprocessor to the PDP-11 this will be called an Output Transfer, often abbreviated "OUT" or "O". These terms are not to be confused with sending and receiving data on the serial line which will be called "sending" or "transmission," "receiving" or "reception."

BSEL0 controls input transfers and BSEL2 controls output transfers. BSEL1 contains bits used for maintenance purposes which are not of concern to the programmer. It also contains the MASTER CLEAR bit which can be used to initialize the DMC11 microprocessor. BSEL2 is not used. A switch on the microprocessor module prevents the PDP-11 program from clearing RUN or performing other maintenance functions in BSEL1 which would disable the microprocessor's ability to initialize an unattended PDP-11 computer system.

INPUT TRANSFERS
Whenever the data port is not in use it is subject to being seized by the microprocessor for use in an output transfer. Therefore the PDP-11 program must request the microprocessor to assign it the port before proceeding with an input transfer. It must also specify the type of input transfer (a transmit buffer, a receive buffer, control information, etc.) so the microprocessor can make appropriate preparations.

The PDP-11 program should set bits 0-2 of BSEL0 to indicate the type of transfer and then set bit 5, Request in (RQI) to request the port. (These bits may be set by a single instruction.) The microprocessor will respond by setting bit 7, Ready In (RDYI) when the port has been assigned to the PDP-11 program. When RDYI has been set the PDP-11 program should load the desired data into the data port (BSEL4-7). Then it should clear RQI. The microprocessor will take the data and drop RDYI which completes the transfer.

Bit 6 of BSEL0, Interrupt Enable Input (IEI), controls whether the PDP-11 program receives an interrupt (to Vector XX0) when the microprocessor has set RDYI. It is most efficient for the PDP-11 to have interrupts disabled and simply scan RDYI one or more times until the microprocessor has set it. While the PDP-11 program is waiting it must be prepared to
DMC11

accept an output transfer because the microprocessor may have seized the port in the meanwhile.

The microprocessor cannot service certain types of input transfers immediately. In these cases, it is convenient to use interrupts. If the PDP-11 program finds RDYI clear after several scans, it can enable interrupts by setting IEI. The DMC11 will interrupt the PDP-11 (to Vector XX0) when the microprocessor has set RDYI. The PDP-11 program will get the interrupt even if the microprocessor had already set RDYI at the time the program sets IEI. The program can bypass any scanning if IEI is set when the program sets RQI.

The PDP-11 program may set or clear IEI by using a MOV or BIS instruction whenever RQI and RDYI are both clear or when it sets RQI (same instruction). The PDP-11 may clear IEI by using a MOV or BIC instruction when it clears RQI (same instruction). The PDP-11 must set IEI by using two successive BIS instructions (required to ensure IEI gets set) when it has set RQI and is awaiting RDYI. If interrupts have been enabled, the PDP-11 must not clear RQI until the interrupt has occurred.

NOTE

The PDP-11 program should not begin a new input transfer until the previous transfer has been completed, as indicated by the microprocessor clearing RDYI. If the PDP-11 program wishes to begin a new transfer immediately, it should check that RDYI has been cleared before setting RQI. This can be done by scanning RDYI until it has been cleared. (When the DMC11 clears RDYI it also clears all other bits in this byte except IEI.) The PDP-11 program must not attempt to queue more than seven buffers for transmission or reception or data integrity may be lost.

OUTPUT TRANSFERS

The microprocessor initiates an output transfer when it has status or error information to transfer to the PDP-11 program or it wishes to return a full buffer on reception or an empty buffer on transmission. The microprocessor can initiate an output transfer at any time the data port is free: that is, not assigned to the PDP-11 program for an input transfer and not in use for a previous output transfer. However, if the PDP-11 program has initialized the DMC11 by setting MASTER CLEAR or generating the INIT signal on the UNIBUS, the microprocessor does not generate any output transfers until it has been initialized by the PDP-11 program.

The microprocessor loads status or error information into the data port (BSEL4-7) and sets bits 0-2 of BSEL2, to indicate the format and significance of the data. It then sets bit 7 of BSEL2, Ready Out (RDYO), to indicate to the PDP-11 program that data is available. In response to RDYO setting, the PDP-11 program should note the type of output transfer as specified in bits 0-2 of BSEL2 and read the data in the data port. When the PDP-11 program has sampled all the data, it must complete the

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output transfer by clearing RDYO. This frees the data port for a subsequent transaction.

If the PDP-11 program wishes, it can enable interrupts on output transfers by setting bit 6 of BSEL2, Interrupt Enable Output (IEO). If IEO is set, the DMC11 interrupts the PDP-11 (to Vector XX4) after the microprocessor has set RDYO. Since the PDP-11 program usually does not know when an output transfer will occur (for example, when a message will be received) an efficient PDP-11 program ordinarily enables interrupts on output transfers. If IEO was not set at the time the microprocessor set RDYO no interrupt will occur if the PDP-11 program then sets it. (Therefore it is recommended that IEO be set at initialization time and left set, or cleared at initialization time and left clear.)

NOTE

The PDP-11 program must respond to RDYO being set by reading the data and clearing RDYO. Failure to do this prevents the data port from being freed. If the PDP-11 program has requested an input transfer by setting RQI, it must be prepared to respond to an output transfer prior to being given RDYI. If the PDP-11 program fails to respond to RDYO, it never gets RDYI. The PDP-11 program should not spin on RDYI in a loop that does not also test RDYO unless interrupts on output transfers are enabled, and the loop executes at a lower priority level than the DMC11 interrupt level.

<table>
<thead>
<tr>
<th>UNIBUS CONTROL &amp; STATUS REGISTERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSR'S 15</td>
</tr>
<tr>
<td>RUN</td>
</tr>
<tr>
<td>RDYO</td>
</tr>
</tbody>
</table>

Figure 1

**SELO**

<table>
<thead>
<tr>
<th>BIT</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-0</td>
<td>TYPEI</td>
<td>Defines type of input transfer</td>
</tr>
</tbody>
</table>

BIT 1  BIT 0

<table>
<thead>
<tr>
<th>0</th>
<th>0</th>
<th>Buffer Address/Character Count In (BA/CC I)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>Control In (CNTL I)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>reserved</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Base In (BASE I)</td>
</tr>
</tbody>
</table>

2 | IN | I/O

Set or cleared by PDP-11. 0 indicates transmission, 1 reception

reserved

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### DMC11

<table>
<thead>
<tr>
<th>BIT</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>RQI</td>
<td>Set by the PDP-11 to request an input transfer, cleared by the PDP-11 when data has been loaded</td>
</tr>
<tr>
<td>6</td>
<td>IEI</td>
<td>Set or cleared by PDP-11. If set the PDP-11 is interrupted to Vector XX0 when RDYI is set</td>
</tr>
<tr>
<td>7</td>
<td>RDYI</td>
<td>Set by the microprocessor in response to RQI to indicate the data port is available for an input transfer. Cleared by the microprocessor at the end of an input transfer</td>
</tr>
<tr>
<td>8</td>
<td>STEP µP</td>
<td>Maintenance only</td>
</tr>
<tr>
<td>9</td>
<td>ROM 1</td>
<td>Maintenance only</td>
</tr>
<tr>
<td>10</td>
<td>ROM 0</td>
<td>Maintenance only</td>
</tr>
<tr>
<td>11</td>
<td>LU LOOP</td>
<td>Maintenance only</td>
</tr>
<tr>
<td>12</td>
<td>STEP LU</td>
<td>Maintenance only</td>
</tr>
<tr>
<td>13</td>
<td></td>
<td>reserved</td>
</tr>
<tr>
<td>14</td>
<td>MASTER CLEAR</td>
<td>Setting this bit initializes the DMC11. This bit is self clearing</td>
</tr>
<tr>
<td>15</td>
<td>RUN</td>
<td>Maintenance only</td>
</tr>
</tbody>
</table>

**SEL2**

<table>
<thead>
<tr>
<th>BIT 1</th>
<th>BIT 0</th>
<th>Defines type of output transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Buffer Address/Character Count Out (BA/CC 0)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Control Out (CNTL O)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>reserved</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>reserved</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2</th>
<th>OUT I/O</th>
<th>Set or cleared by the microprocessor. 0 indicates transmission, 1 reception</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-5</td>
<td>reserved</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>IEO</td>
<td>Set or cleared by PDP-11. If set the PDP-11 is interrupted to Vector XX4 when RDYO is set</td>
</tr>
<tr>
<td>7</td>
<td>RDYO</td>
<td>Set by the microprocessor when an output transfer is ready, cleared by PDP-11 when it has completed the output transfer</td>
</tr>
<tr>
<td>8-15</td>
<td>reserved</td>
<td></td>
</tr>
</tbody>
</table>

**SEL4**

| 15-0 | First half of the Data Port |

**SEL6**

| 15-0 | Second half of the Data Port |

The format and contents of the data port depend on the transfer type (TYPEI or TYPEO). Loaded by the PDP-11 on input transfers, loaded by the microprocessor on output transfers
DMC11

INITIALIZATION

The power-up sequence and UNIBUS INIT signal initialize the DMC11 and sets DTR on DMC11-DA and DMC11-FA line units. The PDP-11 program can accomplish the same effect by setting MASTER CLEAR in BSEL1. Each of these procedures restarts the microprocessor to the beginning of its microprogram. In this state, the microprocessor does not send or receive messages on the serial line or generate output transfers. The PDP-11 program should not access the CSRs for 2 micro-seconds following MASTER CLEAR. Alternatively, the program may load BSEL2 with a non-zero value; do a MASTER CLEAR, then wait for the DMC11 to clear BSEL2.

When the PDP-11 program wants the DMC11 to function, it must perform an input transfer that specifies the base address of a 64 word table in PDP-11 memory, which is called the base table. The PDP-11 program requests the BASEI transfer by setting TYPEI to 11. In response to RDVI, the program loads the low-order 16 bits of the address into SEL4 and the high-order 2 bits of the address into bits 15 and 14 of SEL6. If the DDCMP protocol operation is to be initialized, the RESUME bit (bit 13 of SEL6) must be clear.

Once the PDP-11 has specified a base address, the 64 word base table belongs to the microprocessor until the DMC11 is master cleared by INIT or MASTER CLEAR. The PDP-11 program may examine the contents of the base table (for example, error counters relating to protocol operation) but must not alter its contents.

By supplying a base address with the RESUME bit clear the microprocessor is conditioned to respond to the DDCMP start-up sequence.

The PDP-11 program must perform an input transfer using the Control In format immediately following the BASEIN transfer. It must set the Half-Duplex bit (SEL 6 bit 10) in this transfer if the channel is half-duplex and it must leave the bit clear if the channel is full-duplex. In addition, the program must specify whether the DMC11 is to operate as a half-duplex secondary station (long timer) or a half-duplex primary station (short timer) by setting or clearing Secondary (SEL6 bit 11). A half-duplex link must have one primary station and one secondary station. The only difference between the two is in the length of time spent before retransmitting a start sequence.

A Control In transfer should be performed only immediately following a BASEIN transfer. If it is desired to switch modes (for example to switch to half-duplex for dial back-up operation) the PDP-11 program should shut the DMC11 down in an orderly fashion by creating a procedure error then master clear the DMC11, supply a new base and then perform the Control-In. If the protocol is not to be initialized, the base in transfer may specify the resume bit.

The DMC11 options containing the integral modem must be specifically strapped for half-duplex, when using single cable operation, in addition to requiring the Control In transfer.
DDCMP START UP
Before data messages can be transmitted or received, the DDCMP start-up procedure must be completed to make certain that both ends of the link are correctly initialized. The start-up procedure is initiated within one timer interval following the assignment of the BASE. In order to complete successfully, both DMC11's must initiate the start-up procedure. The start-up procedure will normally complete within a few timer intervals following initiation of the start-up procedure by both DMC11's, unless there are errors on the communications channels. Successful completion of the start-up procedure places a DMC11 in the running state and implies that both DMC11's were simultaneously executing the start-up procedure and that it was possible to exchange messages in both directions on the communications channel.

The PDP-11 program may ignore the details of the start-up procedure. However, one important property of the procedure is significant. Once the local DMC11 has entered the running state (completed the procedure), it detects and flags as an error the fact that the other end has reinitialized the start-up procedure. As a result, the PDP-11 program receives a Control Out transfer with SEL6 bit 7 (DDCMP START REC'D) set. If this happens, the PDP-11 program knows that the other end of the link has restarted. The PDP-11 program should initialize the DMC11 and begin again.

DATA TRANSMISSION
When the PDP-11 program wishes to transmit a buffer of data it clears bits 1 and 0 of BSEL0 to indicate a Buffer Address/Character Count In transfer and clears bit 2 of BSEL0, (IN I/O) to specify that this is a full buffer to be transmitted. It then requests an input transfer by setting RQI. In response to RDY1 it loads SEL4 with the low order 16 bits of the buffer address, bits 15 and 14 of SEL6 with the high order bits of the address and bits 13 to 0 of SEL6 with the 14 bit character count. Buffers from 1 to 16,383 bytes long may be used for local operation. For remote operation buffers are limited to a practical maximum of about 512 bytes, depending on the error rate of the communications facilities. Each buffer corresponds to a single DDCMP data message.

When the message has been successfully transmitted and an acknowledgment received, the microprocessor will initiate an output transfer with bits 1 and 0 of BSEL2 clear to indicate the Buffer/Character Count Out (BA/CC 0) format. Bit 2 (Out I/O) will be clear to indicate that a successfully transmitted buffer has been returned to the program.

The PDP-11 program may queue up to seven buffers for transmission by supplying buffers to the microprocessor faster than it returns them.

NOTE
The PDP-11 program should not request an input transfer that will supply a transmit buffer if 7 are already outstanding as data integrity may be lost.
DATA RECEPTION
When the PDP-11 program has an empty buffer it wishes to fill with received data it clears bits 1 and 0 of BSEL0 to indicate a BA/CC I transfer and sets bit 2 of BSEL0 (IN I/O) to specify that an empty buffer has been made available for reception. It then requests an input transfer by setting RQI. In response to RDYI it loads SEL4 and SEL6 with the buffer address and character count, in the same format as for transmission. The character count must be large enough to accommodate the longest message expected.

When a message has been successfully received and stored in the buffer the microprocessor will initiate an output transfer with bits 1 and 0 of BSEL2 cleared to indicate the BA/CC format. Bit 2 (OUT I/O) will be set to indicate a full buffer has been received. SEL4 and SEL6 will contain the address of the buffer and the actual number of characters received.

If a message is received when no receive buffer is available the microprocessor will inform the PDP-11 by means of a Control Out transfer with bit 2 of SEL6 (O'RUN) set. The other end of the link will be informed of the error and will automatically retransmit the message. The PDP-11 program should supply a buffer as soon as possible.

The PDP-11 may queue up to seven empty buffers for reception by supplying them to the microprocessor faster than it returns buffers.

NOTE
The PDP-11 program should not request an input transfer that will supply a buffer for reception if 7 are already outstanding as data integrity may be lost.

CONTROL OUT TRANSFERS
The microprocessor informs the PDP-11 program of unusual or error conditions involving the communications channel, remote end of the link, DMC11 hardware or PDP-11 program by means of an output transfer with bit 1 of BSEL2 clear and bit 0 set indicating a Control Out (CNTL O) transfer. SEL6 contains bits that indicate the error condition. Some errors are advisory in nature and normal operation may continue. Others are fatal and require the PDP-11 program to initialize the DMC11 by doing a Master Clear followed by a BASEl and CNTL l.

Bit 0 (DATA CK) indicates that a retransmission threshold has been exceeded. (More than 7 consecutive retries have occurred for transmission or reception.) This indicates a defective communications channel. The PDP-11 can examine error counters in the base table for more details of the error. This is a non-fatal error. Should the cause of the error be corrected normal operation will continue with no messages lost in either direction. This error may appear repeatedly until the condition is corrected or until the DMC11 is initialized. Transient errors corrected before 7 retransmissions will not be reported to the PDP-11 program but will be counted in the base table.
Bit 1 (TIME OUT) indicates that the microprocessor has received no response from the remote end of the link for a specified period (21 seconds). This indicates a broken communications channel or a failure at the other end of the link (possibly a power failure). Like DATA CK, this is a non-fatal error which can occur repeatedly.

Bit 2 (O'RUN) indicates that a message was received but no buffer is available. The O'RUN bit is not set on an isolated occurrence. However, if an 8th consecutive retry fails for lack of a buffer the O'RUN error bit is set.

Bit 3 (DDCMP MAINT REC'D) indicates that a message in the DDCMP Maintenance format was received. This is a fatal error. The DMC11 must be initialized and put into maintenance mode. Messages in progress are lost.

Bit 4 (LOST DATA) indicates that a message was received that is longer than the buffer supplied by the PDP-11 program. This is a fatal error.

Bit 6 (DISCONNECT) indicates that an on to off transition of the modem data set ready lead has been detected (remote operation only). This is a non-fatal error. For dial-up operation the PDP-11 program must consider the possibility that a new caller has connected to the DMC11 if this is required by security considerations.

Bit 7 (DDCMP START REC'D) indicates that a DDCMP Start message was received when the protocol was in the Running state. This indicates that the remote computer has reinitialized its end of the link. This is a fatal error. The PDP-11 program may initialize the DMC11 if it wishes to start over and complete the start-up sequence.

Bit 8 (NON EX MEM) indicates that a Unibus address time-out has occurred. This could have been caused by the PDP-11 program specifying an invalid base address, buffer address, or count, or the PDP-11 memory is defective. This is a fatal error.

Bit 9 (PROC ERR) indicates a procedure error on the part of the PDP-11 program. The requested input transfer cannot be honored due to a programming error. This error can be caused by requesting a BA/CC before supplying a base address, requesting a base address a second time, or specifying an invalid code in BSEL0 bits 1 and 0. This is a fatal error. The PDP-11 program may create this condition as a means of shutting down the DMC11 in an orderly manner. Data Terminal Ready is cleared as a result of this error.

MAINTENANCE MESSAGES
A special DDCMP message format, the Maintenance message, is used for down line loading, restarting, or otherwise maintaining satellite computer systems. Messages in this format are subject to error checking but are unsequenced, unacknowledged, and not retransmitted automatically by the DMC11. Transmission is always half-duplex.

Maintenance messages can only be sent and received while the microprocessor is in the DDCMP maintenance state. The PDP-11 program may cause the microprocessor to enter this state by a CNTLI transfer with bit 8 of SEL6 (DDCMP MAINT) set. In this case the PDP-11 program
must precede the Control In transfer by a Master Clear followed by a Base In. In addition to setting bit 8 of SEL6, the Control In transfer must also set the Half Duplex bit (bit 10 of SEL6) if half duplex facilities are used.

Once in DDCMP maintenance mode, maintenance messages can be sent and received similarly to data messages. On transmission, the data portion of the message is taken from the buffer with the DMC11 generating the header and CRC's. On reception, only the data portion is placed in the buffer. Messages not in DDCMP maintenance format or having incorrect CRC's are simply discarded. Also, no ACK's are sent in this mode so transmit done is set following each transmission.

The data portion of the maintenance message may contain any data that is desired, but ordinarily it conforms to the DIGITAL Maintenance Operation Protocol (MOP) formats. When a host computer wishes to restart a satellite computer system, it must send the appropriate MOP messages as described below. In order to leave Maintenance mode, the PDP-11 program must initialize the DMC11 and supply a base address with the RESUME bit clear.

REMOTE LOAD DETECT AND DOWN LINE LOAD
Whenever the microprocessor is running, it is constantly scanning the serial line for a DDCMP maintenance message containing an ENTER MOP MODE data field. What happens when this particular message is received depends on the setting of two switch packs on the DMC11 line unit. Depending on the setting of these switches, the DMC11 will trigger the PDP-11 to begin executing a program in a read-only memory (ROM) bootstrap (BM873, M9301, etc.). In case a ROM bootstrap is triggered, switches on the line unit specify an 8-bit byte offset to the bootstrap address space. The address range is 173000 to 173376. The offset is determined by switch pack E91 on the M8202 module and E88 on the M8201 module.

The data portion of the ENTER MOP MODE message is 5 bytes long. The first byte contains the decimal number 6. The remaining 4 bytes contain the same 8-bit value. This value is specified by a switch pack on the DMC11 line unit and serves as a password to protect against inadvertent recognition of the ENTER MOP MODE message. These messages with an invalid password, are discarded if the switch settings specify remote load detect. If the password switch pack is set to 377 then the RLD is disabled. The password switch pack is E90 on the M8202 and E87 on the M8201.

NOTE
No receive buffer is required for remote load detection.

POWER FAIL RECOVERY
The DMC11 keeps all data necessary to attempt recovery from a power failure in its base table. When the PDP-11 program detects a power failure, it should cease requesting input transfers and create a procedure error by specifying an invalid code in BSEL0 bits 1 and 0. At this point, the DMC11 ceases to send and receive messages and update the
BASE table. When power has been restored, the PDP-11 power recovery program can tell the DMC11 microprocessor to recover from the error by performing a BASE I transfer with the RESUME bit set. The original base address must be specified and the contents of the base table must be the same as they were when power was lost; otherwise, the program must start over (RESUME bit clear). If the base table is within MOS or bipolar memory (without battery backup), recovery will not be successful since the base table will have been lost. If the PDP-11 processor is a PDP-11/34, 11/45, 11/60, 11/55, or 11/70, DMC11 power fail recovery may be accompanied by data loss, therefore the software should be designed to reinitialize the DMC11 using software-maintained information about transmit and receive messages pending.

SHUTDOWN OF THE DMC11
The PDP-11 program may shut down the DMC11 by creating a procedure error by specifying an invalid code in BSELO bits 1 and 0. The PDP-11 program should process output transfers from messages already sent and acknowledged or received until the procedure error code appears in a CNTL O transfer. Additionally, the procedure error (or invalid code) will cause the DMC11 to drop DTR until a master clear is issued.

The above method of orderly shut-down ensures that all messages which the DMC11 has received and acknowledged are passed to the PDP-11 program.

DATA SET CONTROL
The DMC11-AR microprocessor maintains Data Terminal Ready continuously, dropping it following a procedure error (PROC ERR). Data Terminal Ready is reasserted when the device is master cleared. An on-to-off transition of Data Set Ready provides a CNTL O transfer if the DMC11 has been given a base address and has sent the DDCMP start sequence.

Request to Send is asserted by the line unit when there is data to send and negated when the transmit data shift registers and silo's are empty.

CUMULATIVE ERROR COUNTS
In order to help localize component failures in the communications channel, the DMC11 provides a record of each recoverable communication error it encounters. Eight bit counters for these errors are provided within the base table. The base table is updated periodically to provide these counters. Additionally, the table is updated following every fatal error. The format of these counters is detailed as follows:

<table>
<thead>
<tr>
<th>Location</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>BASE+5</td>
<td>NAKS Recd</td>
</tr>
<tr>
<td>BASE+6</td>
<td>NAKS Sent—No Buffer Available</td>
</tr>
<tr>
<td>BASE+7</td>
<td>NAKS Sent—Bad Header BCC</td>
</tr>
<tr>
<td>BASE+10</td>
<td>NAKS Sent—Bad Data BCC</td>
</tr>
<tr>
<td>BASE+11</td>
<td>REPS Sent</td>
</tr>
<tr>
<td>BASE+12</td>
<td>REPS Recd</td>
</tr>
</tbody>
</table>

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OPTIMIZING PERFORMANCE OF THE DMC11
The DMC11 implements the DDCMP protocol, which imposes a fixed overhead of ten characters on each data message and requires a synchronization sequence whenever the line has gone idle. Optimal performance is approached when the message sizes approach the maximum that may be transmitted without error, the DMC11 is provided with maximal numbers of buffers, and message transfer is bidirectional. Applications using very small messages yield poor link efficiency. Applications using very large messages may yield poor link efficiency as a result of line error rates.

DATA PORT MESSAGE FORMATS
1. BA/CC I and BA/CO O format

![Figure 2]

SEL4 bits 15-0 BA 15:00 The low order 16 bits of the 18 bit buffer address
SEL6 bits 15-14 BA 17:16 The high order 2 bits of the 18 bit buffer address
bits 13-0 CC 13:00 The 14 bit character count (in positive notation, not complement form)

2. BASE I format

![Figure 3]

SEL4 bits 15-0 B 15:00 The low order 16 bits of the 18 bit base address of the 128 word base table
SEL6 bits 15-14 B 17:16 The high order 2 bits of the 18 bit base address
bit 12 RESUME If clear the microprocessor initializes the base table and protocol. If set the microprocessor resumes operation as specified by the contents of the base table
3. CNTL I format

![Figure 4](image)

**SEL6** Bit 11 **SEC**  If set indicates a half duplex secondary station. If clear indicates a half duplex primary station. Not used for full duplex

Bit 10 **HD**  If set indicates half duplex DDCMP operation is required. If clear full duplex is required. Must be used with bit 11, SEC

Bit 8 **MAINT**  If set the microprocessor enters the DDCMP maintenance mode and remains in that mode until subsequently initialized

4. CNTL O format

![Figure 5](image)

See the section on Control Out Transfers for the use of these bits.

**SYSTEM ADDRESSES**
The DMC11 uses eight (8) Bytes of floating address space. The addresses as used for DMC11-AR/AL are:

- 76XXX0  Control IN status register
- 76XXX1  Maintenance register
- 76XXX2  Control OUT register
- 76XXX3  Reserved
- 76XXX4  I/O Transfer port
- 76XXX5  I/O Transfer port
- 76XXX6  I/O Transfer port
- 76XXX7  I/O Transfer port

The relative position of the DMC11 within the floating address system is number seven, directly following LK11A.
DMC11

VECTOR ASSIGNMENT
The DMC11 uses two vectors (mod 10) XX0 and XX4. Interrupts are vectored to XX0 for RYDI and to XX4 for RDYO if the respective interrupt enable is set. The vector assignment is within the floating vector system—relative position is number 25 directly following DWUN.

PROGRAM INTERRUPT PRIORITY
The DMC11 interrupt priority for Vectors XX0 and XX4 are controlled by one standard PDP-11 priority connector. The priority can be changed by substituting the appropriate priority connectors. DMC11’s will be shipped with a priority 5 connector.

SPECIFICATIONS

DMC11-AR/AL—DDCMP Microprocessor Module

<table>
<thead>
<tr>
<th>Protocol</th>
<th>DDCMP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type of Operation</td>
<td>Full duplex or half duplex, point to point</td>
</tr>
<tr>
<td>Data Format</td>
<td>8 bit bytes, DDCMP message formats</td>
</tr>
<tr>
<td>Data Transfers</td>
<td>16 bit NPR (8 bit NPR at beginning or end of buffers where required)</td>
</tr>
<tr>
<td>Status Area in PDP-11</td>
<td>Location: Programmable</td>
</tr>
<tr>
<td>Memory</td>
<td>Size: 64 words</td>
</tr>
<tr>
<td>Mounting Space</td>
<td>One hex SPC slot in DD11-C, or DD11-D back-plane</td>
</tr>
<tr>
<td>Bus Loading</td>
<td>One UNIBUS load</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>5.0 amps at +5V</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>+10 to +40°C</td>
</tr>
<tr>
<td>Humidity</td>
<td>10 to 90%</td>
</tr>
<tr>
<td>Reference</td>
<td>DEC STD 102—Class C device</td>
</tr>
</tbody>
</table>

DMC11-MA, DMC11-MD—Line Unit Modules (Local)

| Operating Mode                | Half duplex (single cable), full duplex (two cables) |
| Data Format                   | Synchronous serial by bit, LSB first |
| Character Size                | 8 bits |
| Block Check                   | 16 bit CRC-16 polynomial |
| Data Rate                     | 1,000,000 bps (DMC11-MA), 56,000 bps (DMC11-MD) |
| Maximum Distance              | 6,000 feet (DMC11-MA), 18,000 feet (DMC11-MD) |
| Modulation                    | Diphase (double freq.) NRZ |
| Transmitter Timing            | RC Osc., trimmable ±5% |
| Receiver Timing               | From received signal |
| Line Interface                | Transformer coupled |
| Common Mode Rejection         | 500 to 1 |
| Transmitter Signal            | 4 volts P-P |
| Receiver Signal               | 150 mv (min.) P-P |
| Cable Type                    | Belden 8232 or equivalent (not supplied) |
| Connector Type                | AMP 20606 series |
| Mounting Space                | One hex SPC slot (DD11C or D), cut out also permits use in end slots of backplane. |
DMC11

Power Consumption
3.0 amps at +5V
.046 amps at -15V
.018 amps at +15V

DMC11-DA/FA—Line Unit Module (remote)
Operating Mode: Full or half duplex
Communications Channel: Private wire or switched
Data Format: Synchronous, serial by bit, LSB first
Character Size: 8 bits
Block Check: 16 bit CRC-16 polynomial
Data Rate: Up to 19,200 bps (clocked by modem)
Interface: Up to 250,000 bps (clocked by modem)
(No CCITT V.24/EIA RS-232-C compatible
(DMC11-DA only)
CCITT V.35 or DDS compatible (DMC11-FA only)
Modems
Bell 208, 209 or equivalent (DMC11-DA only)
Bell 500A LI/5 or GTE Lenkurt L500 A-5 or equivalent (DMC11-FA only)
Signals Supported
BA transmit data
DB serial clock transmit (SCT)
BB receive data
DD serial clock receive (SCR)
CC data set ready
CD data terminal ready
CA request to send
CB clear to send
Cable
25 foot with connector supplied
Mounting Space
One hex SPC slot (DD11C or D), cutout permits use in end slots of backplane as well
Power Consumption
3.0 amps at +5V
.31 amps at -15V
.03 amps at +15V

ORDERING INFORMATION

DEC No. Prerequisite Description
DMC11-AR/AL PDP-11 DDCMP Microprocessor
DMC11-MA DMC11-AL 1 Mb local line unit
DMC11-MD DMC11-AL 56 Kb local line unit
DMC11-DA DMC11-AR remote (EIA) line unit
DMC11-FA DMC11-AR Remote V.35/DDS line unit
BC03N-A0 DMC11-RA or MD 100 foot coax cable

RELATED DOCUMENTATION
DDCMP Protocol Specification V4.0

2-97
AUTOMATIC CALLING UNIT INTERFACE, DN11

DESCRIPTION
With the DN11 and a Bell 801 Automatic Calling Unit (ACU), any PDP-11 can dial any telephone number in the Direct Distance Dial Network and establish a data link. The DN11 is a digit-buffered interface, and digits to be dialed are presented as four-bit binary numbers. The interface drives the ACU with EIA-232-C voltages and is connected via a standard 25-pin plug.

The programmer has access to all lines of the 801 through the DN11. The 801 presents the following leads to the DN11: Power Indicator, Data Line Occupied, Abandon Call and Retry, Data Set Status and Present Next Digit. The DN11 provides the following leads to the 801: Digit Present, Call Request and four Digit Leads.

Because the PDP-11 UNIBUS serves as a multiplexer, multiple automatic calling units can be added to the PDP-11. One PDP-11 System Unit accepts up to four 801 ACU Interfaces. Each interface looks like one device to the UNIBUS.

The Sequence of Operations
The following describes the use of the DN11 to originate a DDD call. This is an automated version of the procedure that everyone goes through when placing a telephone call.

1. Turn 801 power on (FWI = 0).
2. Check for unoccupied data line (DLO = 0).
3. Set Call Request bit (FCRQ = 1).
4. The 801 will seize the line on receiving the dial tone and assert Present Next Digit which causes a PDP-11 program interrupt (FPND = 1).
5. The line is now in use and the Data Line Occupied bit is set (DLO = 1).
6. The first digit to be dialed is provided by loading the four least significant bits of the byte into the digit bits (8 to 11) of the DN11 status register. The upper four bits of the byte are read-only and can have any value during the loading of the four low-order bits.
7. The 801 is informed that the 1st digit has been loaded by asserting the Digit Present Bit (FDPR = 1).
8. The 801 then reads Digit leads 1 through 4 and lowers Present Next Digit Lead (FPND = 0).
9. The hardware responds and lowers Digit Present Lead (FDPR = 0).
10. The 801 then dials the first digit and again raises Present Next Digit Lead (FPND = 1).
11. The next digit is loaded and the Digit Present bit is asserted (FDPR = 1).

12. Sequences 6 through 10 are repeated until all digits have been dialed.

13. When the last digit has been dialed, one of two procedures must be used to complete the call.

a) If "handshaking signals" are used (Bell 100 series modems or equivalent):

A Detect Answer option is used. The 801 retains line control and looks for an answering tone, from the called station. Upon receiving the tone the modem is connected to the line, Data Set Status is asserted and a program interrupt is generated (DSS = 1). This stops the Abandon Call and Retry timer which would have been initiated had no tone been received. These, in turn, would have generated a signal to the DN11 and cause a program interrupt with the Abandon Call and Retry bit set (ACR = 1). The program would then either retry or drop the call.

b) If using modems without the automatic handshaking feature:

The End-of-Number (EON) mode must be used. EON is sent after the last digit has been dialed. This causes the 801 to connect the modem to the line and assert Data-Set Status (DSS = 1). However, the modem and its controller must be able to determine when the called station has answered and is sending data. To do this, it is necessary to use an 801 with option "Y" (available from the Telephone Company). This option lets the Abandon Call and Retry timer continue running even after the DSS bit has been set. When the ACR timer times out it will notify the user of the line to check if data is being received by the modem.

14. There are two options available when terminating a call:

a) The Call Request bit is set to zero (FCRQ = 0). This will remain until the Data Line Occupied bit also goes to zero (DLO = 0), which is a necessary condition before a new call can be initiated.

b) If the 801 option "Z" is used, the call can be terminated by clearing Data Terminal Ready in the modem. In this case, dropping Call Request will not terminate the call. However, it must be dropped before a new call can be attempted.

15. Should the 801 lose power during a call an interrupt will be generated and the Power Off bit will be set (PWI = 1). The interface will not return an interrupt if the Call Request bit is set with the power off (FCRQ = 1).

Programming
Each ACU interface contains one register and therefore requires one
16-bit address. Address space has been assigned for 64 interfaces. The four addresses for the four interfaces that can be plugged into one system unit must be consecutive addresses starting with 775XX0 where XX = 20 for the first line. If only one line is in use, it uses address 775 200. Interface number 2 has address 775 202, and interface number 64 has address 775 376.

Note: In addition to the individual Interrupt Enable bit for each interface, there is a master enable bit associated with line number 1 of a given system unit. It enables the interrupts for the entire group. The master enable bit on lines 2 through 4 of a given system unit are ignored by the interface.

Each set of four DN11’s require one interrupt vector. The vector address for communications options are assigned in the range from 300 to 777. (See Appendix A).

All units are shipped with the bus request line set to BR4. This can be changed in the field with a Bus Request Priority Jumper Plug.

**ACU Interface Status Register**

![ACU Interface Status Register Diagram]

**BIT** | **NAME** | **FUNCTION**
--- | --- | ---
15 | Power Indicate (PWI) | This bit is normally zero and is set by the ACU whenever power is switched off at the unit. If a call is in progress at that time, DONE is set. This causes an interrupt if INTENB and MINAB = 1 (Read only).

14 | Abandon Call and Retry (ACR) | A control lead from the ACU. This bit is set by the ACU whenever an internal timer times out. The timer is reset by the ACU whenever it gives PND and is for detecting wrong numbers and busy signals. It is inhibited by the presence of DSS except if
the 801 option "Y" is in use; it times out even then and gives an interrupt (by setting DONE). This is used when the programmer wants a timer to detect wrong numbers and busy signals.

12  Data Line Occupied (FDLO)

This bit is set by the ACU whenever the line to the telephone central office is being used by the ACU. It allows the programmer to test the ACU to see if the last call was successfully terminated before he tries to use it for the next one (Read only).

11-8  Digit Bits (NB1-4)

These four bits are control leads to the ACU. These low order bits of the second byte make up the BCD digit to be dialed. Since the high-order four are read only, it does not matter what is in them during a load, and the programmer may use them as he wishes. In MAINT mode, these bits are used to drive the four control lines that can cause interrupts. See bit 3 for description (Read/Write).

7  DONE

This bit is set to indicate that the ACU is done with the previously requested action and ready to accept new data, usually the next digit in a sequence to be dialed.

The conditions that set DONE are listed (CRQ must be a one):

1. Transition of PND to one (after CRQ set or previous DPR set).
2. Transition of DSS to one (after last DPR or EON).
3. Transition of ACR to one (if timeout error—anytime).
4. Transition of PWI to one (if power switched off) (Read/Write)

6  Interrupt Enable (INTENB)

This bit allows the setting of done to cause an interrupt if the master enable bit (bit 02 line #1 of a system unit) is set (Read/Write).

5  Data Set Status (DSS)

Control lead from ACU. This is a statement by the ACU that the called party has answered and that the associated data set now has control of the line. It is accom-
panied by the setting of DONE to obtain an interrupt. It remains set until after the end of the call (or until the data terminal ready lead to the associated modem is dropped which then drops FDSS).

If the associated modem answers a call while the dialer is in use (CRQ = 1), then DSS will be enabled and DONE set. If interrupt Enable is set there will be an interrupt (Read only).

Control lead from the ACU. This is a request by the ACU for the program to load another digit during dialing. It is accompanied by the setting of DONE to obtain an interrupt. It is cleared by the ACU when the digit is accepted (after DPR is set) and will remain off at least 600 ms before coming up for the next request (Read only).

This bit, when set, allows checking of the interface without a connected ACU. It allows FCRQ to be read and switches the ACU response lines—PND, DSS, PWI and ACR to the output of the digit lines for testing purposes.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Digit</th>
<th>ACU Line to Ctl Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>08</td>
<td>NB1</td>
<td>PND FPND</td>
</tr>
<tr>
<td>09</td>
<td>NB2</td>
<td>DSS FDSS</td>
</tr>
<tr>
<td>10</td>
<td>NB4</td>
<td>PWI PWO</td>
</tr>
<tr>
<td>11</td>
<td>NB8</td>
<td>ACR FACR</td>
</tr>
</tbody>
</table>

This bit also forces CRQ (to ACU) off and forces FDLO (Bit 12) on. (Read/Write).

Allows the program to disable then re-enable all 4 ACU interrupts easily with one bit. This bit is connected for only one of the four possible lines which mount in one system unit (Read/Write).

Control lead to the ACU. This bit must be set by the program after it loads the next digit (in response to a PND request) to inform the ACU to continue dialing. The interface automatically clears this bit when the ACU clears PND to indicate acceptance of the digit (Read/Write).
0 Call Request (FCRQ)  Control lead to ACU. This bit starts the Automatic Calling Sequence (Write only).

**SPECIFICATIONS**

**Control Signals:**

All control leads are brought into the DN11 from the Bell 801. All leads are EA RS-366 and CCITT compatible. All leads are failsafe (i.e., they appear off if the 801 loses power).

**Bus Load:**

One DN11 interface represents one unit load to the PDP-11 UNIBUS. Thus, four controls in one System Unit represent four unit loads.

**Program Interrupts:**

Normal interrupts are caused during a call by:

1. Transition of PND to a one. Sets DONE. Digit desired.
2. Transition of DSS to a one. Sets DONE. Data set connected.
3. Transition of ACR to a one. Sets DONE. Busy or wrong number.

Error interrupts are caused during a call by:

1. Transition of PWI to off. Sets DONE. Power to ACU was switched off.

(Note: Appropriate Enable bits must be set.)

**Physical Connection:**


**Power Required:**

1.4 Amps of $+5V$ for the first line; 0.4 Amps of $+5V$ for the second through the fourth lines.

**Temperature/Humidity:**

$0^\circ-40^\circ C$ with Relative Humidity of 20% to 90%, non-condensing.

**Pin Numbers on the 801 Cable**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Designation</th>
<th>Abbr.</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Call Request</td>
<td>CRQ</td>
</tr>
<tr>
<td>5</td>
<td>Digit Present</td>
<td>DPR</td>
</tr>
<tr>
<td>14</td>
<td>Digit Lead</td>
<td>NB1</td>
</tr>
</tbody>
</table>

2-103
DN11

15  Digit Lead  NB2
16  Digit Lead  NB4
17  Digit Lead  NB8

Input

Pin  Designation  Abbr.
5    Present Next Digit  PND
6    Power Indication  PWI
22   Data Line Occupied  DLO
1    Frame GND  FGD
7    Signal GND  SGD

Models

DN11-AA  Prewired System Unit for up to four Bell 801 Automatic Calling Unit interfaces. (DN11-DA)

DN11-DA  One Line Interface for a Bell 801 Automatic Calling Unit. Includes 25' Cable (Up to four DN11-DA's may be mounted in a DN11-AA).

CONFIGURATIONS

ASYNCHRONOUS SINGLE-LINE INTERFACE

SYNCHRONOUS SINGLE-LINE INTERFACE

2-104
ASYNCHRONOUS MULTIPLE LINE INTERFACE
NPR SYNCHRONOUS LINE INTERFACE, DQ11

FEATURES

• Non-Processor Request (NPR) data transfers for transmit and receive.
• Transmission speeds up to 1.0 million bits per second when utilizing an appropriate protocol.
• Full- or half-duplex operation.
• Programmable parity (VRC) checking. Parity (odd or even) is switch selectable.
• Data Set control.
• Switch-selectable (one or two) Sync characters to character frame.
• Programmable Sync character.
• Programmable character size; up to sixteen bits per character with double character transfers for characters containing eight bits or less.

2-106
• Double-buffered transmit and receive data registers.
• Double-buffered character count and bus address registers.
• Auto idle, strip Sync, and half-duplex program selectable.
• Diagnostic-controlled self-testing capabilities.
• Three switch-selectable control characters for program interrupts.
• Interfaces to Bell 201, 208, and 303 or equivalent modems.

INTRODUCTION

The DQ11 is a high-speed, double-buffered communications device designed to interface the PDP-11 Processor to a serial synchronous communications channel. This interface allows the PDP-11 to be used for remote batch and remote concentrator applications. With the DQ11, the PDP-11 can also be used as a front-end synchronous line controller to handle remote and local synchronous terminals. The DQ11 sets a new performance standard for the industry with transmission speeds up to 1.0 Megabaud.

The DQ11 provides parallel-to-serial and serial-to-parallel data conversion, voltage or current level conversion, character recognition, error detection, and Data Set control for half- or full-duplex operation. The interface is compatible with the Bell 201, 208, and 303 modems, or their equivalents.

Transmit and receive data transfers between the PDP-11 UNIBUS and the DQ11 are handled as Non-Processor Requests (NPR). These are direct memory or device access data transfers without processor supervision. As an NPR device, the DQ11 provides extremely fast access to the PDP-11 UNIBUS and can transfer data at exceptionally high rates once it gains control. The PDP-11 Processor state is not affected by these types of transfers, since they occur on a cycle-steal basis.

The DQ11 contains diagnostic-controlled, self-testing facilities to ensure both the quality of the data converters and control logic, and to minimize on-line malfunctions.

The DQ11-DA furnishes level conversion conforming to Electronic Industries Association (EIA) standard RS-232-C and to CCITT Recommendation V.24. The DQ11-EA is designed for current mode operation, utilizing the Bell System 303, or an equivalent modem. The DQ11-DA is capable of transmitting data at speeds up to 10,000 bits per second. Data may be transmitted at speeds up to 1.0 million bits per second with the DQ11-EA.

The DQ11 device is a single system unit and a module set. The module set includes all logic required to interact with the PDP-11 UNIBUS. It consists of a double-buffered Character Count Register, a double-buffered Bus Address Register, Transmitter, Receiver, and three switch-selectable characters (receive only) for character recognition. The Character Count and Bus Address Registers are maintained in the hardware, enabling data transfer rates up to 125,000 characters per second.
DATA SET CONTROL
Data Set control is a standard feature of the DQ11 system. It includes the following functions:

- Request to Send (jumper inhibits initialize)
- Data Terminal Ready (jumper inhibits initialize)
- Ring Indicator (flag on leading and trailing edge)
- Carrier Detect Indicator (flag on leading and trailing edge)
- Clear to Send Indicator (flag on leading and trailing edge)
- Data Set Ready Indicator
- Data Set Flag Interrupt Enable
- Two optional bits for customer-defined interrupts and/or Data Set control functions.

DQ11 CONFIGURATIONS

<table>
<thead>
<tr>
<th>DEC No.</th>
<th>Capabilities</th>
<th>Type of Interface</th>
<th>Modem Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQ11-DA</td>
<td>Block Transfers</td>
<td>EIA/CCITT</td>
<td>Bell 201, 208 or Equivalent</td>
</tr>
<tr>
<td></td>
<td>Data Set Control</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DQ11-EA</td>
<td>Block Transfers</td>
<td>Current Mode</td>
<td>Bell 303, or Equivalent</td>
</tr>
<tr>
<td></td>
<td>Data Set Control</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

OPERATION

General
The DQ11 is a double-buffered synchronous serial line interface capable of two-way simultaneous communications. It translates between serial data and parallel data. Output characters are transferred in parallel from the PDP-11 UNIBUS into the DQ11 where they are serially shifted to the communication line. Input characters from the modem are shifted into the DQ11 and made available to the PDP-11 on an NPR interrupt basis.

Synchronization between the DQ11 and the transmitting device is established by a Sync character code. Once synchronization is achieved, serial data can be transmitted and received continuously (no start or stop bits are required as in asynchronous communications). Both the receiver and transmitter are double buffered. Since the Character Count Register is also double buffered, a full buffer time is available to service character count overflow interrupts. The clocking necessary to serialize the data may be provided by the associated high-speed synchronous modem.

SYSTEM UNIT

Transmitter Section
The Transmitter Section of the DQ11 performs parallel-to-serial conversion of data supplied to it from the PDP-11 UNIBUS.
After the Initialize pulse, the program must set the Miscellaneous Register (bits 11 through 8) for the desired character length (1 to 16 bits), and a desired word count and current address for transmit and receive. Before any required handshaking with the Data Set, the program may load the Sync Register with the desired Sync character. When the Sync Register is loaded, the Sync character will be used for both Receiver and Transmitter operations.

Any required handshaking to establish connection with the Data Set may be done at this time. Once handshaking is complete, the program can assert the Transmit GO (Tx GO) bit in the Transmit Status Register (Tx Stat) to commence NPR data transfers.

The Transmitter Section of the DQ11 allows the sending of IDLE characters whenever Tx GO is zero. In the non-transparent mode, the IDLE character is the content of the Sync Register.

**Receiver Section**
The Receiver Section of the DQ11 performs serial-to-parallel conversion of incoming data arriving from the modem.

After any required handshaking with the Data Set, NPR receiver data transfers and framing will commence when the Receive GO (Rx GO) bit in the Receive Status Register is asserted by the program. The Receiver becomes synchronized with the incoming data when it recognizes one or two consecutive Sync characters.

Once synchronization is established and when the Receive Active (Rx Active) bit in the Receive Status Register is asserted, receiver data transfers commence. Clearing the Rx Active bit while Rx GO is asserted forces new Sync characters. Receive Active may be set following synchronization or on the first non-Sync character following synchronization. The standard shipping configuration will be synchronized on two consecutive Sync characters followed by Active on the first non-Sync character.

**PROGRAMMING**
**General**
The address assigned to the DQ11 is the floating address space reserved for PDP-11 peripherals. The DQ11 address assignment starts at 170010 and follows the DH11 in the order of assignments.

Each DQ11 requires four addresses to accommodate the following device registers:

Receive Status Register (Rx STAT)
Address: 76XXX0 (Addressable by word or byte)

Transmit Status Register (Tx STAT)
Address: 76XXX2 (Addressable by word or byte)
REG/ERR Register
Address: 76XXX4 (Addressable by word or byte)

Secondary Registers (SEC REG)
Address: 76XXX6 (Addressable by word only)

Sixteen secondary registers are provided for read/write operations. These registers are:

Receive Bus Address (BA)—Primary
Receive Character Count (CC)—Primary
Transmit Bus Address (BA)—Primary
Transmit Character Count (CC)—Primary
Receive Bus Address (BA)—Secondary
Receive Character Count (CC)—Secondary
Transmit Bus Address (BA)—Secondary
Transmit Character Count (CC)—Secondary
Sync
Miscellaneous
Transmit Buffer (Tx BUF)

Interrupts and Vector Assignment
The interrupt service routine should service all flags within the interrupting vector before returning to the mainline program.

All interrupts are under two vectors, where vector "A" is XXO and vector "B" is XX4. These interrupts are as follows:

Receive Status Register (XXO):
Receiver Done Primary (Rx Done P)
Receiver Done Secondary (Rx Done S)
Character Flag

Transmit Status Register (XX4):
Transmit Done Primary (Tx Done P)
Transmit Done Secondary (Tx Done S)
Error Flag
Data Set Flag

The DQ11 follows the DH11 in the floating vector assignment area. Vector assignment is from 300 to 777.

Register Definitions
The bit assignments within each register are presented in the following information.

Programming Note:
Upon power up, the program must clear:

a) The bus address registers (reg. pointer 0, 2, 4, 6) with the related extended bus address bits.
b) The character count registers (reg. pointer 1, 3, 5, 7) with the related enter T/exit T bits.

RECEIVE STATUS REGISTER (Rx STAT)
Address: 76XXX0 (Addressable by word or byte)

### Bit Function

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>RECEIVE GO (Rx Go)</td>
<td>When set, this bit enables receiver data transfers (NPR) and framing. When cleared, receiver data transfers are inhibited from being set by the hardware. Clearing Rx Go will also clear Receive Active. This bit is read/write and is cleared by:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1) Initialize</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2) Master Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3) If Rx Clock Loss, Rx Latency, or Rx Non-Existent Memory are set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4) If the Character Count (CC) goes to zero (Primary and Secondary registers).</td>
</tr>
<tr>
<td>01</td>
<td>STRIP SYNC</td>
<td>When this bit is set, all Sync characters following Receive Active are stripped from the incoming serial data. In transparent text and in total transparency the Strip Sync function is inhibited.</td>
</tr>
<tr>
<td>Bit</td>
<td>Function</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>----------</td>
<td>-------------</td>
</tr>
<tr>
<td>02</td>
<td>RECEIVE PRIMARY/SECONDARY (Rx P/S)</td>
<td>This bit is read/write and is cleared by Initialize and Master Clear. Indicates which of the Bus Address (BA) and Character Count (CC) Registers are being used or will be used. A zero indicates that the Primary registers are active; a one indicates that the Secondary registers are active. If a transfer is prematurely ended (i.e., the CC did not increment to zero, as in negating GO, or by a transfer ending flag, or by bit 7 of the Sequence Register), the Rx P/S bit will not flip to the next CC or BA registers. This bit is read only and is cleared (set to Primary register) by Initialize and Master Clear.</td>
</tr>
<tr>
<td>03</td>
<td>HALF-DUPLEX (HD)</td>
<td>The setting of this bit indicates that the DQ11 is in the half-duplex mode. When set, the Receiver is inhibited when Transmit Active is asserted. This bit is read/write and is cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>04</td>
<td>CHARACTER INTERRUPT ENABLE (CHAR IE)</td>
<td>When set, this bit allows the Character Detected Flag to generate a program interrupt on Vector A. This bit is read/write and is cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>05</td>
<td>RECEIVER DONE INTERRUPT ENABLE (Rx DONE IE)</td>
<td>If set, this bit allows interrupts to occur on Vector A, if Rx Done &quot;P&quot; or &quot;S&quot; is set. This bit is read/write and is cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>06</td>
<td>Rx DONE P(S) FLAGS &amp;</td>
<td>These flags are set when their respective character counts (P or S) overflow. These bits are also set by the DQ11-BB Character Recognition</td>
</tr>
<tr>
<td>Bit</td>
<td>Function</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>-------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>08</td>
<td>CHARACTER DETECTED thru</td>
<td>These four bits are used to latch character status which caused a character</td>
</tr>
<tr>
<td></td>
<td>(CHAR DET)</td>
<td>flag. They represent the switch-selected character flags in the DQ11</td>
</tr>
<tr>
<td>11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>RECEIVE ACTIVE</td>
<td>The setting of this bit indicates that the Receiver is in the data transfer</td>
</tr>
<tr>
<td></td>
<td>(Rx ACTIVE)</td>
<td>mode. The hardware becomes synchronized with the incoming data when it</td>
</tr>
<tr>
<td></td>
<td></td>
<td>recognizes one or two consecutive Sync characters. Additionally, active is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>set when synchronized or at the first non-Sync character after becoming</td>
</tr>
<tr>
<td></td>
<td></td>
<td>synchronized.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clearing Active forces re-synchronization if Rx GO is asserted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The shipping configuration will be synchronized on two consecutive sync</td>
</tr>
<tr>
<td></td>
<td></td>
<td>characters followed by Active on the first non-sync character.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>This bit is read/write and is cleared by Initialize, Master Clear, bit 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>of the Sequence Register, and when Rx GO is cleared.</td>
</tr>
<tr>
<td>13</td>
<td>USER OPTION</td>
<td>These bits are available as part of the Data Set control feature of the</td>
</tr>
<tr>
<td></td>
<td>&amp;</td>
<td>DQ11. They may be used for generating additional flags or for providing</td>
</tr>
<tr>
<td>14</td>
<td></td>
<td>additional modem control.</td>
</tr>
</tbody>
</table>
These bits are read/write and are cleared by Initialize and Master Clear.

15 CHARACTER FLAG

The Character Flag bit is set when a character is detected. (Reference description of bits 8 through 11.)

The bit will cause an interrupt if the Character Interrupt Enable bit (bit 4) is set.

The CHARACTER FLAG is read/write and is cleared by Initialize and Master Clear.

TRANSMIT STATUS REGISTER (Tx STAT)
Address: 76XXX2 (Addressable by word or byte)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>TRANSMIT GO (Tx GO)</td>
<td>When set, this bit enables transmit data transfers (NPR).</td>
</tr>
</tbody>
</table>

**NOTE:**
Reference bit 02 for Character Count (CC) information.

This bit is read/write and is cleared by:

1) Initialize
2) Master Clear

2-114
<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>IDLE MODE</td>
<td>If set, this bit allows the sending of IDLE* characters whenever Tx GO is zero. This bit is read/write and is cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>02</td>
<td>TRANSMIT PRIMARY/SECONDARY ACTIVE ( Tx P/S ACTIVE)</td>
<td>Indicates which of the Character Count and Bus Address Registers will be or are being used. A zero indicates that the Primary “P” Register is active; a one indicates that the Secondary “S” Register is active. When Character Count Register overflow occurs, the Character Count Register will switch (i.e., P→S or S→P). If the transfers are prematurely ended, as when clearing Tx GO, the Character Count Register will not switch and will be used again when Tx GO is re-asserted. This bit is read only and is cleared (set to “P” register) by Initialize and Master Clear.</td>
</tr>
<tr>
<td>03</td>
<td>ERROR INTERRUPT ENABLE (ERR IE)</td>
<td>When set, this bit enables interrupts on Vector “B” from the error flag. The error flag will be asserted when any of the error indicators are ON. They are as follows: VRC error, BCC error, Non-Existent Memory Latency, Clock Loss. This bit is read/write and is cleared by Initialize and Master Clear.</td>
</tr>
</tbody>
</table>

*Non-transparent mode: The IDLE character is the content of the Sync Register.
<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>04</td>
<td>DATA SET INTERRUPT ENABLE (DATA SET IE)</td>
<td>When set, this bit enables interrupts (Vector B) from the Data Set flag. The Data Set flag will be set from either the leading or trailing edge transitions of Carrier Detect (CO), Clear to Send (CS), or Ring. This bit is read/write and is cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>05</td>
<td>TRANSMIT DONE INTERRUPT ENABLE (Tx DONE IE)</td>
<td>If set, this bit allows interrupts to occur on Vector B if the Tx Done bit is set. This bit is read/write and is cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>06</td>
<td>TRANSMIT DONE &amp; PRIMARY SECONDARY</td>
<td>These bits are set when their respective character counts (P or S) overflow.</td>
</tr>
<tr>
<td>07</td>
<td>(Tx DONE P/S)</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:**
If Tx DONE is set by the Sequence Register, the Tx P/S (bit 2) will not change state.

These bits are read/write and are cleared by Initialize and Master Clear.

**NOTE**
Bits 08 through 15 are Data Set Control functions (Request to Send, Clear to Send, etc.) The DQ11 hardware will transmit and/or receive data independent of these control functions.

The Data Set control module has a strap which, when removed, inhibits Initialize from clearing Data Terminal Ready (DTR) and Request to Send (RS). The user should be aware of required modem and/or hardware delays before Request to Send (RS) can be negated. For instance, Bell 201A modems require a one-bit time delay following the last bit of transmission before negating RS. Due to double-buffered hardware, Tx DONE indicates that data transfers have been completed but not all data has been transmitted. All data has been transmitted only when Tx Active is negated (one-to-four character times after Tx DONE).

The function of each of the following Data Set control bits is given in the format of NAME(EIA/CCITT/PIN).
<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>08</td>
<td>REQUEST TO SEND (CA/105/4)</td>
<td>Request to Send (RS) is a transmit lead to the data communications equipment (Data Set). This control function is used to condition the local data communications equipment for data transmission and, on a half-duplex channel, to control the direction of data transmission. A program state change directed to RS will be presented to the Data Set on the next positive transition of the transmit clock. When the RS bit is set, an ON signal is transmitted. When cleared, an OFF signal is transmitted. This bit is read/write and is cleared by Initialize and Master Clear (if the jumper is in).</td>
</tr>
<tr>
<td>09</td>
<td>DATA TERMINAL READY (CD/108.2/20)</td>
<td>The Data Terminal Ready (DTR) bit controls switching of the data communications equipment to the communications channel. Auto dial and manual call origination: maintains the established call. Auto Answer: allows &quot;handshaking&quot; in response to a RING signal. This bit is read/write and is cleared by Master Clear and Initialize (if the jumper is in).</td>
</tr>
<tr>
<td>10</td>
<td>DATA SET READY (CC/107/6)</td>
<td>The Data Set Ready (also referred to as &quot;Modem Ready&quot; or &quot;Interlock&quot;) bit reflects the current state of the Data Set Ready lead. The Data Set Ready lead indicates that the modem is powered up and is not in the test, talk, or dial mode. This bit is read only; it is not affected by Initialize or Master Clear.</td>
</tr>
<tr>
<td>11</td>
<td>RING (CE/125/22)</td>
<td>This bit reflects the state of the data set ring lead. The trailing and leading edge of the ring lead will cause the data set flag to be set, and an interrupt will follow if the Data Set Interrupt Enable (IE) bit is set.</td>
</tr>
<tr>
<td>Bit</td>
<td>Function</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>-----------------------------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>12</td>
<td>CARRIER OR SIGNAL QUALITY DETECTOR (CF/109/8)</td>
<td>This bit reflects the current state of the Modern Carrier (CO) Control lead. An OFF indicates that no signal is being received or that the received signal is unsuitable for demodulation. The leading and the trailing edge of CO will cause the Data Set flag to be set, and an interrupt will follow if the Data Set IE bit is set. This bit is read only; it is not affected by Initialize or Master Clear.</td>
</tr>
<tr>
<td>13</td>
<td>CLEAR TO SEND (CB/106/5)</td>
<td>This bit reflects the current state of the Modem Clear to Send (CS) lead. An ON state indicates that the modem is ready to transmit data. The state of this lead is a direct result of the Request to Send lead. Also, CS is delayed from RS as a function of the type of modem and the type of lines used (four wire or two wire). The leading and the trailing edge of CS will cause the Data Set flag to be set, and an interrupt will follow if the Data Set IE bit is set. This bit is read only; it is not directly affected by Initialize or Master Clear (indirectly via RS).</td>
</tr>
<tr>
<td>14</td>
<td>USER OPTION</td>
<td>This bit is provided at the back panel for user connection of a non-standard status bit and/or program interrupt via the Data Set Flag. The back panel connection is TTL only and represents two standard TTL loads. This bit is read/write and is cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>15</td>
<td>DATA SET FLAG</td>
<td>If this bit is set and Data Set IE is asserted, an interrupt will occur on Vector &quot;B&quot;. The Data Set flag is asserted by the leading or trailing transitions of Ring, CO, and CS. This bit is read/write and is cleared by Initialize and Master Clear.</td>
</tr>
</tbody>
</table>
REG/ERR REGISTER
Address: 76XXX4 (Addressable by word or byte)

NOTE
The error bits described below generate an in-
terrupt request on Vector "B" if the Error Inter-
rupt Enable (ERR IE) bit (bit 03 of the Transmit
Status Register) is asserted.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Rx, Tx CLOCK LOSS ERROR</td>
<td>These bits (Rx or Tx) are set if the clock stops with Active set (Rx or Tx).</td>
</tr>
<tr>
<td>01</td>
<td></td>
<td>The clock loss flag will be set if GO is asserted without the clock or if the clock drops for more than 0.02 seconds while GO is true. Tx is bit 00, and Rx is bit 01. These bits are read/write and are cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>02</td>
<td>Rx, Tx LATENCY ERROR</td>
<td>These bits (Rx or Tx) are set if an NPR request is not serviced in less than one character time. The setting of this bit will clear the respective GO flip-flop. This error condition implies that the UNI-BUS is overloaded, is malfunctioning, or the Baud rate exceeds specifications. Tx is bit 02, and Rx is bit 03. These bits are read/write and are cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>03</td>
<td></td>
<td></td>
</tr>
<tr>
<td>04</td>
<td>Rx, Tx NON-EXISTENT MEMORY ERROR</td>
<td>These bits (Rx or Tx) are set if the DQ11, during an NPR cycle, addresses itself to a non-existent core memory location. This condition implies a program or hardware</td>
</tr>
<tr>
<td>Bit</td>
<td>Function</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>---------------------------------</td>
<td>-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>06</td>
<td>Rx BLOCK CHECK CHARACTER (BCC) ERROR</td>
<td>This bit is asserted if the BCC generated by the received message and the received BCC do not compare. When this bit is set, the Rx BCC is cleared (hardware function) and ready for the next message. Additionally, this does not affect Rx GO. It is recommended that a message retransmit be initiated when this form of error is detected. These bits are read/write and are cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>07</td>
<td>Rx VERTICAL REDUNDANCY CHECK (VRC) ERROR</td>
<td>This bit is set if the last received character had incorrect character parity. VRC is jumper selectable for even or odd parity; parity on/off is program selectable by bit 15 of the Miscellaneous Register. This bit is read/write and is cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>08</td>
<td>SECONDARY</td>
<td>These bits point to sixteen secondary registers for read/write operations. The selected register is accessed using select 6 (XXXXX6) with word transfers only. The following registers may be selected:</td>
</tr>
<tr>
<td></td>
<td>thru REGISTER</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>POINTER</td>
<td></td>
</tr>
</tbody>
</table>

**Bits (11-8)**  
**Octal #**  
**Register (Selected Via 76XXX6)**  

<table>
<thead>
<tr>
<th>Octal</th>
<th>Register Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Receive Bus Address (Rx BA)—Primary</td>
</tr>
<tr>
<td>1</td>
<td>Receive Character Count (Rx CC)—Primary</td>
</tr>
<tr>
<td>2</td>
<td>Transmit Bus Address (Tx BA)—Primary</td>
</tr>
<tr>
<td>3</td>
<td>Transmit Character Count (Tx CC)—Primary</td>
</tr>
</tbody>
</table>

2-120
<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Receive Bus Address (Rx BA) — Secondary</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Receive Character Count (Rx CC) — Secondary</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Transmit Bus Address (Tx BA) — Secondary</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Transmit Character Count (Tx CC) — Secondary</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Not used</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Sync</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Miscellaneous</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Transmit Buffer (Tx BUF)</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Not used</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Not used</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Not used</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Not used</td>
<td></td>
</tr>
</tbody>
</table>

These bits are read/write and are cleared by Initialize and Master Clear.

12 WRITE ENABLE FOR BITS 14 & 13 (14, 13 WRITE EN) When set, this bit allows the data written into bits 14 and 13 to be transferred to the scratch pad memories (Bus Address and Character Count) the next time select 6 is used. This bit is also self-clearing when the write-to-scratch-pad memory occurs.

This bit is read/write and is cleared by Initialize and Master Clear.

13 MEMORY EXTENSION OR ENTER & T/EXIT T

The Bus Address (BA) and Character Count (CC) registers are 18-bit registers. Bits 14 and 13 with bit 12 provide a means of reading and/or writing the BA and CC bits (bits 17, 16 are bits 14 and 13, respectively). In addition, the register pointer bits (bits 11 through 8) determine what CC or BA is to be accessed.

MEMORY EXTENSION: Bits 14 and 13 are address lines A16 and A17, respectively. These two bits are the read/write ports for transmit and receive. The proper port is selected (Rx or Tx) when the register bits are addressed to the desired Bus Address Register. See description of bits 10 through 8.

2-121
<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ENTER T (14)</td>
<td>Enter transparency forces transparency (block transfers) and inhibits all character recognition. This function is used if a message to be transmitted (or received) is completely transparent to all data and control characters.</td>
</tr>
<tr>
<td></td>
<td>EXIT T (13)</td>
<td>If set, this exit transparency bit allows exit from the transparent mode and enables character recognition. This function is used as a companion to ENTER T or used in protocol hardware control (as in BISYNC or ASCII standards).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The ENTER T and EXIT T bits execute their respective functions when the character counts are tested for non-zero by the hardware. This occurs when the current Character Count Register transitions to zero or at the first transfer following the assertion of GO.</td>
</tr>
<tr>
<td>15</td>
<td>ERROR INTERRUPT</td>
<td>Bits 14 and 13 Read always represent the contents of the respective addressed scratch pad memories. (Select 6 must be used to transfer a write to bits 14 and 13 into the scratch pad memories.)</td>
</tr>
<tr>
<td></td>
<td>(ERR INTR)</td>
<td>This error flag is set if any of the error bits are asserted. The error bits are for VRC, BCC, Rx/Tx Non-Existential Memory, Rx/Tx Latency, and Rx/Tx Clock Loss.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>This bit is read only and presents a zero when all the error bits are zero and when Master Clear or Initialize has been issued.</td>
</tr>
</tbody>
</table>

**SECONDARY REGISTERS (SEC REG)**
Address: 76XXX6 (Addressable by word only)

The Secondary Registers listed below are addressed by setting bits 8 through 11 of the REG/ERR Register (Select 4) to the appropriate value.
<table>
<thead>
<tr>
<th>Register Octal Address</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Receive Bus Address (Rx BA)—Primary</td>
</tr>
<tr>
<td>1</td>
<td>Receive Character Count (Rx CC)—Primary</td>
</tr>
<tr>
<td>2</td>
<td>Transmit Bus Address (Tx BA)—Primary</td>
</tr>
<tr>
<td>3</td>
<td>Transmit Character Count (Tx CC)—Primary</td>
</tr>
<tr>
<td>4</td>
<td>Receive Bus Address (Rx BA)—Secondary</td>
</tr>
<tr>
<td>5</td>
<td>Receive Character Count (Rx CC)—Secondary</td>
</tr>
<tr>
<td>6</td>
<td>Transmit Bus Address (Tx BA)—Secondary</td>
</tr>
<tr>
<td>7</td>
<td>Transmit Character Count (Tx CC)—Secondary</td>
</tr>
<tr>
<td>10</td>
<td>Not used</td>
</tr>
<tr>
<td>11</td>
<td>Sync</td>
</tr>
<tr>
<td>12</td>
<td>Miscellaneous</td>
</tr>
<tr>
<td>13</td>
<td>Transmit Buffer (Tx BUF)</td>
</tr>
<tr>
<td>14</td>
<td>Not used</td>
</tr>
<tr>
<td>15</td>
<td>Not used</td>
</tr>
<tr>
<td>16</td>
<td>Not used</td>
</tr>
<tr>
<td>17</td>
<td>Not used</td>
</tr>
</tbody>
</table>

A functional description of each of the above secondary registers is presented in the remainder of this section.

**CHARACTER COUNT (CC)—REGISTERS 1, 3, 5, and 7**

**BUS ADDRESS (BA)—REGISTERS 0, 2, 4, and 6**

The BA register for transmit and receive must be started on even boundaries. However, the BA (and CC) registers may end on either odd or even boundaries.

The CC and BA registers for transmit and receive are double buffered, thus reducing peak load response to CC overflow.

CC and BA are 16-bit registers. The BA Register is extended to 18 bits by the Memory-Extension bits; the CC Register is extended to 18 bits by the ENTER T and EXIT T bits in the REG/ERR Register.

These bits are read/write and are not cleared by Initialize or Master Clear. They must be cleared by a program initialization procedure.

When an Initialize or Master Clear is issued, the Primary/Secondary (P/S) flip-flops select the primary CC and BA registers. When CC overflow occurs, the Secondary Register (Tx or Rx—whichever overflowed) will be selected. Data transfers will cease, and GO will be cleared when the flip to the next Character Count (CC) register occurs and is found to be zero. The next “GO” will start with the last selected CC (the one that terminated the last “GO”).

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NOTE

The hardware does not require or expect the Primary/Secondary (P/S) registers for transmit and receive to be in phase except following Master Clear and Initialize.

<table>
<thead>
<tr>
<th>Bits 15 - 8</th>
<th>Bits 7 - 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>DLE</td>
</tr>
<tr>
<td>1</td>
<td>ITB</td>
</tr>
<tr>
<td>2</td>
<td>ETB</td>
</tr>
<tr>
<td>3</td>
<td>ETX</td>
</tr>
<tr>
<td>4</td>
<td>EOT</td>
</tr>
<tr>
<td>5</td>
<td>ENQ</td>
</tr>
<tr>
<td>6*</td>
<td>DLE</td>
</tr>
<tr>
<td>7</td>
<td>SOH</td>
</tr>
<tr>
<td>8</td>
<td>NAK</td>
</tr>
<tr>
<td>9</td>
<td>ACK0</td>
</tr>
<tr>
<td>10</td>
<td>ACK1</td>
</tr>
<tr>
<td>11</td>
<td>RV1</td>
</tr>
<tr>
<td>12</td>
<td>WACK</td>
</tr>
<tr>
<td>13</td>
<td>NOT USED (SEQ = 0)</td>
</tr>
<tr>
<td>14</td>
<td>NOT USED (SEQ = 0)</td>
</tr>
<tr>
<td>15</td>
<td>NOT USED (SEQ = 0)</td>
</tr>
</tbody>
</table>

*Required for SEQ 9.

These bits are read/write and are NOT cleared by Initialize and Master Clear.

SYNC REGISTER—REGISTER 11

The Sync Register is programmable for up to sixteen bits. Unused bits must be set to zero. If characters less than or equal to eight bits are used, then the odd and even bytes should contain the same Sync character. The Least Significant Bit (LSB) is right-justified, as are the data bits.

These bits are Read Write and are cleared by Master Clear and Initialize.
### MISCELLANEOUS REGISTER—REGISTER 12

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>SHIFT CLOCK</td>
<td>The Shift Clock is a maintenance function. The transmitter shifts when this bit is set to ONE (transition to), and the receiver strobes data when this bit is set to zero (transition to). This bit is read/write and is cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>01</td>
<td>STEP MODE</td>
<td>This bit selects the clocking source for the test loop. See description of bit 3. If this bit is zero, the auto clock source is selected. The source for the auto clock is approximately 14KC RC clock if loop mode is also selected. If loop mode is not selected, the source clock will be the serial clock transmit and serial clock receiver leads. If this bit is a one, the Shift Clock (bit 00) will be the clock source. This bit is Read/Write and is cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>02</td>
<td>NOT USED</td>
<td>If set, this bit causes the transmitter to loop back to the receiver. This bit is Read/Write and is cleared by Initialize and Master Clear.</td>
</tr>
<tr>
<td>03</td>
<td>TEST LOOP</td>
<td></td>
</tr>
</tbody>
</table>

2-125
<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>04</td>
<td>RECEIVE NON-PROCESSOR REQUEST (Rx NPR)</td>
<td>The Rx NPR bit is a maintenance function. It is intended for use when Receiver Active is zero. A one written into this bit forces an Rx NPR. The data transferred to core will be the contents of the receiving shift register (not the buffer) and the Bus Address (BA) and Character Count (CC) will be updated. This bit is a write ones only and always reads as a zero.</td>
</tr>
<tr>
<td>05</td>
<td>MASTER CLEAR</td>
<td>The Master Clear function resets all active functions and flags in the DQ11. The CC, BA, MEM EXT, ENTER T, EXIT T, CHAR DET, and the SEQ are not cleared by Master Clear. This bit is a write ones only and always reads as a zero.</td>
</tr>
<tr>
<td>06</td>
<td>POLYNOMIAL 16-23</td>
<td></td>
</tr>
<tr>
<td>07</td>
<td>SEND DATA (SD)</td>
<td>This bit always monitors the transmitted data if the test loop is selected. In addition, if the Transmit Active bit is a zero, this bit is Read/Write and can be used to directly test the receiver as a maintenance function. A zero equals MARK and a ONE equals SPACE. This bit is Read/Conditional Write and is cleared by Initialize and Master Clear.</td>
</tr>
</tbody>
</table>
Bits per character selection is made via bits 11, 10, 9, and 8 as follows:

<table>
<thead>
<tr>
<th></th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>Bits per character</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>16</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>15</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>14</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>13</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>12</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>11</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>10</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>8</td>
</tr>
<tr>
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<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>7</td>
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<td>0</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
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<td>1</td>
<td>1</td>
<td>5</td>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

These bits are Read/Write and are cleared by Initialize and Master Clear.
<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>SYNC 2</td>
<td>SYNC 2 will be set if the receiver is synchronized (framed). This bit is read only and is cleared by Initialize, Master Clear, and by clearing Active.</td>
</tr>
<tr>
<td>13</td>
<td>SYNC 1</td>
<td>SYNC 1 will be set if the receiver has received one SYNC character. A jumper is provided to enable SYNC 1 to direct set SYNC 2, causing framing to be completed. If the jumper is not installed, SYNC 1 will condition SYNC 2 to be set if the next received character is another SYNC. If the next received character is not a SYNC, then SYNC 1 will be cleared, and a bit-by-bit search will continue for another SYNC character. This bit is read only and is cleared by Initialize, Master Clear, and by clearing Active.</td>
</tr>
<tr>
<td>14</td>
<td>Tx ACTIVE</td>
<td>When set, this bit indicates that the transmitter is in the process of transmitting a character; it will remain set until all characters and/or bits have been transmitted. This bit is cleared by Initialize, Master Clear, and lack of data to transmit.</td>
</tr>
<tr>
<td>15</td>
<td>VERTICAL REDUNDANCY CHECK (VRC)</td>
<td>When set, the VRC bit selects parity to be generated (transmit) and checked (receive) in the most significant bit position of the selected character. VRC odd/even is switch-selectable. When VRC is used, PAD or FILL characters must have correct VRC or an error will be flagged. This bit is Read/Write and is cleared by Master Clear and Initialize.</td>
</tr>
</tbody>
</table>

**TRANSMIT BUFFER (Tx BUF)---REGISTER 13**

The Transmit Buffer is a 16-bit, read-only maintenance register which monitors the parallel input to the Transmit Shift Register (i.e., the Transmit Buffer).

These bits are cleared by Initialize and Master Clear.
SPECIFICATIONS

Function
The DQ11 provides a two-way communications interface between the PDP-11 UNIBUS and a serial synchronous transmission line.

Type
Double-buffered, Transmit and Receive, Serializer/Deserializer.

Operating Mode
Full- or half-duplex.

Transmission Speeds
EIA RS-232-C—Up to 10,000 bits per second, Current Mode Operation—Up to 1 million bits per second.

Clocking
Synchronous clock from the modem (internal Crystal clock optional).

Sync Character
Program selectable.

Sync Detection
Activates on first non-sync character following one or two successive sync characters, or immediately upon detecting one or two successive sync characters (switch selectable).

Order of Bit Transmission
Low order bit first.

Error Detection
VRC (odd or even) for transmit and receive; jumper selectable. VRC (ON/OFF) is a program function.

Character Recognition
Three switch-selectable characters for generating program interrupts.

Program Interrupts
Program interrupts on RING, Carrier Detect, Clear to Send, Transmit/Receive DONE, Character Flag, and errors.

Character Size
Up to 16 bits per character, program selectable.

Double character transfers when eight bits (or less) per character are selected.

Bus Address
Bus Address (BA) may be set to any 128K word address.

Character Count
Character Count (CC) may be set for up to 65,536 characters.

UNIBUS Loads
The DQ11 System Unit presents one load to the PDP-11 UNIBUS.
**Power Requirements**
Basic System Unit: +5 V at 6.0 A  
+15 V at .04 A  
−15 V at .07 A

**Temperature & Humidity Range**
10 to 50° C with up to 90% non-condensing relative humidity.

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>DEC No.</th>
<th>Description</th>
<th>Prerequisite</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQ11-DA</td>
<td>Full-half-duplex synchronous line module set. EIA/CCITT termination suitable for direct use with Bell System 201 or equivalent modems. Transmission speeds up to 10,000 Baud. Data Set control included. Supplied with 7.6m (25-foot) modem cable.</td>
<td>PDP-11</td>
</tr>
<tr>
<td>DQ11-EA</td>
<td>Full-half-duplex synchronous line module set. TTL to Bell System 303 or equivalent modems. Transmission speeds up to 1 million bits per second. Data Set Control included. Supplied with 7.6m (25-foot) modem cable.</td>
<td>PDP-11</td>
</tr>
</tbody>
</table>
SYNCHRONOUS LINE INTERFACE, DU11

FEATURES
- Transmission speeds up to 9600 bits per second
- Double-buffered program interrupt
- Full- or half-duplex operation
- Programmable Sync character
- Programmable character size (5, 6, 7, or 8 bits)
- Receiving Sync character stripping program selectable
- Automatic transmit of Sync program selectable
- Interfaces to Bell Series 200 synchronous modems or equivalent
- Auto answering capability
- Parity checking and generation
- Modem control
- Simple, compact, single-board design

INTRODUCTION
The DU11 is a single-line, program-controlled, double-buffered communications device designed to interface the PDP-11 Processor to a serial synchronous line. The self-contained unit is fully programmable with respect to Sync character, character length (5 to 8 bits), and parity selection.

The DU11 is ideally suited for interfacing the PDP-11 to high-speed synchronous lines for remote batch, remote data collection, and remote
DU11 concentration applications. Multiple DU11's on a PDP-11 allow its use as a synchronous line concentrator or front-end synchronous controller to a larger computer.

The DU11 provides serial-to-parallel and parallel-to-serial data conversion, voltage level conversion, and modem control for half- or full-duplex operation. The Bell Series 200 synchronous modems or equivalent may be used with the DU11.

Modem control is a standard feature of the DU11. The necessary signals needed to establish communications with the Bell Series 200 synchronous modems are present in the Receive Status Register (RxCSR). No transition of control lines emanating from the modem directly cause a change in the state of the transmitter or receiver logic.

The DU11 is capable of transmitting data at the following speed:

EIA/CCITT: 9600 bits per second maximum
(limited by modem and data set interface level converters)

The DU11 conforms to Electronic Industries Association (EIA) specification RS-232-C and CCITT Recommendation V.24.

OPERATION

General
The DU11 is a character buffered synchronous serial line interface capable of two-way simultaneous communications. The DU11 translates between serial data and parallel data. Output characters are transferred in parallel from the PDP-11 UNIBUSTM into the DU11 where they are serially shifted to the communication line. Input characters from the modem are shifted into the DU11 and made available to the PDP-11 on an interrupt basis.

Synchronization between the DU11 and the transmitting device is established by a Sync character code. Both the receiver and transmitter are double buffered. This allows a full character time in which to service transmitter and receiver interrupts. The clocking necessary to serialize the data is provided by the associated high-speed synchronous modem.

The DU11 consists of five registers: two status registers, two data buffer registers, and a Parameter Control Register which is used to control characteristics of the interface such as mode of operation (synchronous internal or external), number of bits per character, parity selection, and the Sync character.

Synchronous Mode—Transmitter Section
The transmitter section of the DU11 performs parallel-to-serial conversion of data supplied to it from the PDP-11 UNIBUS.
After the initialize pulse, the program must set the Parameter Control Register for the mode of operation (in this case synchronous), the desired character length (5, 6, 7, or 8 bits—parity not included), and the mode of parity.

Before any necessary handshaking with the data set, the program may load the Sync Register with the desired character. When the Sync Register is loaded, the character will be used for both the Receiver and Transmitter operations. Any required handshaking to establish connection with the data set may be done at this time.

Once handshaking is complete, the program can assert the Send bit in the Transmitter Status Register (TxCSR). When Send is asserted, the transmitter is enabled but will not start transmitting data until the first character is loaded into the Transmitter Data Buffer (TxBFVF). If Send is cleared during transmission, the character currently being transmitted will be completed, the line will go to a mark hold state, the internal transmitter logic will be reset, and synchronization will be lost. When Send is cleared, there is no guarantee that the Transmitter Done bit will assert upon completion of transmission of the current character.

When it is necessary to know when the last bit of the last character has been transmitted, the following steps may be taken: Prior to loading the Transmitter Data Buffer (TxBFVF) with the last character, the DNA INTR EN (Data Not Available Interrupt Enable) bit should be asserted in the Transmitter Status Register (TxCSR) and the Tx DONE INTR EN bit should be cleared. The interrupt in the transmitter logic subsequent to the loading of the TxBFVF will signify the completion of the transmission of the last character.

The transmission of initial Sync characters may be accomplished through either of the following two methods:

1. The program must arrange its data buffer such that the required number of Sync characters precedes any text. The Sync Register may or may not contain the Sync character. If the Sync Register is not loaded, it will contain an all-ones character subsequent to a master reset or initialize.

Assuming that any necessary handshaking has been completed with the data set and that Send has been asserted, the program can commence transmission from its data buffer.

When the first data bit is transferred to the communications line, the Transmitter Done bit will be asserted. If the Transmitter Interrupt Enable bit is set, an interrupt request will be generated.

If the Sync character was not initially loaded into the Sync register, then synchronization cannot be guaranteed unless the program response to the Transmitter Done Bit is less than 1/Baud x (bits per character—1½ bit time) seconds. This can be verified by the absence of the Data Not Available (DNA) bit in the TxCSR and applies only to the transmission of the initial Sync characters.
Subsequent synchronization can be maintained by having the program insert Sync characters into the message at the established intervals.

An alternate method of maintaining subsequent synchronization would be to load the Sync Register with the Sync character and assert the Data Not Available Interrupt Enable bit in the TxCSR. The program could ignore the service of the Transmitter Done bit at certain intervals by clearing the Transmitter Done Interrupt Enable bit. During this interval, transmission would be from the Sync Register. When transmission from the Sync Register begins, the Data Not Available bit will assert, causing an interrupt request. As long as the program ignores the Transmitter Done Bit, transmission will emanate from the Sync Register.

If desired, the program can ignore the Data Not Available bit by clearing its Interrupt Enable.

2. Following any necessary handshaking procedure and the assertion of Send, the program loads the Sync Register with the Sync character and asserts Data Not Available Interrupt Enable. The program then clears the Transmitter Done Interrupt Enable (if it was set) and then loads TxDBUF with the Sync character. At this point, transmission begins. No interrupt request will be generated by the transmission of the first character unless the Transmitter Done Interrupt Enable bit is set. The first bit of the second character will cause an interrupt request. At this point, one Sync character has been transmitted. It is suggested that a minimum of five Sync characters be transmitted. In systems that are prone to error because of lost synchronization, as many as twelve Sync characters may be desired.

If more than one Sync character is required to achieve synchronization, the Data Not Available Interrupt requests can be monitored by the program. These requests will be continuous as long as the Transmitter Done bit goes unserviced and the Data Not Available Interrupt Enable bit is asserted.

Once synchronization has been established, subsequent synchronization can be maintained by delaying service of Transmitter Done and monitoring the Data Not Available bit.

Once synchronization is achieved, transmission of text will follow only if the program loads the text into the TxDBUF.

An intrinsic feature of the DU11 is its ability to maintain synchronization even if the TxDBUF has not been updated. This is done by the transmitter idling out the contents of the Sync Register if the TxDBUF has not been updated in 1/Baud x (bits per character—½ bit time) seconds).

This means that if the transmitter were not serviced in the previously stated time frame, transmission would include data from the Sync Register. If this situation occurs, the Data Not Available bit will be set in the
TxCSR. If desired, the program may set the DNA INTR EN bit and cause interrupt requests when Data Not Available comes true.

**NOTE**
The Send bit in the TxCSR must remain set for the duration of the message. An on-to-off transition will cause the transmitter to enter an idle state after completion of the character currently being transmitted.

**Synchronous Mode—Receiver Section**
The Receiver Section of the DU11 performs serial-to-parallel conversion of 5, 6, 7, and 8-level codes.

**SYNC INTERNAL MODE**
The Parameter Control Register (PARCSR) controls both the transmitter and receiver configurations. Once the program has completed any necessary handshaking with the data set, the receiver data handling logic can be enabled. This is done by the program asserting Search Sync in the Receiver Status Register (RxCSR). This also enables the receiver to compare incoming characters with the character held in the Sync Register.

For the receiver to become synchronized with the transmitter, either one or two consecutive Sync characters must be recognized by the receiver. The number of characters is jumper selectable.

**NOTE**
Standard configurations will be set for two characters.

When this has happened, the Receiver Active bit will assert. Any characters received after Receiver Active has been asserted will cause interrupt requests, providing Receiver Interrupt Enable is set and the Strip Sync bit is not asserted.

**NOTE**
Search Sync must remain set for the duration of the message. If not, the character being received at the time of the on-to-off transition will be lost along with synchronization.

In some instances, the user may want the receiver to ignore Sync characters. This can be accomplished, providing the Receiver Active bit is set. First, the Sync character must be loaded into the Sync Register; then the Strip Sync bit in the RxCSR must be asserted. No interrupt requests will be generated when this character is received, although it does appear in the RxDBUF until the next character is received. If bit 15 of the Receiver Data Buffer (RxDBUF) is asserted (signifying an error), the received Sync character will not be stripped and the RxDone bit will be asserted.

Overrun errors will occur in the receiver logic if the Receiver Done bit in the Receiver Status Register (RxCSR) is not serviced in 1/Baud x (bits
per character) seconds. When the overrun condition occurs, the character previously in RxDBUF is written over by the character causing the overrun.

**SYNC EXTERNAL MODE**

In this mode, the Parameter Control Register must be set for SYNC EXTERNAL. Refer to the description of the Mode Select bits for the actual setting. When the SYNC EXTERNAL mode has been selected, only the operation of the receiver logic differs; transmitter operation remains the same as described above. This is the only mode of operation in which the programs can force synchronization.

When the programmer asserts Search Sync, the Receiver Active bit will also assert even though no actual Sync characters have been received. If Search Sync is cleared, Receiver Active will also be cleared. Prior to the assertion of Search Sync the Receiver Data Buffer (RxDBUF) will appear as the serial line; that is, data will shift through the RxDBUF at the rate of the modem. No action in the receiver logic will result from this data being shifted, although the program can monitor this data stream. When the Search Sync bit is asserted, the receiver logic will start framing characters on the first bit received after Search Sync was asserted. The serial streams that appeared in the RxDBUF will be discontinued, and the Receiver Done bit will be asserted when the selected number of bits have been received. The received character will appear in the RxDBUF. Other than the differences mentioned, all other parameters and features of the synchronous receiver are applicable.

**PROGRAMMING**

The five registers and their addresses are listed below:

1. Receiver Status Register (RxCSR) 16XX40
2. Receiver Data Buffer Register (RxDBUF) 16XX42
3. Parameter Control Register (PARCSR) 16XX42
4. Transmitter Status Register (TxCSR) 16XX44
5. Transmitter Data Buffer Register (TxDBUF) 16XX46

All information between the DU11 and the PDP-11 CPU is transmitted in parallel fashion by byte or word. The RxCSR and TxCSR are addressable by word or byte. The PARCSR is write only by word operation. The RxDBUF is read only by word or byte. The TxDBUF is write only by word or byte to the even address only.

Data transfer is under program control. All data is transferred by the program (not an NPR device). Four contiguous UNIBUS addresses are required in the floating address area. Two contiguous interrupt vector addresses are required in the floating vector address area. The first vector of the set will have priority over the second if two interrupt requests are made simultaneously. The first vector will deal with conditions in the RxCSR. The second vector will deal with conditions in the TxCSR.
The initialize signal from the UNIBUS will generate a Master Reset in the DU11. A description of the Master Reset bit and the bit assignments within each register are presented in the remainder of this section.

**RECEIVER STATUS REGISTER (RxCSR)**

Address: 16XX40 (Addressable by word or byte)

<table>
<thead>
<tr>
<th>Bit 15</th>
<th>Bit 14</th>
<th>Bit 13</th>
<th>Bit 12</th>
<th>Bit 11</th>
<th>Bit 10</th>
<th>Bit 9</th>
<th>Bit 8</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
</table>

- **Bit 00**: RESERVED
- **Bit 01**: DATA TERMINAL READY
  When set, this bit causes the data terminal lead to be asserted to the modem. Auto Dial and Manual call origination: maintains the established call. Auto Answer: allows hand-shaking in response to a ring signal.

  This bit is program read/write and is optionally cleared by INIT or Master Reset.

- **Bit 02**: REQUEST TO SEND
  When set, this bit causes the Request to Send lead to be asserted at the modem interface.

  This bit is program read/write and is optionally cleared by INIT and Master Reset.

- **Bit 03**: SECONDARY TRANSMIT DATA
  This bit is connected to the secondary transmit line of the modem. With certain modems, supervisory data can be transmitted over this line at a reduced rate. It can also be used as a control lead; e.g., acknowledgement of messages.

  This bit is program read/write and is optionally cleared by INIT or Master Reset.

- **Bit 04**: SEARCH SYNC
  SYNC INTERNAL MODE: When asserted to the receiver, this bit causes the receiver to start examining incoming characters for the Sync code held in the Sync Register. After the selected number of Sync characters are recognized, the Receiver Active bit is set. Either one or two Sync characters may be selected. The characters must be contiguous.
SYNC EXTERNAL MODE: In this mode, the Receiver Active bit will assert at the same time the Search Sync bit is asserted. Character framing will start with the first bit received after Search sync has been asserted; character framing ends after the number of bits per character specified in the word length (select bits of the PARCSR) have been received.

Once Receiver Active is asserted, this bit must stay asserted or synchronization will be lost, and the receiver will go into an idle state.

This bit is program read/write and is cleared by INIT and Master Reset.

**Bit 05**

DATA SET INTERRUPT ENABLE
When set, this bit allows interrupt requests to be made to the receiver vector if the Data Set Change bit is asserted.

This bit is program read/write and is cleared by INIT or Master Reset.

**Bit 06**

RECEIVER INTERRUPT ENABLE
When set, this bit allows interrupt requests to be made to the receiver vector if the Receiver Done bit is set.

This bit is program read/write and is cleared by INIT or Master Reset.

**Bit 07**

RECEIVER DONE
This bit is set when a character is transferred into the Receiver buffer. If, however, the Receiver Active bit is set and the Strip Sync bit is a one, and the character received is a Sync character, the Receiver Done bit will not be set, providing bit 15 of the RxDBUF is clear.

This bit is program read/only and is cleared by reading RxDBUF, INIT, and Master Reset.

An Interrupt request will be generated if the Receiver Interrupt Enable bit is set when this bit is asserted.

**Bit 08**

STRIP SYNC
When this bit is set, characters that match the contents of the Sync Register will be ignored, provided bit 15 of the Receive Data Buffer Register is not asserted. In this case, the Receiver Done bit will not be asserted.

This bit is program read/write and is cleared by INIT or Master Reset.

**Bit 09**

DATA SET READY
This bit is a direct reflection of the Data Set Ready (or interlock) lead emanating from the modem. This line, when asserted, indicates that the modem is powered up, and is not
in the test, talk, or dial mode. Any transition of this bit will cause the Data Set Change bit to be asserted.

Program read only.

Bit 10  SECONDARY RECEIVED DATA
This bit reflects the state of the Secondary Received Data line emanating from the modem. Any transition on this line will cause the Data Set Change bit to assert. With certain modems, supervisory data can be received over this line at a reduced rate. It can also be used as a control lead; e.g., acknowledgment of messages.

Program read only.

Bit 11  RECEIVER ACTIVE
When operating in the synchronous mode using internal synchronization, this bit will be set when the selected number of contiguous Sync characters have been recognized (either 1 or 2). If the Sync EXTERNAL mode were selected, the Receiver Active bit will follow the state of the Search Sync bit.

This bit is program read and is cleared by INIT and Master Reset.

Bit 12  CARRIER
This bit is a direct reflection of the modem carrier. Any change in the status of this line causes the Data Set Change bit to be asserted.

Program read only.

Bit 13  CLEAR TO SEND
This bit reflects the state of the clear-to-send line of the modem. Any transition of this line causes the Data Set Change bit to set.

Program read only.

Bit 14  RING INDICATOR
This bit reflects the state of the modem ring line. Any transition of this line causes the Data Set Change bit to set.

Program read only.

Bit 15  DATA SET CHANGE
This bit is set by a transition on the following lines:

- Any transition on the Ring line.
- Any transition on the carrier line.
- Any transition on the Data Set Ready line.
- Any transition on the Clear-to-Send line.
- Any transition of the Secondary Received Data.
If bit 05 of this register is set, the assertion of this bit will cause an interrupt to the receiver vector. This bit is cleared only by INIT, Master Reset, or when the RxCSR is read.

**RECEIVER DATA BUFFER REGISTER (RxDBUF)**
Address: 16XX42 (Read Only—Addressable by word or byte)

---

**Bits 00–07**
RECEIVER DATA BUFFER
This buffer contains the data received from the modem with character lengths from 5-to-8 bits, plus parity if selected. The parity bit, if any, will be included as part of the received character and will appear as the bit following the most significant bit. In the case of 8-bit characters, no parity bit will be displayed.

The character in the RxDBUF is right-hand adjusted; bit 00 is the least significant bit of any character, and bit 07 is the most significant bit of an 8-bit character. Subsequent to a Master Reset, this register contains all ones.

Program read.

**Bits 08–11**
RESERVED

**Bit 12**
PARITY ERROR
This bit is set when the receiver detects a parity error in the character received. The character will appear in the RxDBUF. The parity bit itself is available to the program for character length selection for less than 8 bits per character.

This bit is program read and is cleared by INIT, Master Reset, and by reading the RxDBUF low byte.

**Bit 13**
RESERVED

**Bit 14**
OVERRUN
When the receiver logic detects an overrun condition, this bit is set. An overrun is caused primarily by poor program response time.

Once the Receiver Done bit is set, the program must respond in 1/BPS x (Bits per character) seconds. If not, overrun will occur. This condition indicates the loss of at least one character. This bit will cause the error bit to assert.
DU11

This bit is program read only and is cleared by reading the RxDBUF low byte, INIT, or Master Reset.

Bit 15  ERROR
This bit will be asserted if one of the three error bits in the RxDBUF are set (logical OR of bits 14 and 12).

This bit is program read only and is cleared only when bits 14 and 12 are clear.

PARAMETER CONTROL REGISTER (PARCSR)
Address: 16XX42 (Write only—addressable by word only)

NOTE:
If this register is inadvertently addressed with a byte operation, both bytes of the UNIBUS will be loaded. The unspecified byte may contain unwanted data.

The following bits are used to control the characteristics of the interface. These include mode of operation (synchronous internal or synchronous external), number of bits per character, and parity selection. These bits are in an undefined state after power-up until programmed.

Bits
00-07  SYNC REGISTER
This register contains the Sync character to be transmitted and used for receiver synchronization by the interface. The length of this character must correspond to the length of the data character. Parity does not have to be included if it has been selected.

Subsequent to a master reset, the internal transmitter Sync register will contain all ones; the receiver's internal Sync register will contain all zeros.

Character length is adjusted from right to left, with bit 00 being the least significant bit and bit 07 the most significant bit for an 8-bit character.

Program write only.

Bit 08  EVEN PARITY SELECT
When the Parity Enable bit (bit 09) is set, the sense of the parity is controlled by this bit. When set, even parity will be
generated by the transmitter and checked for by the receiver. The same will be done for odd parity when cleared.

Program write.

Bit 09  PARITY ENABLE
If this bit is set, parity generation and checking will be done. If bad parity is detected at the receiver, then the parity error flag will be set in the upper byte of the Receiver Data Buffer Register (RxDBUF).

Program write.

Bits 10 & 11  WORD LENGTH SELECT
These bits are used to select the number of bits per character, either 5, 6, 7, or 8. This selection does not include the parity bit, if parity is selected.

<table>
<thead>
<tr>
<th>Bits Per Character</th>
<th>PARCSR</th>
<th>Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Program write.

Bits 12 & 13  MODE SELECT 01, 00
The function of these bits is to select the mode of operation: synchronous internal or synchronous external. The following table shows the legal configurations possible with the DU11. All other combinations of the mode select bits will produce errors in the interface.

<table>
<thead>
<tr>
<th>MODE</th>
<th>PARCAR</th>
<th>Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synchronous External</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Synchronous Internal</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Program write.

Bits 14 & 15  RESERVED
BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY
IF MAILED IN THE UNITED STATES

Postage will be paid by:

DIGITAL EQUIPMENT CORPORATION
SALES SUPPORT LITERATURE GROUP
PK3-2/M-88
MAYNARD, MASS. 01754

FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.
Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our handbooks.

What is your general reaction to this manual? (format, accuracy, completeness, organization, etc.)

________________________________________________________________________

________________________________________________________________________

________________________________________________________________________

What features are most useful?

________________________________________________________________________

________________________________________________________________________

________________________________________________________________________

Does the publication satisfy your needs?

________________________________________________________________________

________________________________________________________________________

________________________________________________________________________

What errors have you found?

________________________________________________________________________

________________________________________________________________________

________________________________________________________________________

Additional comments

________________________________________________________________________

________________________________________________________________________

________________________________________________________________________

Name

Company

Dept.

Title

City

State

Zip

(staple here)
TRANSMITTER STATUS REGISTER (TxCSR)
Address: 16XX44 (Addressable by word or byte)

Bit 00 BREAK
When this bit is asserted, the serial output of the transmitter is held in the space condition. If the program presents data to the transmitter during this period, the operations to the program will appear normal. An interrupt request will be generated at the normal time even though a character was never actually transferred.

NOTE:
The setting of this bit is not recommended when operating in the synchronous mode except for maintenance programming.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 01 RESERVED

Bit 02 RESERVED

Bit 03 HALF DUPLEX/FULL DUPLEX
When this bit is set, operation will be in the half-duplex mode. In the half-duplex mode, the receiver will be disabled if the Send bit in the TxCSR is asserted.

This bit is read/write and is cleared by INIT or Master Reset.

Bit 04 SEND
When asserted, this bit enables the transmitter. Once the transmitter is enabled, transmission will start when the first character has been loaded into the TxDBUF. This line must remain true for the length of the entire message. If not, the current character in the shift register will be transmitted, and the transmitter will go into an idle state.

This bit is used in all modes of operation.

This bit is program read/write and is cleared by Master Reset or INIT.

2-143
Bit 05  DNA INTR EN (DATA NOT AVAILABLE INTERRUPT ENABLE)
Allows interrupt requests to be made to the transmitter vector if the Data Not Available bit is set. This bit is set if the user wants to know if a filler character was sent while in data mode via an interrupt or to notify the program when the last bit of a character has been transmitted.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 06  TRANSMITTER INTERRUPT ENABLE
When set, this bit will allow a program interrupt request to be generated by the Transmitter Done bit.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 07  TRANSMITTER DONE
This bit will be set when the first bit of the character contained in the TxDBUF is presented to the line. At that time, the program can load another character into the transmitter buffer.

If the transmitter interrupt enable bit is set, this bit will generate an interrupt request to the transmitter vector.

Program read. Cleared by writing a character into the TxDBUF. Reset by INIT or Master Reset.

Bit 08  MASTER RESET (MR)
This bit is used to place the transmitter and receiver in an idle state (not to be confused with idle mode). The UNIBUS Initialize signal will also place the DU11 in an idle state.

When the transmitter is placed in an idle state, the following conditions exist:

1. All internal timing is reset.
2. The contents of the Sync register, internal to the transmitter, will be all ones.
3. All the bits in the TxCSR may be reset except the Transmitter Done bit which will be set.
4. The TxDBUF will contain all ones.

When the receiver is in an idle state, the following conditions exist:

1. All internal timing is reset.
2. The contents of the Sync register, internal to the receiver, will be all zeros.
3. The following bits in the RxCSR will be cleared:

2-144
DU11

Data Set Change
Receiver Active
Strip Sync
Receiver Done
Receiver Interrupt Enable
Data Set Interrupt Enable
Search Sync

The following bits of the RxCSR may be optionally excluded from the bits cleared by a Master Reset or INIT signal:

Secondary Transmit Data
Request to Send
Data Terminal Ready

If the user decides to connect the option jumper to clear the above bits, then all of these bits will be cleared. The DU11 is shipped with this jumper in.

The contents of the RxBUF will be all ones in the low byte. In the high byte, the Error, Overrun, Frame Error, and Parity Error bits will be cleared.

The contents of the high byte in the Parameter Control Register (PARCSR) will be unaffected by the Master Reset.

Immediately after power-up, these bits will be in an undefined state.

**NOTE:**
This bit is one-shot; that is, it will be asserted for 6 μsec and then return to the zero state.

**Bit 09**
RESERVED

**Bit 10**
MAINTENANCE BIT WINDOW
When in the maintenance mode 01 or 00, this bit can be used to monitor the input to the receiver logic. The stimulus that creates the input could be either the Maintenance Data bit or the serial output of the transmitter, depending on the state of the Break bit.

Program read only.

**Bits 11 & 12**
MAINTENANCE MODE SELECT (BITS 01 & 00)
These bits are used to select anyone of three maintenance modes:

<table>
<thead>
<tr>
<th>BIT SETTING</th>
<th>12</th>
<th>11</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Internal Maintenance Mode</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2. External Maintenance Mode</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3. Internal Maintenance Mode for Systems Testing</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
INTERNAL MAINTENANCE MODE (01)
Internal maintenance mode clocking comes from the Clock bit (bit 13) driven via the program. While using this mode, the following EIA level converters are disabled (this is done so that the majority of the logic can be diagnosed without disconnecting the modem cable):

  Receiver Clock
  Transmitter Clock
  Receiver Data
  Transmitter Data

Modem control flags should be cleared and not used in this mode. All inputs that were driven by the modem will now be simulated by the program setting the appropriate flags. The function of the half-duplex bit in the TXCSR cannot be tested in this mode. The external maintenance mode must be used to test this function.

EXTERNAL MAINTENANCE MODE (10)
When in the external maintenance mode, all lines connected to the data set must be removed at the data set interface. A special connector replaces the connector of the data set. The function of the special connector is to turn around specified signals after level conversion and bring them back to the DU11 as simulated inputs.

The test loop back connector to be used is the H315 connector.

Clocking in this mode is under control of the maintenance clock bit. Refer to clock bit description for its characteristics.

This is the only mode that can be used to check out the function of the Half-Duplex bit.

INTERNAL MAINTENANCE MODE FOR SYSTEMS TESTING (11)
With bits 12 and 11 both set to a one (mode 11), the internal maintenance mode provides an adequate method of clocking the receiver and transmitter. The clocking method should not be synchronous to the program. An RC clock is provided in the interface for this purpose. Mode 11 will be the same as mode 01 with respect to data set control lines. The only difference is that Receiver and Transmitter clocking is derived from an RC clock at 3 kC.

NOTE:
If bits 12 and 11 are zero, normal operating mode is assumed.

These bits are program read/write and are cleared by INIT or Master Reset.
Bit 13  MAINTENANCE CLOCK
This bit is used to simulate the Transmitter and Receiver clock. It is used for diagnostic purposes only. With this bit, the diagnostic has the ability to single step the interface. A 0-to-1 transition of this bit causes the transmitter to transfer a bit from the internal shift register to the output of the transmitter.

A 1-to-0 transition of this bit causes the receiver to transfer the input of the receiver into the internal shift register.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 14  MAINTENANCE DATA
This bit is used only in the maintenance mode by the diagnostic program. In either maintenance mode 01 or 10, this bit can be used to simulate data at the receiver input. When used as a simulated input to the receiver, the Break bit must be set to inhibit additional input from the transmitter. This bit should be cleared if it is not being used as the simulated input. If this bit were inadvertently set in maintenance mode and the Break bit was clear, the receiver input would have two sources of input.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 15  DATA NOT AVAILABLE
This bit is set by the transmitter logic when a character is transmitted from the Sync register. This applies only to synchronous operation and is caused by late or no program response.

The program response to the Transmitter Done bit must be within $1/{\text{Baud}} \times (\text{bits per character}) = \frac{1}{2}$ bits per second. If not, a character from the Sync register will be transmitted.

If the Data Not Available Interrupt Enable bit is set in the TxC SR, it will cause an interrupt to the transmitter interrupt vector.

This bit is program read and is cleared by reading the TxC SR, INIT, and Master Reset.

TRANSMITTER DATA BUFFER REGISTER (TxDBUF)
Address: 16XX46 (Addressable by word or byte to the even address only)
DU11

Bits
00-07 TRANSMITTER DATA BUFFER
This register is loaded by the program with the character to be transmitted. Character length is from 5 to 8 bits. The character is right-hand adjusted, with bit 00 being the least significant bit of any character and bit 07 the most significant bit of an 8-bit character. Any parity bit required is generated by the interface.

Subsequent to a Master Reset or INIT, this register will contain all ones.

Program write.

Bits
08-15 RESERVED

CONTROL LEADS
The modem control leads are provided to interface the DU11 to Bell series 200 synchronous modems or equivalent. These leads allow the DU11 to be used in switched or dedicated, full- or half-duplex configurations.

The DU11 is connected to a Bell model 201 synchronous modem (or equivalent) by a 7.6m (25-foot) cable terminated at the modem end with a 25-pin male connector. Interface signals versus connector pin assignments are given below.

<table>
<thead>
<tr>
<th>PIN</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Signal or Protective Ground</td>
</tr>
<tr>
<td>2</td>
<td>Send Data</td>
</tr>
<tr>
<td>3</td>
<td>Receive Data</td>
</tr>
<tr>
<td>4</td>
<td>Send Request</td>
</tr>
<tr>
<td>5</td>
<td>Clear to Send</td>
</tr>
<tr>
<td>6</td>
<td>Interlock</td>
</tr>
<tr>
<td>7</td>
<td>Signal Ground</td>
</tr>
<tr>
<td>8</td>
<td>Carrier On-Off</td>
</tr>
<tr>
<td>15</td>
<td>Serial Clock Transmit</td>
</tr>
<tr>
<td>17</td>
<td>Serial Clock Receive</td>
</tr>
<tr>
<td>20</td>
<td>Data Terminal Ready</td>
</tr>
<tr>
<td>22</td>
<td>Ring Indicator 1</td>
</tr>
<tr>
<td>24</td>
<td>External Timing</td>
</tr>
</tbody>
</table>

SPECIFICATIONS

Function
Provides an interface between the PDP-11 UNIBUS and a single synchronous bit serial communications channel.

Mechanical
The DU11 consists of one quad (8½” x 10½”) etched circuit card, and a 25-foot connecting cable terminated in a plug appropriate to the data communications equipment to be connected.
Operating Mode
Full- or half-duplex under program control.

Environmental
+10 to +50°C with a relative humidity of 20% to 95% (without condensation).

Power Requirements
+5 V at 2 A
-15 V at 0.15 A
+15 V at 0.05 A

UNIBUS Loads
The DU11 presents one unit load to the PDP-11 UNIBUS.

ORDERING INFORMATION
DU11-DA Full/half duplex synchronous line module set. Double buffered, 5, 6, 7, or 8-bit characters. EIA/CCITT termination suitable for use with Bell series 200 synchronous modems or equivalent. Includes 7.6-m (25-foot) modem cable.

APPLICATIONS
Applications for high-speed synchronous communications interfaces vary widely, and new applications are being developed every day. These applications span all user groupings—commercial, industrial, scientific, and government.

Functionally, these applications may be divided into a few fundamental classes, such as:

- **REMOTE DATA COLLECTION.** Gathering information at a number of remote locations and transmitting it to a central processing point.
- **REMOTE BATCH PROCESSING.** The processing of batch or production jobs at a location remote to where the job is generated and the results are needed.
- **REMOTE CONCENTRATION.** Multiple DU11s connected to a PDP-11 enable it to be used as a synchronous line concentrator or front-end synchronous controller to a larger computer. The concentrator helps reduce line costs by concentrating data from several lines onto one high-speed line.
- **COMPUTER-TO-COMPUTER COMMUNICATIONS.** The DU11 can be used to connect two PDP-11s together or a PDP-11 to another larger processor (e.g., an IBM 360). Intercomputer communication is used in such applications as load sharing, data base sharing, and remote job entry. It permits more effective utilization of the interconnected computers because the slack time in one computer’s schedule can be used to help smooth out the peaks in another’s.
- **ON-LINE TERMINAL PROCESSING.** The DU11 can connect a wide variety of remote terminals to the PDP-11.
SYNCHRONOUS LINE INTERFACE, DUP11

FEATURES
- Transmission speeds up to 19,200 bits per second
- Double-character-buffered receive & transmit
- Full- or half-duplex operation
- Byte-oriented operation (protocols such as DDCMP and BISYNC)
- Bit-oriented operation (protocols such as SDLC, HDLC, ADCCP, and X.25)
- CRC-16 generation and checking for use with DDCMP protocol
- Bit-oriented operation (protocols such as SDLC, HDLC, ADCCP)
- CRC-16 generation and checking for use with DDCMP protocol
- CRC/CCITT generation and checking for use with bit-oriented protocols
- Programmable SYNC character for byte-oriented operation
- Secondary address recognition for bit-oriented operation
- 8-bit character size
- SYNC stripping on receive operations under program control
- Interfaces to Bell 201, 208, and 209 series synchronous modems or equivalents
- Auto answering capability
- Modem control
- Simple, compact single-board design (i.e., SPC slot UNIBUS option)
INTRODUCTION
The DUP11 is a single-line, program-controlled, double-buffered communications device designed to interface the PDP-11 processor to a serial synchronous line. The self-contained unit is capable of handling a wide variety of protocols, including byte-oriented protocols, such as DDCMP and BISYNC and bit-oriented protocols, such as SDLC, HDLC, ADCCP, and X.25.

The DUP11 is ideally suited for interfacing the PDP-11 to medium-speed synchronous lines for remote batch, remote data collection, remote concentration and network applications. Multiple DUP11's on a PDP-11 allow its use in applications requiring several synchronous lines.

The DUP11 provides serial-to-parallel and parallel-to-serial data conversion, voltage level conversion, and modem control for half or full-duplex operation. The Bell Series 200 synchronous modems or equivalent may be used with the DUP11.

Modem control is a standard feature of the DUP11. The necessary signals needed to establish communications with the Bell Series 200 synchronous modems are present in the Receive Status Register (RxCSR). A transition of control lines emanating from the modem directly will not cause a change in the state of the transmitter or receiver logic.

The DUP11 is capable of transmitting data at the maximum speed of 9600 baud (limited by modem and data set interface level converters).

The DUP11 is capable of transmitting data at the maximum speed of 19.2K baud (limited by modem and data set interface level converters).

DESCRIPTION
The DUP11 is a character-buffered, synchronous, serial-line interface capable of two-way simultaneous communications. The DUP11 translates between serial data and parallel data. Output characters are transferred in parallel from the PDP-11 UNIBUS into the DUP11 where they are serially shifted to the communication line. Input characters from the modem are shifted into the DUP11 and made available to the PDP-11 on an interrupt basis.

This allows a full character time in which to service transmitter and receiver interrupts. The clocking necessary to serialize the data is provided by the associated synchronous modem.

The DUP11 contains five registers: two status registers, two data buffer registers, and a Parameter Status Register.

SPECIFICATIONS
Function
The DUP11 provides an interface between the PDP-11 UNIBUS and a single, synchronous, bit-serial communications channel. It is capable of
DUP11

handling a wide variety of protocols, including bit-oriented protocols (such as SDLC, HDLC, ADCCP, and X.25).

Mechanical
The DUP11-DA consists of one hex-size (15\(\frac{3}{4}\) inch x 8\(\frac{3}{8}\) inch) module, a 16 inch flat ribbon cable, and a 25 foot (7.6 meters) connecting cable. It requires one slot in a DD11-B mounting panel or equivalent. Only slots 2 and 3 of the DD11-B can be utilized with this device. Two DUP11-DAs can be mounted in one DD11-B.

Operating Mode
The DUP11 operates in half- or full-duplex mode, under program control.

Environmental
Temperature: +10 degrees C to +40 degrees C.
Relative Humidity: 10% to 90%, non condensing.

Power Requirements
+ 5V @ 3.6A
+15V @ .0
-15V @ .0

The DUP11 presents one unit load to the PDP-11 UNIBUS.

Ordering Information
DUP11-DA Full/half duplex synchronous-line module set. EIA/CCITT termination suitable for use with Bell Series 200 synchronous modems or equivalent. Supplied with 25-foot modem cable.
Prerequisite: DD11-B system unit, (slots 2 or 3 only).

DUP11 OPERATION
The operation of the DUP11 depends on whether it must handle a byte-oriented protocol, such as DDCMP or BISYNC, or a bit-oriented protocol, such as SDLC, HDLC, ADCCP, and X.25. This is determined by bit 15 (DEC MODE) of the Parameter Status Register.

The transmitter operation of the DUP11 performs parallel-to-serial conversion of 8-bit bytes supplied to it from the PDP-11 UNIBUS and optionally calculates and sends CRC-16 block check characters.

After the initialize or device reset pulse, the program must set the DEC MODE bit in the Parameter Status Register (PARCSR) to indicate that a byte-oriented protocol is in use. The program should also specify if CRC calculation is desired and set the CRC INHIBIT bit of the PARCSR register if not desired. For byte-oriented operation, the DUP11 uses the CRC-16 polynomial:

\((X^{16} + X^{15} + X^2 + 1)\)

Protocols such as DDCMP can make efficient use of the DUP11 CRC capability. These protocols are characterized by the fact that all characters within the message are included in the CRC. For other byte-
oriented protocols such as BISYNC, the CRC capability of the DUP11 must usually be inhibited.

Before transmitting, any necessary handshaking with the data set should be completed. Once this has been done, the program can enable the transmitter by setting the SEND bit of the Transmitter Status Register (TxCSR). (Refer to Pg. 4-272.)

The program begins transmission by loading the desired SYNC character into the Transmitter Data Buffer Register (TxDBUF) and setting the TSOM bit. All transmitted SYNC characters must be loaded into the TxDBUF.

When TxDONE is set after the last SYNC character has been loaded, the program should load the first data character into the TxDBUF and clear the TSOM bit. This character and all subsequent data characters will be included in the CRC calculation.

The accumulated CRC check characters are transmitted by setting the TEOM bit. When the data character currently being transmitted is complete, the CRC check characters will be sent (unless inhibited). The TxDONE bit of the Transmitter Status Register (TxCSR) will be set at the start of transmission of the CRC check characters if the program has not cleared the SEND bit. The TxDONE bit can be cleared by again setting TEOM, or additional data characters can be sent by loading the first one into TxDBUF and clearing TEOM. SYNC characters can be idled by loading a SYNC character into TxDBUF, clearing TEOM and setting TSOM.

If the program wishes to idle the serial line to a mark, it should clear SEND immediately after setting the TEOM bit. In this case the TxDONE bit will not set until the entire CRC has been sent and the line has gone to the mark state for 1/2 bit time.

The transmitter CRC register is initialized to zeros by the initialize pulse and by device reset. It is also held in the zero state by logic synchronized to the TSOM bit. It will be held in this state until the last character associated with TSOM has been transmitted. When the CRC has been sent in response to TEOM, the CRC register will be zero.

The DUP11 does not automatically idle SYNC characters if the transmitter data buffer is not serviced in time. Instead, the line will be held in the mark state. The DUP11 signals the error condition by setting the TxDAT LATE bit in the TxCSR. The TxDAT LATE bit is cleared by setting TSOM. While TSOM is true, TxDAT LATE will not set and the program can idle multiple SYNC characters without program intervention by disabling interrupts at this time. The DUP11 is double-buffered and the program has at least one character time to respond to the setting of TxDONE. The time available can be calculated according to the formula:

\[
7.5 \text{ (1/bits per second) seconds}
\]
Byte-Oriented Operation—Receiver

The receiver operation of the DUP11 performs serial-to-parallel conversion of 8-bit bytes and optionally calculates and checks the CRC-16 block check characters.

After the initialize or device reset pulse, the program must set the DEC MODE bit of the PARCSR and set the CRC INHIBIT bit of the PARCSR if it does not wish the DUP11 to perform CRC verification. These bits affect both the transmitter and receiver. In addition, the program must load the desired SYNC character into the PARCSR. This SYNC character affects only the DUP11 receiver.

Before enabling the receiver, any necessary handshaking with the data set should be completed. Once this has been done, the program can enable the receiver by setting the RCVEN bit in the Receiver Status Register (RxCSR). Setting RCVEN causes the receiver to search the data stream for two consecutive SYNC characters. When two successive SYNCs have been recognized, the receiver is considered synchronized and subsequent information will be assembled as 8-bit characters.

Whenever a character is assembled, it will be transferred into the Receiver Data Buffer Register (RxDBUF). If the character is not a SYNC character, or if a non-SYNC character has been assembled subsequent to receiver resynchronization, then RxDONE will be set. If the character is a leading SYNC character, then RxDONE will be set unless the STRIP SYNC bit of the RxCSR is set. The program can bypass leading SYNC characters by setting STRIP SYNC.

Until RxDONE sets for the first time subsequent to receiver re-synchronization the receiver CRC register will be zero and the RxACT (receiver active) bit of the RxCSR will be clear. Upon assembling the first character to be presented to the program, RxACT and RxDONE will be set together. This character and all subsequent characters will be included in the receiver CRC calculation.

The RCRC ERROR + ZERO bit of the RxDBUF will be set whenever the receiver CRC calculation for characters up to and including the character in the RxDBUF has resulted in a zero result and the CRC INHIBIT bit in the PARCSR is clear. The program can check for a valid CRC by examining this bit when two characters, in addition to the data characters, have been assembled. The program should ignore this bit at other times. It is entirely possible that this bit may set during the middle of a message should the CRC register happen to assume a zero value at some point.

The program can shut down the receiver by clearing RCVEN. This will clear RxDONE, RxACT, the receiver data buffer, and the receiver CRC register and will disable the receiver. The program can force the DUP11 receiver to resynchronize by clearing RCVEN and then setting it.
The program must respond to the RxDONE bit by reading the RxBDUF within one character time. If this is not done, the OVRUN ERR (overrun error) bit in the RxBDUF will set and the contents of the data buffer will contain the most recently received character. Any previous character(s) will be lost.

**Bit-Oriented Protocol Message Formats**

The DUP11 can operate with bit-oriented protocols such as IBM's SDLC protocol, ISO's HDLC protocol, and ANSI's ADCCP protocol. All these protocols use a particular 8-bit sequence, 01111110, called a FLAG, to mark the beginning and end of variable length messages, called frames, and thereby establish synchronization. Information between FLAGS is dependent on the protocol used, but typically consists of address and control information, user data, and block check characters (Fig. 1). These protocols place no restriction on the information between FLAGS.

<table>
<thead>
<tr>
<th>FLAG</th>
<th>ADDRESS</th>
<th>CONTROL</th>
<th>INFORMATION</th>
<th>CRC</th>
<th>FLAG</th>
</tr>
</thead>
</table>

**Figure 1. Frame Format**

To ensure that a particular data sequence is never mistaken for a FLAG, a technique known as bit-stuffing is used on the information between FLAGS. Whenever five consecutive one bits have been sent, the transmitter inserts a zero bit into the data stream. When the five one bits followed by the zero bit are recognized by the receiver, the receiver removes the inserted zero bit. By this technique, any user-data pattern can be sent and received with no danger of its being mistaken for a FLAG character (Fig. 2). In principle, this technique can be used with frames any number of bits long. However, the DUP11 is restricted to operation with frames which are some number of 8-bit characters in length.

```
..0111110011111101100... user data bits
..011111000111110101100. data on communication line
  stuffed bit      stuffed bit
..011111 0011111 101100... decoded user data
  stuffed bit removed
```

**Figure 2. Example of Bit Stuffing**

When one frame has been completed, another can follow immediately, sharing a single FLAG character. Alternatively, the communication line can be held active by sending multiple FLAG characters. If it is desired to shut down the line, the line can be idled to the mark state.
Sometimes it is desired to abort a frame being transmitted. This can be done by sending an incorrectly formed frame, i.e., one containing seven or more consecutive one bits. The DUP11 transmitter can send a sequence of eight consecutive one bits, called an ABORT to indicate this condition. Following an ABORT, one or more FLAGs can be sent, or the line can be idled to the mark state. There is no danger that user information will be mistaken for an ABORT because of bit-stuffing.

For multipoint operation, secondary stations are distinguished by their addresses. A secondary station must accept and process only frames addressed to it. The DUP11 receiver contains logic to hold a secondary address and compare this address with the first character of a frame. For operation as a secondary station, the DUP11 will skip over all characters in frames intended for other stations, eliminating unnecessary program overhead. This feature can be disabled for operation as a primary station or with protocols which do not use the first character of a frame as an address.

The DUP11 does not process the control or information fields of a frame. These are treated as 8-bit characters and are passed to the program.

Most bit-oriented protocols use a 16-bit CRC block check, calculated according to the CRC/CCITT polynomial:

\[(X^{16} + X^{12} + X^5 + 1)\]

The CRC field is the last field of the frame.

The transmitter uses a 16-bit register to calculate CRC. The transmitter initializes the register to all ones prior to the start of the frame. The transmitter calculates the CRC on all data bits (not stuffed bits) beginning immediately following the FLAG and ending immediately prior to the block check field. The transmitted CRC is the complement of the register contents at the end of the calculation.

The receiver performs a similar calculation, using a separate 16-bit register. The receiver initializes this register to all ones and calculates the CRC on all data bits between the FLAGs (including the transmitted CRC). The receiver then checks for a special value that compensates for transmitting the complement of the calculated CRC. If the special value is not seen, an error is indicated.

The DUP11 CRC logic can be inhibited for protocols that do not use this method of generating and checking a block check. If the CRC logic is inhibited, any block checks will be treated as data by the DUP11 and are the responsibility of the program.

Bit-Oriented Operation—Transmitter
The transmitter section of the DUP11 generates FLAG and ABORT sequences, performs parallel-to-serial conversion of 8-bit bytes supplied to it from the PDP-11 UNIBUS, and optionally generates and sends the CRC/CCITT block check characters. Whenever the data stream between two FLAGs contains five consecutive one bits, the transmitter logic auto-
matically inserts a zero bit to distinguish data and block check characters from FLAG and ABORT sequences.

After the initialize or device reset pulse, the program should clear the DEC MODE bit in the PARCSR. The program should also specify if CRC calculation is desired and set or clear the CRC INHIBIT bit of the PARCSR as desired. The DUP11 calculates and sends the block check characters as described above. For protocols calculating the block check differently, the CRC capability of the DUP11 should be inhibited and the program should generate the required block check characters.

Before transmitting, any necessary handshaking with the data set should be completed. Once this has been done, the program can enable the transmitter by setting the SEND bit of the TxCSR. (Refer to Pg. 4-272.)

The program begins transmission by setting the TSOM bit in the TxDBUF. This initial access momentarily clears the TxDONE bit, which was initially set by the initialize pulse or reset. The transmitter will remain inactive for a period equal to two bit times and then the transmitter will become active. The TxACT (transmit active) and TxDONE bits will be set and a FLAG sequence will begin on the serial line.

Some devices that communicate with the DUP11 require that sixteen 0 bits precede the FLAG character beginning the first frame sent after enabling the transmitter. To accommodate these devices, the program should set TEOM together with TSOM immediately after setting the SEND bit. TxDONE and TxACT will set when the 0 bit sequence begins. When TxDONE sets for the first time the program should respond by clearing TEOM. This will clear TxDONE. TxDONE will set again when the sixteen 0-bits have been sent and a FLAG character has begun. Note that TEOM and TSOM can be used this way only immediately after the transmitter has been enabled.

If it is desired to send an additional FLAG, the program can clear TxDONE by accessing the TxDBUF and leaving TSOM set. TxDONE will set when the additional FLAG has begun. The program can send any desired number of FLAGS by counting.

When TxDONE has set as the last desired FLAG has begun, the program should clear TSOM and write the first character of the frame into the TxDBUF. Note that the DUP11 transmitter will not automatically send an address character, even in secondary address mode.

Writing a character into the TxDBUF will clear TxDONE. TxDONE will set again when the current character or sequence has been sent on the serial line and the new character has begun. The TxDBUF should be accessed only in response to TxDONE.

The program should write successive characters of the frame into the TxDBUF in response to TxDONE. This must be done within one character time or the TxDAT LATE bit will set in the TxCSR indicating an error condition. The time available may be calculated according to the following formula:
\[
(1/\text{bits per second}) \ast (7.5 + n) \text{ seconds}
\]
where \( n \) is the number of bits stuffed (\( n = 0, 1, \) or 2)

Should TxDAT LATE set, the DUP11 transmitter will transmit an ABORT sequence on the serial line. Additional ABORTs will be sent until the program sets TSOM to begin a new frame or clears SEND. Clearing SEND must remain cleared until TxACTION is no longer set.

When the program has loaded the final data character and TxDONE sets to indicate that this character has begun to be sent on the serial line, the program should set TEOM to inform the DUP11 transmitter that the message is complete. Subsequent events depend on whether CRC calculation is inhibited and whether the program wishes to send an additional frame following the terminating FLAG, or wishes to idle FLAGs, or marks.

If the program wishes to shut down transmission, it should clear SEND as soon as it has set TEOM. In this case, the DUP11 transmitter will complete the current data character, send the two block check characters (unless CRC INHIBIT is set in PARCSR) and send the terminating FLAG. The line will then go to the mark hold state. Setting TEOM clears TxDONE. When the line has been in the mark hold state for one-half bit time, TxACTION will clear and TxDONE will set, indicating that the frame has been completely transmitted.

If the program wishes to transmit another frame that immediately follows the current frame and shares a single FLAG character, it should wait for TxDONE to set indicating that the FLAG character has begun transmission. The program should then clear TEOM and load the first character of the new message into the TxBUF. The FLAG will complete and then the new message will begin.

If the program wishes to idle FLAGs between frames, it should leave TEOM set in response to TxDONE setting. TxDONE will not be cleared if the program does not touch the TxBUF, so interrupts during the waiting period are avoided. When the program wants to begin a new frame, it should set TSOM. This clears TxDONE, reinitializes the CRC register and initiates the transmission of one additional FLAG. When this FLAG begins, TxDONE will set and the program should load the first data character of the new frame.

The program can count FLAGs by setting TEOM in response to TxDONE. This will clear TxDONE. TxDONE will set again when a FLAG has begun. The program can continue to set TEOM and count or clear TEOM and set TSOM to begin a new frame.
In some cases it may be desirable to send one or more ABORT sequences following a terminating FLAG. The program should set the TxABORT bit and clear TEOM when TxDONE sets at the time the FLAG has begun. This occurs the first time TxDONE sets after the program has set TEOM. The program should set TEOM to clear TxDONE. TxDONE will set again when the FLAG begins. At this point, the program should clear TEOM and set TxABORT. Setting TxABORT will clear TxDONE. TxDONE will set when the ABORT begins.

If the program wishes to ABORT a frame it is in the process of sending, it should set TxABORT in response to TxDONE. An ABORT will be sent on the serial line as soon as the current character is completed.

The program can count ABORTs by setting TxABORT in response to TxDONE. Setting TxABORT will clear TxDONE, but TxDONE will set again when the requested ABORT begins. To shut the line down after the last desired ABORT has begun, the program should set TxABORT a final time, clear SEND, and wait for TxDONE to set indicating the ABORT has completed and the line is idle. To start a new message after the last desired ABORT has begun, the program should clear TxABORT and set TSOM. When the ABORT completes, a FLAG will begin and TxDONE will set. The program should clear TSOM and load the first data character.

Bit-Oriented Operation—Receiver
The receiver section of the DUP11 detects FLAG and ABORT sequences, performs serial-to-parallel conversion of 8-bit bytes of data, and optionally calculates and checks the CRC/CCITT block check characters. Whenever the data stream between two FLAGs contains five consecutive one bits followed by a zero bit, the receiver section automatically deletes the zero bit from the data stream being assembled into characters and checked in the CRC calculation. This restores the original transmitted data stream.

After the initialize or device reset pulse, the program must clear the DEC MODE bit of the PARCSR and set or clear the CRC INHIBIT bit of the PARCSR. These bits affect both the transmitter and receiver. In addition, the program can set the secondary mode select bit of the PARCSR if the DUP11 is operating as a secondary station with a protocol which uses the first data character as a secondary address. In this case, the program must load the desired secondary address into the PARCSR.

Before enabling the receiver, any necessary handshaking with the data set should be completed. Once this is done, the program can enable the receiver by setting the RCVEN bit in the RxCSR. The receiver will begin to search for a FLAG sequence.

Multiple FLAGS at the beginning of a frame are simply ignored. A frame begins following the last initial FLAG.
If the DUP11 is not in secondary address mode when the first character of a frame has been assembled, the receiver will load the character into the RxDBUF, set the RSOM (receiver start of message) bit in the RxDBUF, and set the RxACT (receiver active) and RxDONE bits in the RxCSR. The program should read the RxDBUF in response to the setting of RxDONE. This will clear RxDONE. (Reading the RxDBUF always clears RxDONE.) RSOM will clear when the next data character has been assembled or if a FLAG or ABORT is received.

If the DUP11 is in secondary address mode, the first character assembled following the last FLAG is compared to the secondary station address register. If it does not match, the initial search for a FLAG begins anew. If it matches, the RxACT bit is set in the RxCSR and the RSOM bit is set in the RxDBUF to indicate the start of a frame. However, the received address character will not be presented to the program. When the subsequent character has been assembled, this character will be loaded into the RxDBUF. RSOM will remain set. RxDONE will be set. The program should read the RxDBUF. RSOM will clear when a third data character has been assembled or if the FLAG or ABORT is received.

Subsequent characters will be loaded into the RxDBUF and presented to the program by setting RxDONE. The program should read the RxDBUF and assemble the incoming frame. If the program does not read the RxDBUF by the time the next character has been assembled, the overrun bit in the RxDBUF will set indicating an error condition. The time available can be calculated by the formula:

\[
\frac{1}{\text{bits per second}} \times (8 + n) \text{ seconds}
\]

where \(n\) is the number of stuffed bits \((n = 0, 1, \text{ or } 2)\)

The DUP11 receiver will recognize the end of frame when it sees a terminating FLAG. The RxACT bit will be cleared and the REOM bit will be set in the RxDBUF. The RxDONE bit in the RxCSR will be set. If CRC INHIBIT is not set and the completed CRC calculation indicates an error, then the RCRC ERROR + ZERO bit will be set in the RxDBUF to inform the program of the error.

When the program reads the RxDBUF and sees REOM set, it should check the state of RCRC ERROR + ZERO if the DUP11 is doing CRC calculation. It must ignore the data buffer. The data buffer contains invalid information when REOM is set.

The DUP11 receiver presents characters as they are assembled. Consequently, even if CRC INHIBIT is not set, the two block check characters will be presented to the program.
If the transmitted data is not a multiple of 8 bits long, a FLAG will be detected in the middle of assembling a character. The program will be presented 8 bits consisting of the left-over data bits and bits derived from the beginning of the FLAG. When the FLAG is recognized, REOM and RxDONE will set as described above. RCRC ERROR + ZERO will set if an error was detected and CRC INHIBIT is not set. The FLAG may be recognized in much less than a character time following the presentation of the above 8 bits. If it occurs before the program has had time to read the RxDBUF, the RxDAT LATE bit will set, indicating an error. The DUP11 is designed to handle frames that are a multiple of 8 bits long, but an error on the serial line might cause the receiver to incorrectly decode stuffed bits creating a frame of incorrect length. The CRC calculation is always done on the actual bits between FLAG characters, regardless of frame length, so any error should be detected.

When the RxDBUF is read, RxDONE will clear and the DUP11 receiver will be ready for another frame. This can begin immediately following a single FLAG or it can follow multiple FLAGS as described above.

The DUP11 receiver will recognize seven consecutive one bits as an ABORT sequence when they appear in the middle of a frame, i.e., any time RCVEN and RxACT are both set. Receiving an ABORT sequence is equivalent to resetting the receiver except that RCVEN is not cleared, the RABORT (received abort) bit in the RxDBUF is set, and the RxDONE bit in the RxCSR is set. Reading the RxDBUF will clear the RABORT bit. When the program sees that RABORT was set, it should discard the partially assembled frame.

When an ABORT has been received, the DUP11 receiver reverts to searching for a synchronizing FLAG.

**Half-Duplex Operation**

The program may specify half-duplex operation by setting the HALF DUPLEX bit in the TxCSR.

In this mode of operation, the receiver will be completely disabled while the SEND bit is set in the TxCSR. All other characteristics of the interface are maintained. This action is only required for half-duplex modems which provide local-copy.

**REGISTERS**

**RECEIVER STATUS REGISTER (RxCSR)—ADDRESS: 16XXX0.**

Addressable by word or byte.

2-161
Bits     Description
00      Data Set Change B
With normal jumper configuration, this bit will be asserted when
any of the following transitions occur on the respective data set
control lines:
—any transition on the Carrier line
—any transition on the Data Set Ready line
—any transition on the Secondary Received Data line
Two optional jumper modifications can be made in the field with
respect to this bit:
1. Removing the data set change jumper will inhibit the setting
   of this bit.
2. This bit will be inhibited and the signal transitions cited above
   will be combined with the ones that always assert Data Set
   Change A (refer to bit 15).
Program read only. Cleared by INIT, Device Reset or by reading
the RxCSR.
01      Data Terminal Ready
When set, this bit causes the Data Terminal Ready lead to be
asserted to the modem.
Program read/write. Optionally cleared by INIT or Device Reset.
02      Request to Send
When set, this bit will cause the Request-to-Send lead to be
asserted to the modem.
Program read/write. Optionally cleared by INIT or Device Reset.
03      Secondary Transmit Data
This bit is connected to the Secondary Transmit line of the
modem. With certain modems, supervisory data can be trans-
mitted over this line at a reduced rate.
Program read/write. Optionally cleared by INIT or Device Reset.

04 Receiver Enable (RCVEN)
This bit controls the operation of the receiver logic. When initially asserted, the receiver is enabled to search for synchronization, regardless of the DUP11's operating mode.

Once synchronization has been achieved, the reception of data and the timing are controlled by this bit.

Clearing this bit at any time will cause all receiver timing and control functions to be reset asynchronously to the modem clock or the data stream currently being received.

The RxDONE bit will be cleared by the OFF transition of this bit.

Program read/write. Cleared by INIT or Device Reset.

05 Data Set Interrupt Enable
When set, this bit allows interrupt requests to be made to the receiver vector, if the Data Set Change A bit is asserted. Program read/write. Cleared by INIT or Device Reset.

06 Receiver interrupt Enable
When set, this bit allows interrupt requests to be made to the receiver vector, if the RxDONE bit is set.

Program read/write. Cleared by INIT or Device Reset.

07 Receiver Done (RxDONE)
This bit is set by the device when the RxACT bit is asserted and a character is transferred from the internal receiver shift register to the RxDBUF (receiver data buffer).

In byte-oriented mode, this bit will also be asserted whenever SYNC characters are received immediately subsequent to the actual synchronizing SYNC characters, unless the STRIP SYNC bit is set.

In bit-oriented operation, this bit will also be asserted if the RxACT bit is set when an ABORT sequence is received or when the REOM bit is set in the RxDBUF.

Program read only. Cleared by reading the RxDBUF, an off transition of RCVEN, INIT, and Device Reset.

An interrupt request will be generated if Receiver Interrupt Enable is set when this bit is asserted.

08 STRIP SYNC
This bit is used only with byte-oriented protocols. Once the receiver has achieved synchronization, any characters received that match the contents of the low byte of the PARCSR will not be presented to the program if they are contiguous to the initial SYNC characters (i.e., RxDONE will not be set) if this bit is set.

As a result, any SYNC characters contiguous to the SYNC characters that caused the actual synchronization are stripped off. The function of this bit is automatically disabled while RXACT is set.

2-163
NOTE
This bit must be cleared when operating with bit-oriented protocols.

Program read/write. Cleared by INIT or Device Reset.

09 Data Set Ready
This bit is a direct reflection of the Data Set Ready (or interlock) lead emanating from the modem. This line, when asserted, indicates the modem is powered up and is not in the test, talk, or dial mode. Any transition of this bit will cause the Data Set Change B bit to be asserted unless the data set change jumper modification has been made (refer to bit 15 of RxCSR).

Program read only.

10 Secondary Received Data
This bit reflects the state of the Secondary Received Data line of the modem. Any transition on this line will cause the Data Set Change B bit to assert unless the data set change jumper modification has been made (refer to bit 15 of this register).

With certain modems, supervisory data can be received over this line at a reduced rate. It can also be used as a control lead.

Program read only.

11 Receiver Active (RxACT)
In byte-oriented operation, this bit will set when the first character has been assembled subsequent to synchronizing on two SYNC characters if Strip SYNC is cleared. If Strip SYNC is set, this bit is asserted after receiving the first non-SYNC character. This bit controls whether incoming data is included in the receiver CRC calculation.

In bit-oriented operation, as a primary station, this bit will set when the first data character of a frame has been assembled. In bit-oriented operation, as a secondary station, this bit will set when the first character of a frame has been assembled and that character matches the contents of the Secondary Station Address Register. This bit will clear when a terminating FLAG is recognized or if the frame is aborted by receipt of seven consecutive one bits. This bit controls the operation of the receiver logic.

Program read, cleared by INIT, Device Reset, and clearing RCVEN.

12 Carrier.
This bit is a direct reflection of the modem carrier. Any change in the state of this line will cause Data Set Change B bit to be asserted, unless the Data Set Change jumper modification has been made. (Refer to bit 15 of this register).

Program read only.

13 Clear to Send.
This bit reflects the state of the Clear-to-Send line of the modem.
Any transition of this line causes the Data Set Change A bit to set.
Program read only.

14 Ring Indicator
This bit reflects the state of the modem Ring line. Any positive transition of this line greater than 10 msec causes the Data Set Change A bit to set.
Program read only.

15 Data Set Change A
This bit is set by a transition on any of the following control lines:
—any positive transition on the Ring line greater than 10 msec.
—any transition on the Clear-to-Send line
An optional field installation change (consists of a jumper modification, supported by diagnostics) will allow this bit to be set by any of the following transitions:
—any transition on the Carrier line
—any transition on the Data Set Ready line
—any transition on the Secondary Received Data line.
Normally these transactions cause bit 0 (Data Set Change B) to be set in this register. If the jumper modification is made, bit 0 will be disabled.
If bit 05 of this register is set, the assertion of this bit will cause an interrupt to the receiver vector.
Program read only. Cleared by INIT, Device Reset, or when the RxCSR is read.

RECEIVER DATA BUFFER REGISTER (Rxdbuf)—ADDRESS: 16XXX2.
Read only—addressable by word.
This register should be read only in response to RxDONE.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-07</td>
<td>Receiver Data Buffer</td>
</tr>
<tr>
<td></td>
<td>This register contains 8-bit data received from the modem. Bit</td>
</tr>
</tbody>
</table>
DUP11

00 is the least significant bit and bit 07 the most significant bit. When the REOM bit is set, the data in this register is not valid.

Program read, cleared by INIT, Device Reset, RABORT or clearing RCVEN.

08 Start of Received Message (RSOM)
This bit is used only in bit-oriented mode. When in the primary mode, this bit is set when the first data character is received. In secondary mode, this bit is set when the character following an address character is received, providing that the address character matched the contents of the secondary station address register. The next transfer from the receiver shift register into the RxDBUF will clear this bit.

Program read. Cleared by INIT, Device Reset, and clearing RCVEN.

09 End of Received Message (REOM)
This bit is used only in bit-oriented operation. This bit will set when a terminating FLAG is recognized. The next transfer from the receiver shift register into the RxDBUF will clear this bit.

Program Read, cleared by INIT, Device Reset, and RCVEN.

10 Received ABORT (RABORT)
This bit will set when an ABORT sequence (seven consecutive one bits) is detected while the receiver is active in bit-oriented operation. When this occurs, all the DUP11 receiver timing, internal control, and registers will be reset.

Setting this bit will cause the RxDONE and Receiver Error bits to be set.

Cleared by INIT, Device Reset, clearing RCVEN, and reading the RxDBUF.

11 Reserved

12 RCRC ERROR + ZERO
This bit will remain zero if CRC INHIBIT is set in PARCSR.

In byte-oriented operation, this bit will be set whenever the DUP11 receiver internal CRC register was zero at the completion of the character in the RxDBUF.

In bit-oriented operation, this bit will be set if the receiver logic detects an invalid block check. This bit will be set when the terminating FLAG is detected, i.e., the same time REOM is set.

When this bit has been set, it will remain set until the next transfer is made into the RxDBUF from the receiver internal shift register. This will normally be for at least one character time.

Program read only. Cleared by INIT, Device Reset, and clearing RCVEN.

13 Reserved.

14 Overrun

When the receiver logic detects an overrun condition, this bit is
DUP11

set. An overrun is caused primarily by poor program response time. Assertion of this bit will cause the Error bit to assert. Once the Receiver Done (RxDONE) bit is set, the program must respond within one character time; if not, Overrun will occur. This condition indicates the loss of at least one character.

This bit will be asserted for a minimum of one character time and will clear within one character time after the overrun condition has been relieved by resetting the RxDBUF.

Program read only. Cleared by INIT, Device Reset and clearing RCVEN.

15 Error

This bit will be set in byte-oriented operation while bits 14 or 12 of this register are set. This bit will be set in bit-oriented operation while bits 14, 12, or 10 of this register are set (logical OR).

Program read only.

PARAMETER STATUS REGISTER (PARCSR)—ADDRESS: 16XXX2.

Write only—addressable by byte or word.

This register should be accessed only when both the transmitter and receiver are in idle state.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-07</td>
<td>Secondary Station Address Register or Receiver Sync Register. Used by the receiver logic only. When the DEC MODE bit is set (byte-oriented protocols) this register contains the SYNC character. Bit 00 is the least significant bit and 07 is the most significant bit. When operating in the secondary mode of bit-oriented protocols, this register contains the desired secondary station address. Program write. Cleared by INIT, or Device Reset.</td>
</tr>
<tr>
<td>08</td>
<td>Reserved.</td>
</tr>
<tr>
<td>09</td>
<td>CRC INHIBIT. Setting this bit inhibits transmitting the CRC check character and inhibits checking the received CRC check character.</td>
</tr>
<tr>
<td>10-11</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
DUP11

12 Secondary Mode Select.
This bit is used with bit-oriented protocols only and affects the DUP11 receiver only. When this bit is cleared and DEC MODE is cleared, the DUP11 receiver will operate as a primary station and all data subsequent to the last received FLAG character will be presented to the program, until the terminating FLAG is detected.

When this bit is set and DEC MODE is cleared, secondary station operation is in effect—only messages that are prefixed with the correct secondary station address will be presented to the program. Note: This bit must be cleared when operating with byte-oriented protocols.

Program write. Cleared by INIT or Device Reset.

13-14 Reserved.

15 DEC MODE
When this bit is asserted, the DUP11 will operate in a manner compatible with the byte-oriented protocols (such as DDCMP and BISYNC). If this bit is clear, the device will operate with bit-oriented protocols (such as SDLC, HDLC, or ADCCP).

Program write. Cleared by INIT or Device Reset.

TRANSMITTER STATUS REGISTER (TxCSR)—ADDRESS: 16XXX4.
Addressable by word or byte.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-02</td>
<td>Reserved</td>
</tr>
<tr>
<td>03</td>
<td>Half-Duplex/Full-Duplex</td>
</tr>
<tr>
<td></td>
<td>When this bit is set, the receiver will be disabled if the SEND bit in the TxCSR is set.</td>
</tr>
<tr>
<td></td>
<td>Program read/write. Cleared by INIT or Device Reset.</td>
</tr>
<tr>
<td>04</td>
<td>SEND</td>
</tr>
</tbody>
</table>
| | When set, this bit enables the transmitter logic. Once enabled,
it will start the transmission of a message when the TSOM bit is detected in the TxDBUF.

Clearing SEND when TEOM is clear will cause the line to go to the mark hold following completion of the current character being sent. Clearing SEND when TEOM is set will cause the line to go to the mark hold state when the message being sent is complete (i.e., following the final characters, block check and flags, as required). NOTE: Once SEND has been cleared it should not be set again until TxACT clears. Program read/write. Cleared by INIT or Device Reset.

05 Reserved

06 Transmitter Interrupt Enable

When set, this bit will allow a program interrupt request to be generated by the TxDONE bit.

Program read/write. Cleared by INIT or Device Reset.

07 Transmitter Done (TxDONE)

This bit is set when the Transmitter Data Buffer is available for a new character. This occurs either as a result of an INIT, Device Reset, or when a character is transferred from the TxDBUF into the transmit shift register. If the transmitter is entering the idle state, (i.e., SEND being cleared during the current message), the OFF transition of the TxACT bit will cause TxDONE to set, not the completion of the current character. The TxDONE bit will also set whenever a SYNC, FLAG, or ABORT character has completed transmission, providing the SEND bit is asserted.

Unless a SYNC, FLAG, or ABORT sequence is being transmitted, the program must respond to the assertion of this bit within the previously cited time frame in order to avoid Data Overrun errors.

If the Transmitter Interrupt Enable is asserted, the setting of this bit will create an interrupt request.

Program Read; cleared by writing the TxDBUF; set by INIT or Device Reset.

08 Device Reset

When this bit is set, all components of the device are initialized, unless the optional clear jumper is removed. In this case, the modem control signals from the device are not affected. Note that initializing the device sets TxDONE.

This bit is a 2μsec one-shot and will self-clear.

INIT and Device Reset perform identical functions with respect to this device. Program write.

Do not address the DUP11 while this bit is set.

09 Transmitter Active (TxACT)

This bit indicates that the serial line is in use. It is set when the first SYNC or FLAG begins to be sent in response to the
program enabling the transmitter and setting TSOM. It is cleared one bit time after the serial line has reentered the mark hold state as a result of the program disabling the transmitter.

Program read. Cleared by INIT or Device Reset.

10 Maintenance Input Data

This bit is used in internal maintenance mode as the receiver serial input while SEND is clear. When this bit is set and the maintenance clock bit makes a 0-to-1 transition, a logical one bit will be transferred into the receiver shift register.

Program read/write. Cleared by INIT or Device Reset.

11-12 Maintenance Mode Select A and B

These two bits are used to select the maintenance mode. The program must leave these bits clear for normal operation.

Bit Setting

<table>
<thead>
<tr>
<th>Select B (bit 12)</th>
<th>Select A (bit 11)</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Normal operation</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>System test mode</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>External maintenance mode</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Internal maintenance mode</td>
</tr>
</tbody>
</table>

The external maintenance mode provides a means of checking all the interface components, including level converters and cables. In this mode a special turn-around connector (H325) must be attached in place of the modem at the end of the cable.

The internal maintenance mode provides a means of checking most of the interface without disconnecting the modem. The level converters and cables are not checked. The diagnostic program simulates the data set clocking using the maintenance clock bit. It monitors the transmitted data using the Maintenance Transmit Data Out bit. It can supply input to the receiver using the Maintenance Input Data bit or can cause the receiver to be stimulated by the output of the transmitter.

The system test mode provides a means of exercising most of the interface together with other devices on the PDP-11 UNIBUS without disconnecting the modem. The level converters and cables are not diagnosed. Transmitted data is internally looped to received data. Data set clocking is simulated by a free-running clock at 5KC plus or minus 20%.

Program read/write. Cleared by INIT or Device Reset.

13 Maintenance Clock

This bit is used to single step the transmitter and receiver clock for diagnostic purposes. A 0-to-1 transition of this bit causes the transmitter to transfer one bit of information to the serial line.

A 1-to-0 transition of the bit causes the receiver to shift the
contents of the receiver shift register and sample the serial output line.
This bit must be cleared for normal user operation.
Program read/write. Cleared by INIT or Device Reset.

14  Maintenance Transmit Data Out
This bit is enabled only in internal maintenance mode and provides a monitoring point for serial output data from the transmitter.
Program read. Cleared by INIT or Device Reset.

15  Transmitter Data Late Error (TxDATA LATE)
This bit is set by the DUP11 transmitter logic when the program has failed to respond to the TxDONE bit in time.
In byte-oriented operation when this bit is set, the serial line will be held in the mark state until TSOM is set and a new message is started.
In bit-oriented operations when this bit is set, the transmitter will idle ABORT characters until either TSOM is set to start a new message or the SEND bit is cleared.
Program read only. Cleared by INIT, Device Reset, or by setting the TSOM bit.

TRANSMITTER DATA BUFFER (TxDBUF)—ADDRESS: 16XXX6.
Addressable by word or byte.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-07</td>
<td>Transmitter Data Buffer (TxDBUF)</td>
</tr>
<tr>
<td></td>
<td>The program loads this register with the information to be transmitted, which is always treated as an 8-bit character.</td>
</tr>
<tr>
<td></td>
<td>For byte-oriented operation, the program must load this register with the SYNC character whenever it is desired to transmit SYNC characters.</td>
</tr>
<tr>
<td></td>
<td>Bit 07 is the most significant bit and bit 00 is the least significant bit.</td>
</tr>
<tr>
<td></td>
<td>Program read/write. Cleared by INIT or Device Reset.</td>
</tr>
</tbody>
</table>
Transmit Start of Message (TSOM)
The program sets this bit to initiate transmission following the enabling of the transmitter. The program can also set this bit between messages to transmit SYNC characters or FLAGS.
In byte-oriented operation the program sets this bit to send SYNC characters. (The Transmitter Data Buffer must contain the desired SYNC character.) The transmitter CRC calculation is initialized. The SYNC characters are not included in the CRC calculation.
In bit-oriented operation the program sets this bit to send FLAG characters that precede a frame. The CRC calculation is initialized.
While this bit is set, Transmitter Data Late errors are inhibited.
Program read/write. Cleared by INIT or Device Reset.

Transmit End of Message (TEOM)
This bit is set by the PDP-11 program to indicate that all data characters of a message have been previously loaded into the TxDBUF and the message should be completed. The transmitter completes the character currently being sent, and sends the block check character unless CRC INHIBIT is set.
In bit-oriented operation, the transmitter then sends FLAG characters while this bit remains set. In bit-oriented operation, Data Late errors are inhibited while this bit is set to permit the program to idle FLAG characters.
In bit-oriented operation, this bit is used together with TSOM immediately following the enabling of the transmitter when a 16 bit 0 sequence must precede the beginning FLAG.
Program read/write. Cleared by INIT or Device Reset.

Transmit ABORT (TxABORT)
This bit is used only in bit-oriented operations. Assuming the transmitter is active, setting this bit will cause an ABORT to be sent when the current character or sequence completes.
Leaving this bit set will cause multiple ABORTs to be sent. While this bit is set, Transmitter Data Late errors are inhibited.
Program read/write. Cleared by INIT or Device Reset.

Maintenance Timer
This bit is enabled only in the external or systems test maintenance modes and is used to provide a known timing reference for diagnostic programming.
Program read only. Cleared by INIT or Device Reset.

TCRCIN
This bit is enabled only in internal maintenance mode and is used in diagnosing the transmitter CRC logic.
Program read only.
<table>
<thead>
<tr>
<th></th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>Reserved</td>
</tr>
<tr>
<td>14</td>
<td>RCRCIN</td>
</tr>
<tr>
<td></td>
<td>This is enabled only in internal maintenance mode and is used in diagnosing the receiver CRC logic. Program read only.</td>
</tr>
<tr>
<td>15</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
SYNCHRONOUS LINE INTERFACE, DUV11

FEATURES
- Transmission speeds up to 9600 bits per second
- Double-buffered program interrupt
- Full- or half-duplex operation
- Programmable Sync character
- Programmable character size (5, 6, 7, or 8 bits)
- Receiving Sync character stripping program selectable
- Automatic transmit of Sync program selectable
- Interfaces to Bell Series 200 synchronous modems or equivalent
- Auto answering capability
- Parity checking and generation
- Modem control
- Simple, compact, single-board design

INTRODUCTION
The DUV11 is a single-line, program-controlled, double-buffered communications device designed to interface the LSI-11 Processor to a serial synchronous line. The self-contained unit is fully programmable with respect to Sync character, character length (5 to 8 bits), and parity selection.

This interface will allow one of two modes of data transmission. Either synchronous or asynchronous transmission can be selected by the program.
DUV11

The DUV11 is ideally suited for interfacing the LSI-11 to high-speed synchronous lines for remote batch, remote data collection, and remote concentration applications. Multiple DUV11's on a LSI-11 allow its use as a synchronous line concentrator or front-end synchronous controller to a larger computer.

The DUV11 provides serial-to-parallel and parallel-to-serial data conversion, voltage level conversion, and modem control for half- or full-duplex operation. The Bell Series 200 synchronous modems or equivalent may be used with the DUV11.

Modem control is a standard feature of the DUV11. The necessary signals needed to establish communications with the Bell Series 200 synchronous modems are present in the Receive Status Register (RxCSR). No transition of control lines emanating from the modem directly cause a change in the state of the transmitter or receive logic.

The DUV11 is capable of transmitting data at the following speed:

EIA/CCITT: 9600 bits per second maximum
(limited by modem and data set interface level converters)

The DUV11 conforms to Electronic Industries Association (EIA) specification RS-232-C and CCITT Recommendation V.24.

OPERATION

General

The DUV11 is a character buffered synchronous serial line interface capable of two-way simultaneous communications. The DUV11 translates between serial data and parallel data. Output characters are transferred in parallel from the LSI-11 Q-BUS into the DUV11 where they are serially shifted to the communication line. Input characters from the modem are shifted into the DUV11 and made available to the LSI-11 on an interrupt basis.

Synchronization between the DUV11 and the transmitting device is established by a Sync character code. Both the receiver and transmitter are double buffered. This allows a full character time in which to service transmitter and receiver interrupts. The clocking necessary to serialize the data is provided by the associated high-speed synchronous modem.

The DUV11 consists of five registers: two status registers, two data buffer registers, and a Parameter Control Register which is used to control characteristics of the interface such as mode of operation (synchronous internal or external), number of bits per character, parity selection, and the Sync character.

For local connection (no modem) or for use with a modem without a clock, an external clock source is required. When using the H312-A null modem pin 24 of the A selection is provided for an external clock connection.

Synchronous Mode—Transmitter Section

The transmitter section of the DUV11 performs parallel-to-serial conversion of data supplied to it from the LSI-11 Q-BUS.
After the initialize pulse, the program must set the Parameter Control Register for the mode of operation (in this case synchronous), the desired character length (5, 6, 7, or 8 bits—parity not included), and the mode of parity.

Before any necessary handshaking with the data set, the program may load the Sync Register with the desired character. When the Sync Register is loaded, the character will be used for both the Receiver and Transmitter operations. Any required handshaking to establish connection with the data set may be done at this time.

Once handshaking is complete, the program can assert the Send bit in the Transmitter Status Register (TxCSR). When Send is asserted, the transmitter is enabled but will not start transmitting data until the first character is loaded into the Transmitter Data Buffer (TxDBUF). If Send is cleared during transmission, the character currently being transmitted will be completed, the line will go to a mark hold state, the internal transmitter logic will be reset, and synchronization will be lost. When Send is cleared, there is no guarantee that the Transmitter Done bit will assert upon completion of transmission of the current character.

When it is necessary to know when the last bit of the last character has been transmitted, the following steps may be taken: Prior to loading the Transmitter Data Buffer (TxDBUF) with the last character, the DNA INTR EN (Data Not Available Interrupt Enable) bit should be asserted in the Transmitter Status Register (TxCSR) and the Tx DONE INTR EN bit should be cleared. The interrupt in the transmitter logic subsequent to the loading of the TxDBUF will signify the completion of the transmission of the last character.

The transmission of initial Sync characters may be accomplished through either of the following two methods:

1. The program must arrange its data buffer such that the required number of Sync characters precedes any text. The Sync Register may or may not contain the Sync character. If the Sync Register is not loaded, it will contain an all-ones character subsequent to a master reset or initialize.

Assuming that any necessary handshaking has been completed with the data set and that Send has been asserted, the program can commence transmission from its data buffer.

When the first data bit is transferred to the communications line, the Transmitter Done bit will be asserted. If the Transmitter Interrupt Enable bit is set, an interrupt request will be generated.

If the Sync character was not initially loaded into the Sync register, then synchronization cannot be guaranteed unless the program response to the Transmitter Done Bit is less than 1 bits per second x (bits per character—1/2 bit time) seconds. This can be verified by the absence of the Data Not Available (DNA) bit in the TxCSR and applies only to the transmission of the initial Sync characters.
Subsequent synchronization can be maintained by having the program insert Sync characters into the message at the established intervals.

An alternate method of maintaining subsequent synchronization would be to load the Sync Register with the Sync character and assert the Data Not Available Interrupt Enable bit in the TxCSR. The program could ignore the service of the Transmitter Done bit at certain intervals by clearing the Transmitter Done Interrupt Enable bit. During this interval, transmission would be from the Sync Register. When transmission from the Sync Register begins, the Data Not Available bit will assert, causing an interrupt request. As long as the program ignores the Transmitter Done Bit, transmission will emanate from the Sync Register.

If desired, the program can ignore the Data Not Available bit by clearing its Interrupt Enable.

2. Following any necessary handshaking procedure and the assertion of Send, the program loads the Sync Register with the Sync character and asserts Data Not Available Interrupt Enable. The program then clears the Transmitter Done Interrupt Enable (if it was set) and then loads TxDBUF with the Sync character. At this point, transmission begins. No interrupt request will be generated by the transmission of the first character unless the Transmitter Done Interrupt Enable bit is set. The first bit of the second character will cause an interrupt request. At this point, one Sync character has been transmitted. It is suggested that a minimum of five Sync characters be transmitted. In systems that are prone to error because of lost synchronization, as many as twelve Sync characters may be desired.

If more than one Sync character is required to achieve synchronization, the Data Not Available Interrupt requests can be monitored by the program. These requests will be continuous as long as the Transmitter Done bit goes unserviced and the Data Not Available Interrupt Enable bit is asserted.

Once synchronization has been established, subsequent synchronization can be monitored by delaying service of Transmitter Done and monitoring the Data Not Available bit.

Once synchronization is achieved, transmission of text will follow only if the program loads the text into the TxDBUF.

An intrinsic feature of the DUV11 is its ability to maintain synchronization even if the TxDBUF has not been updated. This is done by the transmitter idling out the contents of the Sync Register if the TxDBUF has not been updated in 1/Baud x (bits per character—½ bit time) seconds.

This means that if the transmitter were not serviced in the previously stated time frame, transmission would include data from the Sync Register. If this situation occurs, the Data Not Available bit will be set in the TxCSR. If desired, the program may set the DNA INTR EN bit and cause interrupt requests when Data Not Available comes true.
NOTE

The Send bit in the TxCSR must remain set for the duration of the message. An on-to-off transition will cause the transmitter to enter an idle state after completion of the character currently being transmitted.

Synchronous Mode—Receiver Section
The Receiver Section of the DUV11 performs serial-to-parallel conversion of 5, 6, 7, and 8-level codes.

SYNC INTERNAL MODE
The Parameter Control Register (PARCSR) controls both the transmitter and receiver configurations. Once the program has completed any necessary handshaking with the data set, the receiver data handling logic can be enabled. This is done by the program asserting Search Sync in the Receiver Status Register (RxCSR). This also enables the receiver to compare incoming characters with the character held in the Sync Register.

For the receiver to become synchronized with the transmitter, either one or two consecutive Sync characters must be recognized by the receiver. The number of characters is jumper selectable.

NOTE

Standard configurations will be set for two characters.

When this has happened, the Receiver Active bit will assert. Any characters received after Receiver Active has been asserted will cause interrupt requests, providing Receiver Interrupt Enable is set and the Strip Sync bit is not asserted.

NOTE

Search Sync must remain set for the duration of the message. If not, the character being received at the time of the on-to-off transition will be lost along with synchronization.

In some instances, the user may want the receiver to ignore Sync characters. This can be accomplished, providing the Receiver Active bit is set. First, the Sync character must be loaded into the Sync Register; then the Strip Sync bit in the RxCSR must be asserted. No interrupt requests will be generated when this character is received, although it does appear in the RxBUF until the next character is received. If bit 15 of the Receiver Data Buffer (RxDBUF) is asserted (signifying an error), the received Sync character will not be stripped and the RxDone bit will be asserted.

Overrun errors will occur in the receiver logic if the Receiver Done bit in the Receiver Status Register (RxCSR) is not serviced in 1/Baud x (bits
per character) seconds. When the overrun condition occurs, the character previously in RxDBUF is written over by the character causing the overrun.

SYNC EXTERNAL MODE

In this mode, the Parameter Control Register must be set for SYNC EXTERNAL. Refer to the description of the Mode Select bits for the actual setting. When the SYNC EXTERNAL mode has been selected, only the operation of the receiver logic differs; transmitter operation remains the same as described above. This is the only mode of operation in which the programs can force synchronization.

When the programmer asserts Search Sync, the Receiver Active bit will also assert even though no actual Sync characters have been received. If Search Sync is cleared, Receiver Active will also be cleared. Prior to the assertion of Search Sync the Receiver Data Buffer (RxDBUF) will appear as the serial line; that is, data will shift through the RxDBUF at the rate of the modem. No action in the receiver logic will result from this data being shifted, although the program can monitor this data stream. When the Search Sync bit is asserted, the receiver logic will start framing characters on the first bit received after Search Sync was asserted. The serial streams that appeared in the RxDBUF will be discontinued, and the Receiver Done bit will be asserted when the selected number of bits have been received. The received character will appear in the RxDBUF. Other than the differences mentioned, all other parameters and features of the synchronous receiver are applicable.

ISOCHRONOUS OPERATION

Isochronous operation is essentially asynchronous data transmission over a synchronous modem. Character synchronization is achieved by the use of start and stop bits attached to each character. These start and stop bits are added and removed from the character by the transmitter and receiver logic. The advantage of isochronous transmission over asynchronous is achievement of higher baud rates.

After initialization, the program must load the Parameter Status Register with the information used in controlling the operation and selection of parity.

For transmitter or receiver operation the following parameters must be specified: Isochronous mode, character length, and parity. If the receiver is being set up, the Sync Register must also be loaded and the Sync Search bit set.

When the required handshaking, if any, with the dataset is complete, transmission of data can begin after the assertion of SEND. As soon as the first character bit is placed on the communication line by the transmitter, the Transmit Done is asserted, and remains like this until the transmitter services the transmitter buffer or clears the SEND bit.

Receiver operation is initiated by the assertion of Search Sync (SCH SYNC). When this happens, the Receiver Active sets and the receiver starts framing characters upon receipt of the START bit from the transmitter. When the selected number of character bits are received, the
DUV11

receiver tests the line for a valid STOP bit, transfers the received character into the Receiver Data Buffer (RxDBUF) minus the START and STOP bits, and sets the Receiver Done. A framing error occurs if a STOP bit is not detected. Furthermore, if the program fails to service the RxDBUF before the next character is framed, an overrun error occurs.

PROGRAMMING

The five registers and their addresses are listed below:

1. Receiver Status Register (RxCSR) 16XXX0
2. Receiver Data Buffer Register (RxDBUF) 16XXX2
3. Parameter Control Register (PARCSR) 16XXX2
4. Transmitter Status Register (TxCSR) 16XXX4
5. Transmitter Data Buffer Register (TxDBUF) 16XXX6

All information between the DUV11 and the LSI-11 is transmitted in parallel fashion by byte or word. The RxCSR and TxCSR are addressable by word or byte. The PARCSR is write only by word operation. The RxDBUF is read only by word or byte. The TxDBUF is write only by word or byte to the even address only.

Data transfer is under program control. All data is transferred by the program (not a DMA device). Four contiguous Q-BUS addresses are required in the floating address area. Two contiguous interrupt vector addresses are required in the floating vector address area. The first vector of the set will have priority over the second if two interrupt requests are made simultaneously. The first vector will deal with conditions in the RxCSR. The second vector will deal with conditions in the TxCSR.

The initialize signal from the processor will generate a Master Reset in the DUV11. A description of the Master Reset bit and the bit assignments within each register are presented in the remainder of this section.

RECEIVER STATUS REGISTER (RxCSR)
Address: 16XXX0 (Addressable by word or byte)
<table>
<thead>
<tr>
<th>Bit 01</th>
<th>DATA TERMINAL READY</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>When set, this bit causes the data terminal lead to be asserted to the modem. Auto Dial and Manual call origination: maintains the established call. Auto Answer: allows handshaking in response to a ring signal. This bit is program read/write and is optionally cleared by INIT or Master Reset.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 02</th>
<th>REQUEST TO SEND</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>When set, this bit causes the Request to Send lead to be asserted at the modem interface. This bit is program read/write and is optionally cleared by INIT and Master Reset.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 03</th>
<th>SECONDARY TRANSMIT DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>This bit is connected to the secondary transmit line of the modem. With certain modems, supervisory data can be transmitted over this line at a reduced rate. It can also be used as a control lead; e.g., acknowledgement of messages. This bit is program read/write and is optionally cleared by INIT or Master Reset.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 04</th>
<th>SEARCH SYNC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SYNC INTERNAL MODE: When asserted to the receiver, this bit causes the receiver to start examining incoming characters for the Sync code held in the Sync Register. After the selected number of Sync characters are recognized, the Receiver Active bit is set. Either one or two Sync characters may be selected. The characters must be contiguous.</td>
</tr>
<tr>
<td></td>
<td>SYNC EXTERNAL MODE: In this mode, the Receiver Active bit will assert at the same time the Search Sync bit is asserted. Character framing will start with the first bit received after Search Sync has been asserted; character framing ends after the number of bits per character specified in the word length (select bits of the PARCSR) have been received. Once Receiver Active is asserted, this bit must stay asserted or synchronization will be lost, and the receiver will go into an idle state.</td>
</tr>
<tr>
<td></td>
<td>This bit is program read/write and is cleared by INIT and Master Reset.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 05</th>
<th>DATA SET INTERRUPT ENABLE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>When set, this bit allows interrupt requests to be made to the receiver vector if the Data Set Change bit is asserted. This bit is program read/write and is cleared by INIT and Master Reset.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 06</th>
<th>RECEIVER INTERRUPT ENABLE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>When set, this bit allows interrupt requests to be made to the receiver vector if the Receiver Done bit is set.</td>
</tr>
</tbody>
</table>
This bit is program read/write and is cleared by INIT and Master Reset.

**Bit 07**  
**RECEIVER DONE**  
This bit is set when a character is transferred into the Receiver buffer. If, however, the Receiver Active bit is set and the Strip Sync bit is a one, and the character received is a Sync character, the Receiver Done bit will not be set, providing bit 15 of the RxDBUF is clear.

This bit is program read/only and is cleared by reading RxDBUF, INIT, and Master Reset.

An interrupt request will be generated if the Receiver Interrupt Enable bit is set when this bit is asserted.

**Bit 08**  
**STRIP SYNC**  
When this bit is set, characters that match the contents of the Sync Register will be ignored, provided bit 15 of the Receive Data Buffer Register is not asserted. In this case, the Receiver Done bit will not be asserted.

This bit is program read/write and is cleared by INIT and Master Reset.

**Bit 09**  
**DATA SET READY**  
This bit is a direct reflection of the Data Set Ready (or interlock) lead emanating from the modem. This line, when asserted, indicates that the modem is powered up, and is not in the test, talk, or dial mode. Any transition of this bit will cause the Data Set Change bit to be asserted.

Program read only.

**Bit 10**  
**SECONDARY RECEIVED DATA**  
This bit reflects the state of the Secondary Received Data line emanating from the modem. Any transition on this line will cause the Data Set Change bit to assert. With certain modems, supervisory data can be received over this line at a reduced rate. It can also be used as a control lead; e.g., acknowledgment of messages.

Program read only.

**Bit 11**  
**RECEIVER ACTIVE**  
When operating in the synchronous mode using internal synchronization, this bit will be set when the selected number of contiguous Sync characters have been recognized (either 1 or 2). If the Sync EXTERNAL mode were selected, the Receiver Active bit will follow the state of the Search Sync bit.

This bit is program read and is cleared by INIT and Master Reset.
Bit 12  CARRIER
This bit is a direct reflection of the modem carrier. Any change in the status of this line causes the Data Set Change bit to be asserted.
Program read only.

Bit 13  CLEAR TO SEND
This bit reflects the state of the clear-to-send line of the modem. Any transition of this line causes the Data Set Change bit to set.
Program read only.

Bit 14  RING INDICATOR
This bit reflects the state of the modem ring line. Any transition of this line causes the Data Set Change bit to set.
Program read only.

Bit 15  DATA SET CHANGE
This bit is set by a transition on the following lines:
- Any transition on the Ring line.
- Any transition on the Carrier line.
- Any transition on the Data Set Ready line.
- Any transition on the Clear-to-Send line.
- Any transition of the Secondary Received Data.
If bit 05 of this register is set, the assertion of this bit will cause an interrupt to the receiver vector. This bit is cleared only by INIT, Master Reset, or when the RxCSR is read.

RECEIVER DATA BUFFER REGISTER (RxDBUF)
Address: 16XXX2 (Read Only—Addressable by word or byte)

Bits 00–07  RECEIVER DATA BUFFER
This buffer contains the data received from the modem with character lengths from 5-to-8 bits, plus parity if selected. The parity bit, if any, will be included as part of the received character and will appear as the bit following the most significant bit. In the case of 8-bit characters, no parity bit will be displayed.
The character in the RxDBUF is right-hand adjusted; bit 00 is the least significant bit of any character, and bit 07 is the most significant bit of an 8-bit character.
Subsequent to a Master Reset, this register contains all ones.
Program read.

Bits
08–11 RESERVED

Bit 12 PARITY ERROR
This bit is set when the receiver detects a parity error in the character received. The character will appear in the RxDBUF. The parity bit itself is available to the program for character length selection for less than 8 bits per character.
This bit is program read and is cleared by INIT, Master Reset, and by reading the RxDBUF low byte.

Bit 13 FRAMING ERROR
When set indicates that character received was not followed by a valid stop bit. This error only occurs in the isochronous mode of operation.
Read-only bit; cleared by INIT, Master Reset, and DTI SEL 2.

Bit 14 OVERRUN
When the receiver logic detects an overrun condition, this bit is set. An overrun is caused primarily by poor program response time.
Once the Receiver Done bit is set, the program must respond in 1/BPS x (Bits per character) seconds. If not, overrun will occur. This condition indicates the loss of at least one character. This bit will cause the error bit to assert.
This bit is program read only and is cleared by reading the RxDBUF low byte, INIT, or Master Reset.

Bit 15 Rx ERROR
This bit will be asserted if one of the three error bits in the RxDBUF are set (logical OR of bits 14 and 12).
This bit is program read only and is cleared only when bits 14, 13, and 12 are cleared.

PARAMETER CONTROL REGISTER (PARCSR)
Address: 16XXX2 (Write Only—Addressable by word or byte)
NOTE

If this register is inadvertently addressed with a byte operation, both bytes of the Q-BUS will be loaded. The unspecified byte may contain unwanted data.

The following bits are used to control the characteristics of the interface. These include mode of operation (synchronous internal or synchronous external), and isochronous number of bits per character, and parity selection. These bits are in an undefined state after power-up until programmed.

Bits 00–07  SYNCR REGISTER
This register contains the Sync character to be transmitted and used for receiver synchronization by the interface. The length of this character must correspond to the length of the data character. Parity does not have to be included if it has been selected.

Subsequent to a master reset, the internal transmitter Sync register will contain all ones; the receiver's internal Sync register will contain all zeroes.

Character length is adjusted from right to left, with bit 00 being the least significant bit and bit 07 the most significant bit for an 8-bit character.

Program write only.

Bit 08  EVEN PARITY SELECT
When the Parity Enable bit (bit 09) is set, the sense of the parity is controlled by this bit. When set, even parity will be generated by the transmitter and checked for by the receiver. The same will be done for odd parity when cleared.

Program write.

Bit 09  PARITY ENABLE
If this bit is set, parity generation and checking will be done. If bad parity is detected at the receiver, then the parity error flag will be set in the upper byte of the Receiver Data Buffer Register (RxDBUF).

Program write.

Bits 10 & 11  WORD LENGTH SELECT
These bits are used to select the number of bits per character, either 5, 6, 7, or 8. This selection does not include the parity bit, if parity is selected.
### Bits Per Character

<table>
<thead>
<tr>
<th>Bits Per Character</th>
<th>PARCSR</th>
<th>Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Program write.

### Bits

#### 12 & 13

**MODE SELECT 01, 00**

The function of these bits is to select the mode of operation: synchronous internal or synchronous external. The following table shows the legal configurations possible with the DUV11. All other combinations of the mode select bits will produce errors in the interface.

<table>
<thead>
<tr>
<th>MODE</th>
<th>PARCSR</th>
<th>Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synchronous External</td>
<td>13</td>
<td>12</td>
</tr>
<tr>
<td>Synchronous Internal</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Isochronous</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Program write.

#### 14 & 15

**RESERVED**

### TRANSMITTER STATUS REGISTER (TxCSR)

Address: 16XXX4 (Addressable by word or byte)

**Bit 00** **BREAK**

When this bit is asserted, the serial output of the transmitter is held in the space condition. If the program presents data to the transmitter during this period, the operations to the program will appear normal. An interrupt request will be generated at the normal time even though a character was never actually transferred.
NOTE

The setting of this bit is not recommended when operating in the synchronous mode except for maintenance programming.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 01  RESERVED

Bit 02  RESERVED

Bit 03  HALF DUPLEX/FULL DUPLEX
When this bit is set, operation will be in the half-duplex mode. In the half-duplex mode, the receiver will be disabled if the Send bit in the TxCB is asserted.

This bit is read/write and is cleared by INIT or Master Reset.

Bit 04  SEND
When asserted, this bit enables the transmitter. Once the transmitter is enabled, transmission will start when the first character has been loaded into the TxBUF. This line must remain true for the length of the entire message. If not, the current character in the shift register will be transmitted, and the transmitter will go into an idle state.

This bit is used in all modes of operation.

This bit is program read/write and is cleared by Master Reset or INIT.

Bit 05  DNA INTR EN (DATA NOT AVAILABLE INTERRUPT ENABLE)
Allows interrupt requests to be made to the transmitter vector if the Data Not Available bit is set. This bit is set if the user wants to know if a filler character was sent while in data mode via an interrupt or to notify the program when the last bit of a character has been transmitted.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 06  TRANSMITTER INTERRUPT ENABLE
When set, this bit will allow a program interrupt request to be generated by the Transmitter Done bit.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 07  TRANSMITTER DONE
This bit will be set when the first bit of the character contained in the TxBUF is presented to the line. At that time, the program can load another character into the transmitter buffer.
DUV11

If the transmitter interrupt enable bit is set, this bit will generate an interrupt request to the transmitter vector.

Program read. Cleared by writing a character into the TxDBUF. Reset by INIT or Master Reset.

Bit 08

MASTER RESET (MR)

This bit is used to place the transmitter and receiver in an idle state (not to be confused with idle mode). The Q-BUS Initialize signal will also place the DUV11 in an idle state.

When the transmitter is placed in an idle state, the following conditions exist:

1. All internal timing is reset.
2. The contents of the Sync register, internal to the transmitter, will be all ones.
3. All the bits in the TxCSR may be reset except the Transmitter Done bit which will be set.
4. The TxDBUF will contain all ones.

When the receiver is in an idle state, the following conditions exist:

1. All internal timing is reset.
2. The contents of the Sync register, internal to the receiver, will be all zeroes.
3. The following bits in the RxCSR will be cleared:
   - Data Set Change
   - Receiver Active
   - Strip Sync
   - Receiver Done
   - Receiver Interrupt Enable
   - Data Set Interrupt Enable
   - Search Sync

The following bits of the RxCSR may be optionally excluded from the bits cleared by a Master Reset or INIT signal:

- Secondary Transmit Data
- Request to Send
- Data Terminal Ready

The contents of the TxDBUF will be all ones in the low byte. In the high byte, the Error, Overrun, Frame Error, and Parity Error bits will be cleared.

The contents of the high byte in the Parameter Control Register (PARCSR) will be unaffected by the Master Reset.

Immediately after power-up, these bits will be in an undefined state.

NOTE

This bit is one-shot; that is, it will be asserted for 3 μsec and then return to the zero state.
**Bit 09**  
RESERVED

**Bit 10**  
MAINTENANCE BIT WINDOW  
When in the maintenance mode 01 or 00, this bit can be used to monitor the input to the receiver logic. The stimulus that creates the input could be either the Maintenance Data bit or the serial output of the transmitter, depending on the state of the Break bit.  
Program read only.

**Bits**  
11 & 12  
MAINTENANCE MODE SELECT (BITS 01 & 00)  
These bits are used to select any one of three maintenance modes:

<table>
<thead>
<tr>
<th>BIT SETTING</th>
<th>12</th>
<th>11</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Internal Maintenance Mode</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2. External Maintenance Mode</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3. Internal Maintenance Mode for Systems Testing</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**INTERNAL MAINTENANCE MODE (01)**  
Internal maintenance mode clocking comes from the Clock bit (bit 13) driven via the program. While using this mode, the following EIA level converters are disabled (this is done so that the majority of the logic can be diagnosed without disconnecting the modem cable):

- Receiver Clock  
- Transmitter Clock  
- Receiver Data  
- Transmitter Data

Modern control flags should be cleared and not used in this mode. All inputs that were driven by the modem will now be simulated by the program setting the appropriate flags. The function of the half-duplex bit in the TxCSR cannot be tested in this mode. The external maintenance mode must be used to test this function.

**EXTERNAL MAINTENANCE MODE (10)**  
When in the external maintenance mode, all lines connected to the data set must be removed at the data set interface. A special connector replaces the connector of the data set. The function of the special connector is to turn around specified signals after level conversion and bring them back to the DUV11 as simulated inputs.

The test loop back connector to be used in the H315 connector.

Clocking in this mode is under control of the maintenance clock bit. Refer to clock bit description for its characteristics. This is the only mode that can be used to check out the function of the Half-Duplex bit.
INTERNAL MAINTENANCE MODE FOR SYSTEMS TESTING (11)

With bits 12 and 11 both set to a one (mode 11), the internal maintenance mode provides an adequate method of clocking the receiver and transmitter. The clocking method should not be synchronous to the program. An RC clock is provided in the interface for this purpose. Mode 11 will be the same as mode 01 with respect to data set control lines. The only difference is that Receiver and Transmitter clocking is derived from an RC clock at 5 kC.

NOTE

If bits 12 and 11 are zero, normal operating mode is assumed.

These bits are program read/write and are cleared by INIT or Master Reset.

Bit 13 MAINTENANCE CLOCK
This bit is used to simulate the Transmitter and Receiver clock. It is used for diagnostic purposes only. With this bit, the diagnostic has the ability to single step the interface. A 0-to-1 transition of this bit causes the transmitter to transfer a bit from the internal shift register to the output of the transmitter.
A 1-to-0 transition of this bit causes the receiver to transfer the input of the receiver into the internal shift register.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 14 MAINTENANCE DATA
This bit is used only in the maintenance mode by the diagnostic program. In either maintenance mode 01 or 10, this bit can be used to simulate data at the receiver input. When used as a simulated input to the receiver, the Break bit must be set to inhibit additional input from the transmitter. This bit should be cleared if it is not being used as the simulated input. If this bit were inadvertently set in maintenance mode and the Break bit was clear, the receiver input would have two sources of input.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 15 DATA NOT AVAILABLE
This bit is set by the transmitter logic when a character is transmitted from the Sync register. This applies only to synchronous operation and is caused by late or no program response.

The program response to the Transmitter Done bit must be within 1/Baud x (bits per character)—1/2 bits per second. If not, a character from the Sync register will be transmitted.
DUV11

If the Data Not Available Interrupt Enable bit is set in the TxCSR, it will cause an interrupt to the transmitter interrupt vector.

This bit is program read and is cleared by reading the TxCSR, INIT, Master Reset, and DTI SEL 4.

TRANSMITTER DATA BUFFER REGISTER (TxDBUF)
Address: 16XXX6 (Addressable by word or byte to the even address only)

<table>
<thead>
<tr>
<th>15</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESERVED</td>
<td>TRANSMITTED DATA BUFFER</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits
00–07 TRANSMITTER DATA BUFFER
This register is loaded by the program with the character to be transmitted. Character length is from 5 to 8 bits. The character is right-hand adjusted, with bit 00 being the least significant bit of any character and bit 07 the most significant bit of an 8-bit character. Any parity bit required is generated by the interface.

An INIT or Master Reset will place all ones in this register.
Program write.

Bits
08–15 RESERVED

CONTROL LEADS
The modem control leads are provided to interface the DUV11 to Bell Series 200 synchronous modems or equivalent. These leads allow the DUV11 to be used in switched or dedicated, full- or half-duplex configurations.

The DUV11 is connected to a Bell model 201 synchronous modem (or equivalent) by a 7.6m (25-foot) cable terminated at the modem end with a 25-pin male connector. Interface signals versus connector pin assignments are given below.

<table>
<thead>
<tr>
<th>PIN</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Signal or Protective Ground</td>
</tr>
<tr>
<td>2</td>
<td>Send Data</td>
</tr>
<tr>
<td>3</td>
<td>Receive Data</td>
</tr>
<tr>
<td>4</td>
<td>Send Request</td>
</tr>
<tr>
<td>5</td>
<td>Clear to Send</td>
</tr>
<tr>
<td>6</td>
<td>Interlock</td>
</tr>
<tr>
<td>7</td>
<td>Signal Ground</td>
</tr>
<tr>
<td>8</td>
<td>Carrier On-Off</td>
</tr>
<tr>
<td>15</td>
<td>Serial Clock Transmit</td>
</tr>
<tr>
<td>17</td>
<td>Serial Clock Receive</td>
</tr>
<tr>
<td>20</td>
<td>Data Terminal Ready</td>
</tr>
<tr>
<td>22</td>
<td>Ring Indicator 1</td>
</tr>
<tr>
<td>24</td>
<td>External Timing</td>
</tr>
</tbody>
</table>

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DUV11

SPECIFICATIONS

Function
Provides an interface between the LSI-11 BUS and a single synchronous bit serial communications channel.

Mechanical
The DUV11 consists of one quad (8½" x 10½") etched circuit card, and a 25-foot connecting cable terminated in a plug appropriate to the data communications equipment to be connected.

Operating Mode
Full- or half-duplex under program control.

Environmental
+5 to +50°C with a relative humidity of 10% to 95% (without condensation).

Power Requirements
+5 V at 1.2 A max
+12 at 0.45 A max

UNIBUS Loads
The DUV11 presents one unit load to the LSI-11 BUS

ORDERING INFORMATION
DUV11-DA Full/half duplex synchronous line module set. Double buffered, 5, 6, 7, or 8-bit characters. EIA/CCITT termination suitable for use with Bell Series 200 synchronous modems or equivalent. Includes 7.6m (25-foot) modem cable.

APPLICATIONS
Applications for high-speed synchronous communications interfaces vary widely, and new applications are being developed every day. These applications span all user groupings—commercial, industrial, scientific, and government.

Functionally, these applications may be divided into a few fundamental classes, such as:

- REMOTE DATA COLLECTION. Gathering information at a number of remote locations and transmitting it to a central processing point.
- REMOTE BATCH PROCESSING. The processing of batch or production jobs at a location remote to where the job is generated and the results are needed.
- REMOTE CONCENTRATION. Multiple DUV11s connected to an LSI-11 BUS enable it to be used as a synchronous line concentrator or front-end synchronous controller to a larger computer. The concentrator helps reduce line costs by concentrating data from several lines onto one high-speed line.
COMMUNICATIONS PREPROCESSOR, DV11

HIGHLIGHTS
- 8- or 16-line communications multiplexer for use with PDP-11 family computers.
- Synchronous and asynchronous lines can be intermixed on a 4-line basis.
- NPR data transfer on transmission and reception.
- Total 16-line throughput of up to 38,400 characters per second (9600 bits per second full duplex for each line).
- Control table scheme provides programming flexibility, particularly for special character and protocol handling.
- Open-ended flexible design—hardware not committed to any specific protocol.
- 128-character first-in/first-out receiver buffer.
- Program selectable block checks (LRC-8, CRC-16, CRC/CCITT) calculated by the hardware.
- Modem control.
- Synchronous lines have a choice of external or internal clock, two program-selectable sync characters for each line, and switch-selectable character sizes.
- Asynchronous lines have 16 program-selectable speeds and program-selectable formats for each line.
- Choice of external or internal clock.
- Two program-selectable sync characters for each line.
- Switch-selectable character sizes.
- Up to 4 DV11s with total throughput of 76,800 characters per second can be connected to a PDP-11 depending on configuration and application.

GENERAL DESCRIPTION
The DV11 is a communications preprocessor which permits eight or sixteen synchronous and/or asynchronous lines to be interfaced to a PDP-11. It is designed to relieve the PDP-11 processor of almost the entire overhead associated with interrupt handling, character processing and CRC/LRC calculations.
It provides very high throughput (up to 38,400 characters per second total for all 16 lines) and extremely flexible handling of special data link characters. High throughput is achieved by use of direct memory (NPR) transfers on both transmission and reception. Flexibility is achieved, without committing hardware to any specific protocol, through the use of control bytes stored in core tables. The program can specify parameters in each control byte, thus providing flexibility for requirements within a specific application.
The DV11 contains provisions for up to eight reception modes for use with character-oriented protocols (for instance, there are modes for
transparent data reception and for normal text reception). The action taken in each mode and the transition from one mode to another are controlled by control tables located in core memory. A control table for an individual reception state consists of 256 bytes—one for each of the possible characters that can be received during the reception.*

The DV11 hardware can perform block check calculations for longitudinal redundancy checks (LRC) and cyclic redundancy checks (CRC-16 and CRC/CCITT).

The character size (5, 6, 7, or 8 bits) and character format (no parity, even, or odd parity) of synchronous lines are switch-selectable for each 4-line group (0-3, 4-7, 8-11, 12-15). The character size (5, 6, 7, or 8 bits), character format (no parity, even, or odd parity; 1 or 2 stop units) and speed (50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 4800, 7200, 9600, and 38,400 bits per second of asynchronous lines are program-selectable for each line. The DV11 can calculate LRCs for all character sizes, and CRCs for 8-bit characters.

Two sync characters may be manually pre-selected for each 4-line group. Then the program can select from either of those two sync characters for each individual line. For transmission, the same sync character is used as the transmitter fill-character or an "all 1's" condition can be sent.

**PHYSICAL DESCRIPTION**

The DV11 consists of a 9-slot double system unit (DV11-AA) which contains the basic modules, plus a choice of three line groups. The DV11-BA consists of a distribution panel and line cards for eight synchronous lines. The DV11-BB consists of a distribution panel and line cards for eight asynchronous lines. The DV11-BC consists of a distribution panel and line cards for four synchronous and four asynchronous lines.

A total of two DV11-BAs, and DV11-BBs, and DV11-BCs can be used with one DV11-AA.

**BASIC OPERATION**

Sixteen LSI Receiver circuits (synchronous and/or asynchronous depending on configuration) assemble characters received from serial communications lines and assert a flag as each character is received. Sixteen LSI Transmitters disassemble characters and transmit them on serial communications lines and assert a flag whenever they can accept another character for transmission. The Master Scanner sequentially checks the receivers and transmitters for each line to see if a flag exists.

The microprocessor handles all characters received or transmitted by the DV11. It controls all non-UNIBUS data transfers and steps the Master Scanner. Except for those occasions where a UNIBUS instruction or NPR transfer involving the DV11 is taking place, the microprocessor never stops.

*Typically, control bytes are used to indicate how the character is to be handled, whether an interrupt is to be generated, and whether the character is to be included in the block check.
The microprocessor system includes a 128-character first-in/first-out storage buffer. While most characters received by the DV11 will propagate through this buffer and be directly transferred to PDP-11 core by means of an NPR transfer, the occasion may arise when the attention of the PDP-11 program is required before this is done. To prevent the receivers from experiencing data overruns during the interval that the DV11 is awaiting program attention, the microprocessor will continue to load the received characters into the first-in/first-out buffer, but the action of the microprocessor in withdrawing characters from the buffer will cease until the PDP-11 program responds to the interrupt caused by the special character at the bottom of the silo buffer. The character which requires PDP-11 program attention is copied into the Receive Interrupt Character Register at the time the interrupt is generated.

The Receiver Interrupt Character Register is a UNIBUS-addressable register used by the microprocessor to show the PDP-11 program any received character, along with line number and error flags for which the control logic requires assistance in processing.
The Receiver Control Byte Storage Register is a UNIBUS-addressable secondary register used to instruct the microprocessor how to process the character in the Receiver Interrupt Character Register.

The NPR control is the hardware which is used to gain control of the UNIBUS in order to store received characters, obtain characters for transmission, and to obtain control bytes that direct the character processing.

The microprocessor read/write random access memory (RAM) contains current addresses and 2's complement byte counts used in NPR transfers. The initial values are loaded by the PDP-11 program via the UNIBUS, and these values are subsequently updated by the microprocessor. The RAM also contains a line protocol word for each line by which the PDP-11 program can specify what action is to be taken when the byte count reaches zero and what type of block check polynomial should be used. In addition, a line state word is stored for each line providing a snapshot of what microprocessor activity is in progress at a particular line.

**RECEPTION OPERATION**

For synchronous lines, line synchronization and character assembly are accomplished by LSI synchronous receivers which initially compare groups of eight bits received on each line with the preselected sync character to achieve line synchronization. When line synchronization has been achieved, subsequently received characters are placed into a first-in/first-out, 128-character silo storage buffer. Each line receiver appends the line number (four bits) and any error flags (two bits—parity error, overrun error, framing error) to the character prior to placing it in the receiver storage buffer.

For asynchronous lines, character assembly is performed by the receiver portions of LSI circuits called Universal Asynchronous Receiver-Transmitters (UARTs). The UARTs automatically obtain line synchronization on the start bit of each received character. When a character has been assembled, it is placed into the 128-character silo storage buffer together with the line number (four bits) and any error flags (parity error, overrun error, framing error).

The DV11 microprocessor removes characters from the silo along with their line number and error flags. If there is an error flag (as a result of the parity error, framing error, or overrun error detected by the receiver), the character is placed in a UNIBUS-addressable register called the Receiver Interrupt Character Register, and an interrupt request is generated.

If there is no error flag, the DV11 processing depends on whether a character-oriented protocol (example: BISYNC) or a byte-count-oriented protocol (example: DDCMP) is being used.

**Character-Oriented Protocol Reception**

(Example: BISYNC)

If there is no error flag, the microprocessor affixes three mode bits at the high-order end of the received 8-bit character. This 11-bit character is then used as an offset in the PDP-11 control table to obtain a control
byte that will indicate to the microprocessor what mode is to be used for subsequent reception on this line and any special handling information appropriate to this character (such as whether or not to generate an interrupt, whether or not to include the character in a block-check computation, whether or not to store the character in a PDP-11 core message buffer).

If the generation of an interrupt is indicated, the character and the line number are moved to the Receiver Interrupt Character Register along with an error bit code. The error bit code indicates that this interrupt is being generated because a control table control byte has indicated that this is a special character.

If the control byte indicates that this character should be included in a block check, the DV11 microprocessor performs the appropriate calculation (LRC, CRC-16, or CRC/CCITT).

If the control byte directs that a received character be discarded, the character is discarded. If it indicates that the character be stored, the DV11 microprocessor obtains the current address from a secondary register associated with this line and uses that address to store the received character in a message buffer. The DV11 microprocessor then increments the current address secondary register for that line. In addition, the DV11 microprocessor increments the byte count secondary register for that line. If the storage of the character caused the byte count to reach zero, the microprocessor checks to see whether a mode change has been requested. Such a change is indicated by the Byte Count Register being initially loaded with bit 15 cleared. The new mode is stored by the PDP-11 program in the high byte of the Line State Secondary Register in approximately the same format as a control byte. Having accomplished any actions requested in this pseudo control byte, a copy of the character is moved to the Receiver Interrupt Character Register along with the error bits that indicate that a new receive message buffer must be established for this line. In all cases where a character is moved to the Receive Interrupt Character Register, an interrupt is generated, and the DV11 microprocessor ceases to withdraw characters from the receiver silo storage buffer until the PDP-11 program indicates that such withdrawal can proceed again (by setting a bit in the DV11 System Control Register).

Byte-Count-Oriented Protocol Reception
(Example: DDCMP)
If a byte-count-oriented protocol is used, Line Protocol Parameters bit 05 (DDCMP Receive) should be set by the PDP-11 program and the receiver mode should be set to 0. This will direct the DV11 microprocessor to skip the control byte process described above, include all characters in the Block Check Calculation, and store all characters (except BCC1 and BCC2). Details of character storage are the same as indicated above.

RECEIVER THROUGHPUT
The receiver throughput in the DV11 is dependent on the number of characters identified in the control bytes as being special (interrupt generating) and the size of the message buffers for received characters. It
is intended that the ability of control bytes to accomplish reception mode changes relieves the necessity for received special characters generating an interrupt. When a receiver interrupt is generated, received characters are accumulated in a 128-character first-in/first-out (silo) storage buffer until the interrupt is handled. Assuming arrival of characters at a 19,200-character-per-second rate, it would take approximately 6.6 milliseconds for a silo overflow to occur. Thus, substantial worst-case interrupt latency can be accommodated.

In response to a receiver interrupt indication, the PDP-11 program should set the System Control Register (bit 08) indicating that the DV11 microprocessor may resume processing the character in the Receiver Interrupt Character Register and resume withdrawing characters from the receive silo storage buffer.

If the program so desires, it may alter the receiver control byte stored in the Receiver Control Byte Storage Register before setting bit 08 in the System Control Register.

**TRANSMISSION OPERATION**

For each line there is a double-buffered serial transmitter. Transmitters for synchronous lines are packaged in separate LSI circuits, while transmitters for asynchronous lines share UARTs with the receivers. Whenever the transmitter buffer is empty, a flag is raised. The microprocessor scans for transmitter flags and when it finds one, it checks a "work sheet" to determine whether any special action must be taken (e.g., send a block check character). If no special action is required, the microprocessor checks to see if the transmitter "GO" bit for the line is set. If it is set, the microprocessor uses the transmitter current address register to perform an NPR transfer and obtain—from a core message buffer—a character to be transmitted. The DV11 processing of this character depends on whether a Character-Oriented Protocol (example: BISYNC) or a Byte-Count-Oriented Protocol (example: DDCMP) is being used.

**Character-Oriented Protocol Transmission (Example: BISYNC)**

Before transmitting the character, the microprocessor copies it, adds mode bits to the high-order end and performs an NPR to obtain a transmit control byte from a control table. This byte contains information indicating what new modes are to be used, whether to include the character in the block check, and whether to prefix the transmission of the character with a DLE (performed by the microprocessor).

**Byte-Count-Oriented Protocol Transmission (Example: DDCMP)**

If, after the switch in registers, the microprocessor finds the new byte count is also zero, it will clear "Transmit Go" in the Line State Register transmitter mode should be set to 0. This will direct the DV11 microprocessor to skip the control byte process described above and include all characters in the Block Check Calculation. The characters are transmitted as described below.

2-199
Transmission of Characters
The microprocessor loads the character to be transmitted into the appropriate line transmitter and increments the byte count. It then checks the byte count to determine whether it has reached zero. If it has, a check is made to determine whether a mode change has been requested. (Such a change is indicated by the byte count register being initially loaded with bit 15 cleared.) The new mode is stored by the PDP-11 program in the high byte of the Line Progress Secondary Register in approximately the same format as the control byte. Having accomplished any actions requested in this pseudo control byte, the microprocessor will switch to the other set of tables (i.e., from principal to alternate or vice versa). If the byte count that was just exhausted did not request a mode change via bit 15 on the Byte Count Register, the microprocessor will switch from principal to alternate (or vice versa) without reference to the upper byte of the Line Progress Secondary Register.

If, after the switch in registers, the microprocessor finds the new byte count is also zero, it will clear "Transmit Go" in the Line State Register and idle the line. On synchronous lines, the "Idle Mark" bit in the Line Protocol Parameters Register determines whether sync characters or ones are idled. On asynchronous lines, ones are always idled (mark hold).

On synchronous lines, the transmitters serialize each character, appending a parity bit if parity is enabled. On asynchronous lines, the transmitters serialize each character, adding a start bit, a parity bit if parity is enabled, and the stop bit(s).

**SYSTEM CONTROL REGISTER (SCR)—ADDRESS 775000 (775040, 775100, 775140)**
The System Control Register is a byte-addressable register. The bit assignments are as follows:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>NPR STATUS INTERRUPT (VECTOR B)</td>
</tr>
<tr>
<td>14</td>
<td>UNUSED</td>
</tr>
<tr>
<td>13</td>
<td>NPR STATUS INTERRUPT ENABLE</td>
</tr>
<tr>
<td>12</td>
<td>STORAGE INTERRUPT ENABLE</td>
</tr>
<tr>
<td>11</td>
<td>MASTER CLEAR</td>
</tr>
<tr>
<td>10</td>
<td>NPR STATUS OVERFLOW INTERRUPT (VECTOR B)</td>
</tr>
<tr>
<td>9</td>
<td>SYSTEM MAINTENANCE</td>
</tr>
<tr>
<td>8</td>
<td>RECEIVER INTERRUPT RESPONSE</td>
</tr>
<tr>
<td>7</td>
<td>RECEIVER INTERRUPT (VECTOR A)</td>
</tr>
<tr>
<td>6</td>
<td>RECEIVER INTERRUPT ENABLE</td>
</tr>
<tr>
<td>5</td>
<td>MEMORY EXTENSION</td>
</tr>
<tr>
<td>4</td>
<td>FOR MAINTENANCE USE</td>
</tr>
<tr>
<td>3</td>
<td>MICROPROCESSOR GO</td>
</tr>
</tbody>
</table>

Bits Description

00 Microprocessor Go

This bit, when set, permits the DV11 to operate its microprocessor. This is read/write, cleared by initialize. System programs must set this bit for the DV11 to function.

2-201
<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
</table>
| 01   | (For Maintenance Use)  
Do not write one’s here |
| 02   | (For Maintenance Use)  
Do not write one’s here |
| 03   | (For Maintenance Use)  
Do not write one’s here |
| 04-05| Memory Extension  
For the line number entered in bits 00-03 of the Secondary Register Selection Register, the information stored in these bits becomes bits 16 and 17, respectively, of any current address or control table base address loaded by the program into the RAM. These bits are read/write (cleared by Initialize) but when read, represent only the status of bits 4 and 5 of the System Control Register, not the status of address bits 16 and 17 of the selected line. See the Line Control Register for further information. This arrangement permits interrupt service routines to save the contents of the System Control Register accurately. |
| 06   | Receiver Interrupt Enable  
This bit, when set, permits the setting of bit 7 to generate an interrupt request. This bit is read/write, and is cleared by Initialize. |
| 07   | Receiver Interrupt (Vector A)  
This bit, when set, indicates that the microprocessor has either (1) withdrawn a byte from a core control table indicating that an interrupt should be generated for the character presently being processed, or (2) the character presently being processed has one or more of its associated error flags set, or (3) experienced a zero byte count, non-existent memory location, or memory parity error in processing this character. The program should respond to this interrupt by setting SCR08. (The program might wish to alter the control byte in the Receiver Control Byte Storage Register before setting SCR08.) This bit is read-only, except when SCR09 is set. It is cleared by Initialize. |
| 08   | Receiver Interrupt Response Completed  
The setting of this bit clears SCR07 and allows the microprocessor to take action on the character in the RICR (according to the information stored in the Receiver Control Byte Storage Register) and to continue removing characters from the receive silo for processing. |
| 09   | For Maintenance Use  
This bit, when set, permits the program to write bits 7 and 15 of this register. This bit is read/write and is cleared by Initialize. This register must be word-addressed when and while this bit is set. |
<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>NPR Status Overflow Interrupt (Vector B)</td>
</tr>
<tr>
<td></td>
<td>This bit, when set, indicates that the DV11 hardware checked the NPR Status</td>
</tr>
<tr>
<td></td>
<td>Register (a 64-entry silo) and found that there was no room for the entry</td>
</tr>
<tr>
<td></td>
<td>due to insufficient program attention to servicing this register. All DV11</td>
</tr>
<tr>
<td></td>
<td>transmitter action in performing NPR transfers will cease until this</td>
</tr>
</tbody>
</table>
|      | condition is corrected. This bit is read/write and is cleared by Initialize.
| 11   | Master Clear                                                                |
|      | This bit, when set, generates "Initialize" within the DV11 data handling    |
|      | sections. (It does not affect the modem control.) The silos (both received |
|      | character and NPR status*) are cleared. The secondary registers are not       |
|      | cleared. This bit is write-only (reads as zero, as it is self-clearing).    |
| 12   | Storage Interrupt Enable                                                    |
|      | This bit, when set, permits the setting of bit 10 to generate an interrupt  |
|      | request. This bit is read/write and is cleared by Initialize.               |
| 13   | NPR Status Interrupt Enable                                                 |
|      | This bit, when set, permits the setting of bit 15 to generate an interrupt  |
|      | request. This bit is read/write and is cleared by Initialize.               |
| 14   | Unused                                                                      |
| 15   | NPR Status Interrupt (Vector B)                                            |
|      | This bit is set whenever there are one or more entries in the NPR Status    |
|      | Register, which is a silo-type register. The reading of that read-once     |
|      | register clears this bit, but it resets again if a new entry moves down     |
|      | into the register to replace the previously read entry. This bit is read-only|
|      | except when SCR bit 09 is set, when it is read/write. This bit is cleared    |
|      | by Initialize.                                                              |

*The NPR Status Register, bit 15 ("Entry Present"), is cleared by Initialize; the other bits are not.

**RECEIVER INTERRUPT CHARACTER REGISTER (RICR)—**
**ADDRESS 775002 (775042, 775102, 775142)**
This register is read-only and is cleared by Initialize.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-12</td>
<td>ERROR CODE</td>
</tr>
<tr>
<td>11-8</td>
<td>LINE NUMBER</td>
</tr>
<tr>
<td>7-0</td>
<td>INTERRUPTING CHARACTER</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-07</td>
<td>Interrupting Character</td>
</tr>
<tr>
<td></td>
<td>These bits contain the interrupting</td>
</tr>
<tr>
<td></td>
<td>character, right-justified. The least</td>
</tr>
<tr>
<td></td>
<td>significant bit is bit 00. On parity-</td>
</tr>
<tr>
<td></td>
<td>equipped characters, less than eight</td>
</tr>
<tr>
<td></td>
<td>bits, the parity bit will appear</td>
</tr>
<tr>
<td></td>
<td>immediately to the left</td>
</tr>
</tbody>
</table>
Bits | Description
--- | ---
| of the highest-order bit in the character on synchronous lines and will not appear on asynchronous lines. See special note associated with Error Code 0101 below.

08-11 Line Number
These bits indicate the line number on which the interrupting character was received. Bit 8 is the least significant bit.

12-15 Error Code
These bits indicate the reason that the character shown in bits 00-07 generated an Interrupt request. The meaning of these bits depends on whether the line is synchronous or asynchronous.

<table>
<thead>
<tr>
<th>Error Code Bits</th>
<th>Meaning (Synchronous Lines Only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 14 13 12</td>
<td>SPECIAL CHARACTER</td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>The receipt of this character caused the seizure of a control byte which had bit 00 (generate interrupt) set indicating that this is a special character.</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>PARITY ERROR</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>This character was received with a parity sense opposite to that selected for this line by the parity sense switches on the line card.</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>OVERRUN</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>The character(s) preceding this character on this line has (have) been lost due to failure of the DV11 receiver system to keep up with the incoming character rate on this line.</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>PARITY ERROR AND OVERRUN</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>(See previous listings)</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>BYTE COUNT WARNING</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>This character has been stored, but it is the last character that can be stored for this line as the byte count is now zero for reception on this line.</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>BLOCK CHECK COMPLETED</td>
</tr>
<tr>
<td></td>
<td>A block of text or data and the associated block check characters have been received and the program should now check the accumulated receiver block check; the DV11 presents the OR of the high and low bytes of that register in bits 00-07 of this register.</td>
</tr>
</tbody>
</table>
### DV11

<table>
<thead>
<tr>
<th>Error Code Bits</th>
<th>Meaning (Synchronous Lines Only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 1 1 0</td>
<td>UNDEFINED</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>UNDEFINED</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>BYTE COUNT ZERO</td>
</tr>
<tr>
<td></td>
<td>This character was not stored, as the byte count for reception on this line is zero and thus there is no place to store this character.</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>UNDEFINED</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>UNDEFINED</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>UNDEFINED</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>PROCESSING ERROR 00</td>
</tr>
<tr>
<td></td>
<td>A nonexistent memory time-out occurred when the DV11 attempted to store this character.</td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>PROCESSING ERROR 01</td>
</tr>
<tr>
<td></td>
<td>A nonexistent memory time-out occurred when the DV11 attempted to obtain the control byte associated with this character.</td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>PROCESSING ERROR 10</td>
</tr>
<tr>
<td></td>
<td>A memory parity error occurred when the DV11 attempted to store this character. (NOTE: This error should never occur, as the memory parity logic gives alarms only on DATI transfers.)</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>PROCESSING ERROR 11</td>
</tr>
<tr>
<td></td>
<td>A memory parity error occurred when the DV11 attempted to obtain the control byte associated with this character.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Error Code Bits</th>
<th>Meaning (Asynchronous Lines Only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 14 13 12</td>
<td>SPECIAL CHARACTER</td>
</tr>
<tr>
<td></td>
<td>The receipt of this character caused the seizure of a control byte which has bit 00 (generate interrupt) set indicating that this is a special character.</td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>PARITY ERROR</td>
</tr>
<tr>
<td></td>
<td>The character was received with a parity sense opposite to that selected for this line by the programmable Format Register.</td>
</tr>
</tbody>
</table>

2-205
<table>
<thead>
<tr>
<th>Error Code Bits</th>
<th>Meaning (Asynchronous Lines Only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 1 0</td>
<td>OVERRUN</td>
</tr>
<tr>
<td></td>
<td>The character(s) preceding this character on this line has (have) been lost due to failure of the DV11 receiver system to keep up with the incoming character rate on this line.</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>FRAMING ERROR</td>
</tr>
<tr>
<td></td>
<td>The line was in the spacing state (0) at the time of the first stop bit of this character. The FRAMING ERROR code can be used to detect break. Following a framing error, the serial line must return to the mark state (1) for at least 1/16 bit time before subsequent characters will be assembled on the line. A framing error occurring together with a parity error will be indicated as a FRAMING ERROR (code 0011). A framing error and/or parity error occurring together with an overrun error will be indicated as an OVERRUN (code 0010).</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>BYTE COUNT WARNING</td>
</tr>
<tr>
<td></td>
<td>This character has been stored, but it is the last character that can be stored, as the byte count is now zero for reception on this line.</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>BLOCK CHECK COMPLETED</td>
</tr>
<tr>
<td></td>
<td>A block of text or data and the associated block check characters have been received and the program should now check the accumulated receiver block check; the DV11 presents the OR of the high and low bytes of that register in bits 00-07 of this register.</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>UNDEFINED</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>UNDEFINED</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>BYTE COUNT ZERO</td>
</tr>
<tr>
<td></td>
<td>This character was not stored, as the byte count for reception on this line is zero and there is no place to store this character.</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>UNDEFINED</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>UNDEFINED</td>
</tr>
<tr>
<td>Error Code Bits</td>
<td>Meaning (Asynchronous Lines Only)</td>
</tr>
<tr>
<td>-----------------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>UNDEFINED</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>PROCESSING ERROR 00</td>
</tr>
<tr>
<td></td>
<td>A nonexistent memory time-out occurred when the DV11 attempted to store this character.</td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>PROCESSING ERROR 01</td>
</tr>
<tr>
<td></td>
<td>A nonexistent memory time-out occurred when the DV11 attempted to obtain the control byte associated with this character.</td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>PROCESSING ERROR 10</td>
</tr>
<tr>
<td></td>
<td>A memory parity error occurred when the DV11 attempted to store this character. (NOTE: This error should never occur, as the memory parity logic gives alarms only on DATI transfers.)</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>PROCESSING ERROR 11</td>
</tr>
<tr>
<td></td>
<td>A memory parity error occurred when the DV11 attempted to obtain the control byte associated with this character.</td>
</tr>
</tbody>
</table>

In response to a receiver interrupt (SCR07), the PDP-11 program should examine this register (Receiver Interrupt Character Register), make any desired changes in the Receiver Control Byte Storage Register, and then set SCR08.

In the case of code 0000, Special Character, the Receiver Control Byte Storage Register will contain the control byte associated with the Special Character, but with its bit 00 (generate interrupt) cleared to zero. Thus, for those characters where an interrupt is desired merely to advise the program of reception of a particular character, the program will typically wish to set SCR08 without changing the contents of the Receiver Control Byte Storage Register. For all other error codes, the microprocessor creates a special “remain in mode specified by last control byte fetched for this line, do not include in BCC, do not expect BCC1 next, do not store, do not interrupt” control byte and stores that in the Receiver Control Byte Storage Register before initiating a receiver interrupt request. Thus, for those characters or conditions specifying occurrence of an error, the PDP-11 program can dispose of the character by merely setting SCR08. If desired, the Receiver Control Byte Storage Register may be changed before SCR08 is set.

**LINE CONTROL REGISTER (LCR)—ADDRESS 775004**

(775044, 775104, 775144)

(Synchronous Lines Only)

This register controls the maintenance features associated with each synchronous line in the DV11 and provides an opportunity for the PDP-11
program to read the extended address bits for each line. This register is word-addressable only. 

Bits indicated to be “write-only” will be read back in the state they were last set. Since this is not a presentation of the corresponding bit for the selected line, the bit is referred to as “write-only.”

The bit functional assignments are as follows:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-01</td>
<td>Reserved for Maintenance (CAUTION: Various bits may appear here during normal DV11 operation.)</td>
</tr>
<tr>
<td>02-03</td>
<td>Unused</td>
</tr>
</tbody>
</table>
| 04-05 | Extended Address Read (Read-Only)  
For the line number entered in bits 00-03 of the Secondary Register Selection Register, these bits represent the status of bits 16 and 17 of the secondary register specified by bits 08-11 of the Secondary Register Selection Register. This permits the PDP-11 program to read the Extended Address bits of the Current Address and Control Table Base Address entries in the RAM. |
| 06 | Unused |
| 07 | Maintenance (Read-Only) (CAUTION: Various bits may appear here during normal DV11 operation.) |
| 08 | Maintenance |
| 09 | Maintenance (See bit 15) |
| 10 | Sync Select (See bit 15)  
Each four-line group of the DV11 (0-3, 4-7, 8-11, 12-15) has associated with it two switch-selectable sync/fill characters referred to as Sync A and Sync B. For each individual line in that group (as entered in bits 00-03 of the Secondary Register Selection Register), the setting of this bit determines whether Sync A (bit = 0) or Sync B (bit = 1) is used. This bit is write-only and is cleared by Initialize. |
11-12 Maintenance Mode Select (Maintenance) (See bit 15)

Bits 11 and 12 are write-only and are cleared by Initialize. Normal operating mode is 00.

13 Receiver Enable (See bit 15)

When this bit is set by the program, a sync search is initiated on this line by the receiver logic. After an Initialize, this bit must be set by the program before any reception can begin on this line (i.e., Receiver Active (See “Line State” secondary register) will not set unless this bit has been set).

A switch for each line determines whether the receiver searches for one sync character or for two in a row.

A successful sync search results in the setting of Receiver Active (Line State bit 00) for this line.

This bit is write-only and is cleared by Initialize.

NOTE

Should it be desired to resynchronize during the course of reception, the program could accomplish this by setting “Receiver Resynchronize” (Line State 01). To shut down reception on a line, the program should clear Receiver Enable and then set Receiver Resynchronize.

14 Maintenance (See bit 15)

15 Line Control Strobe (Read/Write—Self-Clearing)

The setting of this bit records the status of bits 09, 10, 11, 12, 13, and 14 into the per-line status flip-flops associated with the line specified in bits 00-03 of the Secondary Register Selection Register. This bit is self-clearing, thus write-only. It may be set at the same time as the bits whose status it records, as its action is delayed until the conclusion of the instruction cycle which set it and the proper phasing of the DV11 internal clocks. This bit is necessary due to “reads” in the PDP-11/20 being “read/write” cycles and certain synchronization requirements associated with mode changes during clocking pulses. The bits marked “Maintenance” should be written to zero for normal DV11 use.

NOTE

After setting this bit, do not change bits 00-03 of the Secondary Register Selection Register until this bit has self-cleared indicating conclusion of the strobe operation.

2-209
LINE CONTROL REGISTER (LCR)—ADDRESS 775004  
(775044, 775104, 775144)  
(Assynchronous Lines Only)

This register controls maintenance features, speed, and character formats for each asynchronous line in the DV11 and provides an opportunity for the PDP-11 program to read the extended address bits for each line. This register is word-addressable only. Bits indicated to be "write-only" will read back in the state they were last set. Since this is not a presentation of the corresponding bit for the selected line, the bit is referred to as "write-only."

The bit functional assignments are as follows:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-01</td>
<td>Reserved for Maintenance (CAUTION: Various bits may appear here during normal DV11 operation.)</td>
</tr>
<tr>
<td>02-03</td>
<td>Unused</td>
</tr>
</tbody>
</table>
| 04-05 | Extended Address Read (Read-Only)  
   For the line number entered in bits 00-03 of the Secondary Register Selection Register, these bits represent the status of bits 16 and 17 of the secondary register specified by bits 08-11 of the Secondary Register Selection Register. This permits the PDP-11 program to read the Extended Address bits of the Current Address and Control Table Base Address entries in the RAM. |
| 06-08 | Unused |
| 09-10 | Register Selection Code (See bit 15)  
   Each individual asynchronous line (as entered in bits 00-03 of the Secondary Register Selection Register) has associated four 4-bit registers. Bits 09-10 determine which register is selected when writing into the Line Control Register. These bits are write-only and cleared by Initialize. |

<table>
<thead>
<tr>
<th>Bit 10</th>
<th>Bit 9</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Primary</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Format</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Baud Rate</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Maintenance</td>
</tr>
</tbody>
</table>
11-14 Register Bits (See bit 15) (Write-Only)
These four bits of the Line Control Register are used to access
the selected four-bit register (as entered into the Register Selection
Code) of each individual asynchronous line (as entered in
bits 00-03 of the Secondary Selection Register). The four regis-
ters are described below. These bits are write-only.

15 Line Control Strobe (Read/Write—Self-Clearing)
The setting of this bit records the status of bits 09-14 into the
registers for the line specified in bits 00-03 of the Secondary Re-
gister Selection Register. This bit is self-clearing. It may be set
at the same time as the bits whose status it records, as its ac-
tion is delayed until the conclusion of the instruction cycle which
set it and the proper phasing of the DV11 internal clocks. This
bit is necessary due to "reads" in the PDP-11/20 being "read/
write" cycles and certain synchronization requirements associ-
ated with mode changes during clocking pulses. The bits marked
"Maintenance" should be written to zero for normal DV11 use.

**NOTE**
After setting this bit, do not change bits 00-03
of the Secondary Register Selection Register
until this bit has self-cleared indicating conclu-
sion of the strobe operation.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>Half Duplex (See bit 15)</td>
</tr>
</tbody>
</table>
|      | When this bit is set, the line is conditioned to operate in half-
duplex mode. The selected receiver is blinded during transmis-
sion of a character. When this bit is cleared, the line is condi-
tioned to operate in full-duplex mode. This bit is cleared by
Initialize. |
| 12   | Even Parity (See bit 15) |
|      | This bit specifies whether the line is to have even or odd parity
generated and checked. This bit has no effect unless Parity En-
able is set. This bit indicates odd parity when cleared and even
parity when set. This bit is cleared by Initialize. |
NOTE: Setting or clearing this bit does not affect operation of the line until the next time the program accesses the format register. The program should set this bit to the desired state and then access the format register.

13 Receiver Enable (See bit 15)
The PDP-11 program must set this bit before the receiver logic can assemble characters from the serial input line. When this bit is set, Receiver Active (Line State Bit 00) will subsequently set. This bit is cleared by Initialize.

NOTE: To shut down reception on a line, the program should clear Receiver Enable and then set Receiver Resynchronize.

14 Break (See bit 15)
When this bit is set, the line will be held in the spacing state (0) causing a break condition. The break condition may be timed by sending characters during the break interval, since these characters will never reach the EIA line. This bit is cleared by Initialize.

NOTE
The generation of a Transmitter Byte Count = 0 interrupt occurs when the last character of the message buffer is loaded into the UART transmitter. It is important to note that transmission is not completed when the interrupt is generated. Two more characters remain to be transmitted. One is in the UART transmitter shift register; the other is in the UART transmitter buffer register. Two null (all-0) characters should be loaded prior to setting the Break bit. In like manner, nulls should be used to time the Break signal so that no valid characters will be produced from the UART shift and buffer registers when the Break condition is terminated.
Bits   Description

11-12 Character Length (See bit 15)
These bits specify the character length (not counting start bit, stop bits, and parity bit if enabled) for the line.

<table>
<thead>
<tr>
<th>12</th>
<th>11</th>
<th>Character Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>5 bits</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>6 bits</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>7 bits</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>8 bits</td>
</tr>
</tbody>
</table>

13 Two Stop Bits (See bit 15)
This bit, when set, conditions the line transmitting 5, 6, 7, or 8 bit characters to transmit characters having two stop bits. One stop bit is sent when the bit is cleared.

14 Parity Enable (See bit 15)
When this bit is set, a parity bit is generated on transmission and checked and stripped on reception for the line. When this bit is cleared, no parity bit is generated, checked, or stripped.

The program must set the Even Parity bit to the desired value prior to accessing the Format Register. The program must set the Format Register to the desired state prior to setting the Receiver Enable or Transmitter Go.

```
  15  14  11  10  9
   1   1   1   1   0
   SPEED CODE
```

Bits   Description

14-11 Speed Code (See bit 15)
These four bits specify the speed of operation for the receiver and transmitter of the selected line.

<table>
<thead>
<tr>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>Baud Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>50</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>75</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>110</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>134.5</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>150</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>300</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>600</td>
</tr>
</tbody>
</table>

2-213
The program must set this register to the desired value prior to setting Receiver Enable or Transmitter Go.

** Maintenance Internal Mode (See bit 15)**

Normal operating mode is 0. This bit is cleared by Initialize.

**SECONDARY REGISTER SELECTION REGISTER—ADDRESS 775006 (775046, 775106, 775146)**

The bits in this register provide a path for the program to access the various locations in the DV11 RAM. The PDP-11 program can read or write these locations. The various locations can be considered as indirectly addressable registers.

Interrupts must be inhibited or the contents of this register saved between the setting of bits in this register and the reading or writing of the Secondary Register Access Register—Address X10. This register is byte-addressable.

The bit assignments of the Secondary Register Selection Register are as follows:
Bits      Description

00-03  Line Selection
        For each type of register selected by bits 08-11 below, there are
        16 registers, one per line. The setting of the Line Selection Bits
determines exactly which of these line registers is to be ad-
dressed. The Line Selection Bits are also used to select the line
to which the bits in the Line Control Register (X04) apply.

04-07  Unused

08-11  Register Selection
        These bits determine which type of register is addressed for the
        line number specified in bits 00-03.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>10 09 08</td>
</tr>
<tr>
<td></td>
<td>00 00 00 0</td>
</tr>
<tr>
<td></td>
<td>00 00 00 1</td>
</tr>
<tr>
<td></td>
<td>00 00 10 0</td>
</tr>
<tr>
<td></td>
<td>00 01 01 1</td>
</tr>
<tr>
<td></td>
<td>00 01 00 0</td>
</tr>
<tr>
<td></td>
<td>01 01 01 0</td>
</tr>
<tr>
<td></td>
<td>01 01 00 1</td>
</tr>
<tr>
<td></td>
<td>01 01 11 0</td>
</tr>
<tr>
<td></td>
<td>01 01 11 1</td>
</tr>
<tr>
<td></td>
<td>10 00 00 0</td>
</tr>
<tr>
<td></td>
<td>10 00 10 0</td>
</tr>
<tr>
<td></td>
<td>10 01 00 0</td>
</tr>
<tr>
<td></td>
<td>10 01 10 1</td>
</tr>
<tr>
<td></td>
<td>10 10 00 0</td>
</tr>
<tr>
<td></td>
<td>10 10 11 1</td>
</tr>
<tr>
<td></td>
<td>11 00 00 0</td>
</tr>
<tr>
<td></td>
<td>11 00 10 1</td>
</tr>
<tr>
<td></td>
<td>11 10 01 0</td>
</tr>
<tr>
<td></td>
<td>11 10 11 1</td>
</tr>
</tbody>
</table>

SECONDARY REGISTER ACCESS REGISTER—ADDRESS 775010
(775050, 775110, 775150)
This register should be loaded or read only after the appropriate bits of
the Secondary Register Selection Register have been conditioned to se-
lect the type of register and line number within that type. Since this register is essentially a "window" through which the program may access a large number of other registers, no specific bit assignment may be given. See the individual register bit assignment listings. A list of the registers accessible through this register follows. This register is word-addressable only.

These registers are not cleared by Initialize. The PDP-11 program must clear all of these registers before setting SCR00 (microprocessor go).

<table>
<thead>
<tr>
<th>Code</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>Transmitter Principal Current Address Secondary Register</td>
</tr>
<tr>
<td></td>
<td>This register contains 18-bit entries that will indicate, for each line's transmitter hardware, where in a core memory message table to obtain the next character to load into the transmitter associated with that line. Two additional bits are initially loaded from bits 04 and 05 of the System Control Register (X00), permitting 18-bit addressing capability. When the byte count associated with this current address reaches zero, an entry will be made in the NPR Status Silo and transmission will continue using the Transmitter Alternate Current Address, provided that the &quot;Transmitter Go&quot; bit in the Line State Secondary Register for this line is still set.</td>
</tr>
<tr>
<td>0001</td>
<td>Transmitter Principal Byte Count Secondary Register</td>
</tr>
<tr>
<td></td>
<td>This register contains a 15-bit word that is the 2's complement of the number of bytes (characters) remaining to be transmitted on this line. The 16th bit (bit 15) is used to indicate, when loaded clear, that the high byte of the Line Progress Register will control further action on this line when the principal byte count reaches zero. When a simple change to alternate byte count is desired, bit 15 should be set to one.</td>
</tr>
<tr>
<td>0010</td>
<td>Transmitter Alternate Current Address Secondary Register</td>
</tr>
<tr>
<td></td>
<td>This register has exactly the same function as the Transmitter Principal Current Address Secondary Register described above. When the byte count associated with this current address reaches zero, an entry will be made in the NPR Status Silo and transmission will continue using the Transmitter Principal Current Address, provided the &quot;Transmitter Go&quot; bit in the Line State Secondary Register for this line is still set.</td>
</tr>
<tr>
<td>0011</td>
<td>Transmitter Alternate Byte Count Secondary Register</td>
</tr>
<tr>
<td></td>
<td>This register contains a 15-bit word that is the 2's complement of the number of bytes (characters) remaining to be transmitted on this line. The 16th bit (bit 15) is used to indicate, when loaded clear, that the high byte of the Line Progress Register will control action on this line when the alternate byte count is desired, bit 15 should be set to one.</td>
</tr>
</tbody>
</table>
count reaches zero. When a simple change to principal byte count is desired, bit 15 should be set to one.

NOTE
The program can tell the DV11 whether to start from principal or alternate tables by loading the appropriate bits in the Line State Secondary Register.

0100 Receiver Current Address Secondary Register
This register contains 18-bit entries that will indicate, for each line's receiver hardware, where in a core memory message table to store the next character received on this line. Two additional bits are initially loaded from bits 04 and 05 of the System Control Register (X00).

0101 Receiver Byte Count Secondary Register
This register contains a 15-bit word that is the 2's complement of the number of bytes (characters) remaining to be received on this line. The 16th bit (bit 15) is used to indicate, when loaded clear, that the high byte of the Line State Register will control action on this line when the receiver byte count reaches zero.

When the in-core message table for reception on this line has been filled with received characters, the byte count will have been up-counted to zero. An entry will then be made in the Receiver Interrupt Character Register, a receiver interrupt request will be generated, and the action of the microprocessor in retrieving characters from the received character storage silo will stop. Refer to Receiver Interrupt Character Register error code 1000 for further details.

0110 Transmitter Accumulated Block Check Secondary Register
This register contains an up-to-date calculation of the block check character associated with transmission on each line. The type of polynomial used for each line is specified in the Line Protocol Parameters Secondary Register (1010). Characters to be included are specified by bit 03 of the control bytes obtained from the core transmission control tables during the NPR transmission of characters on this line if a character-oriented protocol such as BISYNC is being used. If a byte-count-oriented protocol such as DDCMP is being used and the transmitter mode is 0, all characters are included. The contents of this register may be checked at any time by the program. The program may also write into this register; this register can be cleared by writing zeros into it. (The microprocessor will do this automatically when the BCC is transmitted.) The contents of this register are sent out over the line as two 8-bit bytes (low order
8 bits first), except if LRC-8 is the selected protocol, in which case only one byte is sent.

**NOTE**
The DV11 calculates CRC-16 and CRC/CCITT on a byte-at-a-time basis (parallel); thus the character length must be eight bits if these block checks are to be used. LRC may be used for shorter characters.

0111 Receiver Accumulated Block Check Secondary Register
This register contains an up-to-date calculation of the block check character associated with reception on each line. The type of polynomial used for each line is specified in the Line Protocol Parameters Secondary Register (1010). Characters to be included are specified by bit 03 of control bytes withdrawn from the receiver control byte tables if a character-oriented protocol, such as BISYNC, is being used. If a byte-count-oriented protocol, such as DDCMP, is being used and the receiver mode is 0, all characters (except leading syncs on synchronous lines which can be stripped) are included. The contents of this register may be checked at any time by the program. The program may also write into this register; this register can be cleared by writing zeros into it. The program must do this after it has checked the block check at the end of the message as the microprocessor does not do this. (This would only be necessary if the block check were not zero—an error condition in most protocols.)

1000 Transmitter Control Table Base Address Secondary Register
This register contains an 18-bit word that indicates the starting address of the transmitter control table for this line. Extended address bits are initially loaded from bits 04 and 05 of the System Control Register (SCR). This address will have the character to be transmitted (with higher order mode bits appended) added to it by the transmitter hardware to obtain a byte address to which the NPR control hardware will go to obtain a control byte. The control byte will instruct the DV11 transmitter what to do with this particular character—whether to include it in the BCC, etc. If all lines in the DV11 are using the same protocol, the program could set all 16 Transmitter Control Table Base Addresses to the same value. In addition, if the protocol permits, the same base addresses could be used for both the transmit control table and for the receive control table.
1010 Line Protocol Parameters Register

This register contains information concerning the protocol to be executed on this line. This register must be initially loaded by the PDP-11 program before reception or transmission begins on this line.

The bit assignments are as follows:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Idle Mark on Both Byte Counts Zero (Synchronous Lines Only)</td>
</tr>
</tbody>
</table>

When this bit is set, the microprocessor will condition the synchronous transmitter on this line to idle MARK when both byte counts reach zero. If the bit is not set, SYNC will be idled. It is anticipated that this feature will be used in half-duplex systems wherein the PDP-11 program will set this bit immediately after loading the last byte count.

The setting of this bit is immaterial on asynchronous lines. MARK is always idled on asynchronous lines.

| 01   | Strip Leading Sync (Synchronous Lines Only) |

When this bit is set, all sync characters received between the time a line goes "active" and the time the first non-sync character arrives will be automatically stripped from the received message. Once a non-sync arrives, this feature is disabled until the line is resynchronized by the issuance of a Receiver Resynchronize command (see Line State Register, bit 01).

The program should not set this bit on asynchronous lines.

| 02   | Reserved |
| 03-04| Block Check Type |

These bits are conditioned by the PDP-11 program to indicate what type of block check calculation is to be done for transmissions and receptions on this line.

| 04 03 | 0 0 | LRC-8 (XOR) |
| 0 1   | CRC-16 \(X^{16} + X^{15} + X^2 + 1\) |
| 1 0   | Unused-16 |
| 1 1   | CRC/CITT \(X^{16} + X^{12} + X^5 + 1\) |

2-219
Bits | Function
---|---
05 | **DDCMP Receive**

If this bit is set and reception is in mode 0, the received character will be processed without reference to a control byte. A control byte calling an inclusion of all characters in the BCC and storage of all characters (excluding syncs stripped by bit 01 above) will be assumed. This bit is intended for use with byte-count-oriented protocols.

06 | **DDCMP Transmit**

If this bit is set and transmission is in mode 0, the transmitted character will be processed without reference to a control byte. A control byte calling for inclusion of all characters in the BCC will be assumed. This bit is intended for use with byte-count-oriented protocols.

07 | **Reserved**

08-15 | **Data Link Escape Character**

In the process of transmitting on a line, the microprocessor fetches control bytes from core indicating what special action, if any, is applicable to the transmission of that character on that line. One of the possibilities is the necessity of transmitting a Data Link Escape Character before transmitting the actual character. The Data Link Escape Character used is retrieved by the microprocessor from the high byte of this secondary register.

1011 | **Line State Register**

This register is a scorecard with which the microprocessor keeps track of what it is doing with respect to the special actions required of it in executing various line protocols. The bit assignments are as follows:

| Bits | Function |
---|---|
00 | **Receiver Active (set and cleared by microprocessor).**

This bit is set when an enabled line (LPR 12 set) has satisfied the synchronization conditions. This
<table>
<thead>
<tr>
<th>Bits</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>Receiver Resynchronize (set by the PDP-11 program and cleared by microprocessor). This bit is set when the PDP-11 program desires to resynchronize a synchronous line or when it has cleared Receiver Enable and is turning off reception on a line. The microprocessor, upon finding this bit set, will clear Receiver Active, clear this bit, and issue a resync pulse to the selected receiver. The microprocessor will also insert a special flag character into the silo, and set bit 07 of the Line Progress Register indicating that the special resynchronization character is in the silo.</td>
</tr>
<tr>
<td>02</td>
<td>Transmitter Go (set by PDP-11 program and cleared by microprocessor). The PDP-11 program will set this bit whenever it has prepared a message for transmission and desires that the DV11 transmit it. The microprocessor will clear this bit whenever Transmitter NXM sets, Transmitter MPE sets, or both byte counts associated with this line are zero. The PDP-11 program may clear this bit if it is desired that a transmission be aborted.</td>
</tr>
<tr>
<td>03</td>
<td>Transmitter Underrun (set by microprocessor and cleared by PDP-11 program). This bit is set if the microprocessor finds, upon loading a character for transmission, that a synchronous transmitter is exhibiting a “Data Not Available” flag. The setting of this bit does not generate an interrupt or clear any other bit; it is for the programmer’s information only. When the bit has been read by the program, the program should clear it. This bit will never be set on an asynchronous line.</td>
</tr>
<tr>
<td>04</td>
<td>Transmitter NXM (set by microprocessor and cleared by PDP-11 program). This bit sets whenever a microprocessor transmitter service routine encounters an NXM condition. The</td>
</tr>
<tr>
<td>Bits</td>
<td>Function</td>
</tr>
<tr>
<td>------</td>
<td>----------</td>
</tr>
<tr>
<td>05</td>
<td>Transmitter MPE</td>
</tr>
<tr>
<td></td>
<td>Same description as Transmitter NXM, but a Memory Parity Error occurred rather than an NXM.</td>
</tr>
<tr>
<td>06</td>
<td>Sync Strip On (set and cleared by microprocessor).</td>
</tr>
<tr>
<td></td>
<td>This bit sets whenever Receiver Active sets on a synchronous line whose Line Protocol Parameters bit 01 (Strip Leading Sync) is set. This bit clears whenever the first non-SYNC character arrives on that line. This bit is for use by the microprocessor only.</td>
</tr>
<tr>
<td>07</td>
<td>Use Alternate Tables (set and cleared by microprocessor or by PDP-11 program).</td>
</tr>
<tr>
<td></td>
<td>Before setting Transmitter Go, the PDP-11 program should condition this bit to indicate to the microprocessor whether to start the transmission from the principal or from the alternate tables. When a byte count runs out, the microprocessor will switch to the other current address and byte count. If the other byte count is also zero, this bit will remain in that second state and “go” will be cleared.</td>
</tr>
<tr>
<td>08-09</td>
<td>Unused.</td>
</tr>
<tr>
<td>10</td>
<td>Expect BCC1 Next on Byte Count Run-out.</td>
</tr>
<tr>
<td></td>
<td>The PDP-11 program may load this bit to indicate to the DV11 that it should expect the first eight bits of the block check character when a “marked” reception byte count reaches zero. When the DV11 processes the last character and the “marked” byte count thus reaches zero, the microprocessor will set Line Progress Register bit 05 to tell the DV11 logic that the BCC is next. This information will be used when the DV11 services the next character that arrives on this line.</td>
</tr>
<tr>
<td>11-12</td>
<td>Unused.</td>
</tr>
<tr>
<td>13-15</td>
<td>Receiver Next Mode on Byte Count Run-out.</td>
</tr>
</tbody>
</table>
The PDP-11 program may load these bits with the receiver mode to which it desires the DV11 hardware to go when a "marked" reception byte count reaches zero.

1100 Transmitter Mode Bits Register
This register contains three bits (00-02) which indicate the "mode" of transmission on this line. These three bits determine which of the up to eight possible control tables will be used for transmission on this line. The transmitter logic appends these bits onto the high-order end of a copy of the character to be transmitted and uses the resulting 11-bit character as an offset from the transmitter control table base address to obtain a control byte from core. The control byte contains special instructions with regard to the character that is about to be transmitted.

1101 Receiver Mode Bits Register
This register contains three bits (00-02) which indicate the "mode" of reception on this line. Specifically, these bits determine which of the up to eight possible control tables will be used for reception on this line. Refer to the section entitled "Control Tables."

1110 Line Progress Register
The bit assignments for the Line Progress Secondary Register are as follows:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Send BCC1 Next</td>
</tr>
<tr>
<td></td>
<td>This bit is set by the microprocessor when it runs out a &quot;marked&quot; transmission byte count (bit 15 loaded as zero) (typical use: DDCMP) or encounters a transmitter control byte with bit 02 (send BCC next) set, typically ITB, ETB, or ETX in BISYNC. It is cleared by the microprocessor when LRC is the selected block check and has been loaded for transmission, or when the BCC1 has been loaded for transmission.</td>
</tr>
<tr>
<td>01</td>
<td>Send BCC2 Next</td>
</tr>
<tr>
<td></td>
<td>This bit is set by the microprocessor when the BCC1 has been loaded for transmission. This bit is cleared by the microprocessor when the BCC2 is loaded for transmission.</td>
</tr>
</tbody>
</table>
Bits | Function
---|---
02 | DLE Sending In Progress
This bit is set by the microprocessor when it has just loaded a DLE for transmission in response to seizure of a control byte that says to prefix a DLE. This bit is used by the microprocessor to prevent stuffing DLE characters continuously. This bit is cleared by the microprocessor when the DLE has been sent.

03-04 | Unused.

05 | Expect BCC1 Next
This bit is set by the microprocessor when it runs out a “marked” reception byte count (bit 15 loaded as zero) (typical use: DDCMP) or encounters a receiver control byte with bit 02 (expect BCC next) set, typically ITB, ETB, or ETX in BISYNC. This bit is cleared by the microprocessor when LRC is the selected block check and has been received, or when the BCC1 has been received.

06 | Expect BCC2 Next
This bit is set by the microprocessor when the BCC1 has been received. This bit is cleared by the microprocessor when the BCC2 has been received.

07 | Resynchronization Flag Character Not Found (set and cleared by microprocessor).
This bit is set when the microprocessor processes a resynchronization request for this line. It is cleared when the microprocessor finds the flag character that it inserted in the silo at the time that resynchronization was requested. Characters retrieved from the silo for this line while this bit is set are discarded.

08-09 | Unused.

10 | Send BCC1 Next on Marked Byte Count Run-out
The PDP-11 program may load this bit to indicate to the DV11 that it should send the first eight bits of the block check character when a “marked” transmitter byte count reaches zero. If this bit is set, the microprocessor in the DV11 will, upon reaching zero, set Line Progress Register bit 00 (see above).
### DV11

<table>
<thead>
<tr>
<th>Bits</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>11-12</td>
<td>Unused.</td>
</tr>
<tr>
<td>13-15</td>
<td>Transmitter Next Mode on Marked Byte Count Run-out</td>
</tr>
</tbody>
</table>

The PDP-11 program may load these bits with the transmitter mode to which it desires the DV11 hardware to go when a "marked" transmitter byte count reaches zero.

1111 Receiver Control Byte Storage Register

This register contains a copy of the control byte fetched from the receiver control table by the DV11. When a control byte is fetched that has bit 00 (generate interrupt) set, a copy of that control byte (but with bit 00 cleared) is stored here; the interrupt-causing character and its line number are moved to the Receiver Interrupt Character Register; and an interrupt request is generated. The PDP-11 program may merely take note of the arrival of this character and set System Control Register bit 08 to direct the microprocessor to resume processing the character. The microprocessor will use this copy of the control byte for that processing. The PDP-11 program can alter the contents of this register before setting SCR08 if it desires to change the character processing from that originally dictated by the control byte.

In the case of receiver interrupts generated by causes other than the fetching of a control byte with bit 00 (generate interrupt) set, a special control byte arranged for character discard, no BCC inclusion, no BCC expectation, and same mode as control byte last fetched for reception on this line, is placed in this register by the microprocessor before conditioning the Receiver Interrupt Character Register and generating the receiver interrupt request.

**SPECIAL FUNCTIONS REGISTER—ADDRESS 775012**

(775052, 775112, 775152)

Reserved for Maintenance. Various bits may appear here during normal operations. This register is word-addressable.

**NPR STATUS REGISTER—ADDRESS 775014 (775054, 775114, 775154)**

This register is a 64-entry silo-type register in that it is read once, and then a new entry "falls" into the register if additional "entries" exist at the time that the read of this register is completed.

This register reports various interrupt-causing conditions associated with the transmitter NPR hardware. Interrupt conditions related to various
transmitter NPR operations are stacked in a first-in/first-out storage buffer along with the line number being serviced when this condition occurred. As soon as the program has finished reading this register once, a new entry is cycled into the register in place of the former entry. The interrupt is SCR 15 (NPR Status Interrupt). This register is read-only and is not cleared by Initialize, except for bit 15 which is cleared by Initialize.

![Diagram of SCR 15](image)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-03</td>
<td>Line Number</td>
</tr>
<tr>
<td></td>
<td>These bits indicate which line was being serviced when the interrupt condition developed. The format of these bits is the same as bits 00-03 of the Secondary Register Selection Register (SRSR) so that the program can load these bits into the SRSR and read the appropriate current address or byte count.</td>
</tr>
<tr>
<td>04-07</td>
<td>Unused</td>
</tr>
<tr>
<td>08-11</td>
<td>Interrupt Condition</td>
</tr>
<tr>
<td></td>
<td>These bits indicate the type of interrupt condition which occurred. The hardware is designed so that simultaneous occurrences on the same line create separate entries (Example: non-existent memory and byte count zero both occur). Note that the condition codes are the addresses of the secondary registers which apply.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Code</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>Transmitter Principal Current Address sent NPR hardware to a nonexistent memory location (NXM).</td>
</tr>
<tr>
<td>0001</td>
<td>Transmitter Principal Byte Count = 0.</td>
</tr>
<tr>
<td>0010</td>
<td>Transmitter Alternate Current Address sent NPR hardware to a nonexistent memory location.</td>
</tr>
<tr>
<td>0011</td>
<td>Transmitter Alternate Byte Count = 0.</td>
</tr>
<tr>
<td>1000</td>
<td>Transmitter Control Table Base Address—fetched control byte produced NXM or a memory parity error. The program should examine the Line State Secondary Register for further details.</td>
</tr>
<tr>
<td>12-14</td>
<td>Unused</td>
</tr>
</tbody>
</table>
**Bits** | **Description**
--- | ---
15 | Entry Present
When set, this bit indicates that bits 00-11 contain a valid entry. Reading the register or generating Initialize clears this bit. It resets when another status report entry reaches the “bottom” of the silo and can be read in bits 00-11. Bits 00-11 are meaningless unless this bit (15) is set.

**RESERVED REGISTER—ADDRESS 775016 (775056, 775116, 775156)**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-15</td>
<td>Reserved; word-addressable</td>
</tr>
</tbody>
</table>

**CONTROL BYTE FORMATS**
The DV11 achieves its high throughput and generalized operating capabilities by having both the transmitter and the receiver character-handling apparatus perform NPR cycles. The NPR cycles access byte tables in PDP-11 core to determine the next step to take with regard to the particular character being processed. The bit assignments in the control bytes are arranged such that the same control bytes may be used for both transmission and reception if the communications protocol being used progresses from mode to mode in a symmetrical fashion on both transmit and receive and provided that the same characters would be included in the Block Check Character in both transmission and reception.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Transmitter Control Byte Function</th>
<th>Receiver Control Byte Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>05-07</td>
<td>Next Mode</td>
<td>Next Mode</td>
</tr>
<tr>
<td></td>
<td>Determines next transmission mode used on this line.</td>
<td>Determines next reception mode used on this line.</td>
</tr>
<tr>
<td>04</td>
<td>Reserved</td>
<td>Store/Discard</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Determines whether this character is stored in message table or is discarded.</td>
</tr>
<tr>
<td>Bits</td>
<td>Transmitter Control Byte Function</td>
<td>Receiver Control Byte Function</td>
</tr>
<tr>
<td>------</td>
<td>----------------------------------</td>
<td>--------------------------------</td>
</tr>
<tr>
<td>03</td>
<td>Include in BCC Yes/No</td>
<td>Include in BCC Yes/No</td>
</tr>
<tr>
<td></td>
<td>Determines whether or not this character will be included in the BCC being accumulated for this line.</td>
<td>Determines whether or not this character will be included in the BCC being accumulated for this line.</td>
</tr>
<tr>
<td>02</td>
<td>Send BCC Next</td>
<td>Expect BCC Next</td>
</tr>
<tr>
<td></td>
<td>Tells transmitter logic to send the 16-bit BCC after the character presently being handled (8-bit if LRC selected.)</td>
<td>Tells receiver logic to expect the 16-bit BCC after the character presently being handled (8-bit if LRC selected.)</td>
</tr>
<tr>
<td>01</td>
<td>Send Data Link Escape Next</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>Tells transmitter logic to send Data Link Escape character from Secondary Register 1010 before sending the character presently being handled.</td>
<td></td>
</tr>
<tr>
<td>00</td>
<td>Reserved</td>
<td>Generate an Interrupt</td>
</tr>
<tr>
<td></td>
<td>The setting of this bit causes the character presently being processed to generate an interrupt. The microprocessor moves that character to the Receiver Interrupt Character Register and generates an interrupt request.</td>
<td></td>
</tr>
</tbody>
</table>

**PROGRAMMABLE MODEM CONTROL DEVICE REGISTERS**

The two programmable modem control device registers and their specific bit assignments are listed in the following paragraphs.

**CONTROL STATUS REGISTER (CSR)—ADDRESS 775020**

(775060, 775120, 775160)
Bits     Status     Description
00-03     LINE #     The LINE # bits are the binary addresses for
                 the modem control's 16 lines (0-15) as follows:

                 | Bit | 3 | 2 | 1 | 0 | Line |
                 |-----|---|---|---|---|------|
                 | 0   | 0 | 0 | 0 | 0 | 0    |
                 | 0   | 0 | 0 | 1 | 1 |      |
                 |     |   |   |   |   |      |
                 |     |   |   |   |   |      |
                 | 1   | 1 | 1 | 1 | 15|      |

If the Scan is cleared by INITIALIZE or CLR SCAN, the Line # Register will settle in 16\mu s ±10%. When settled, the Line # Register will be set to Line #0(0000).

**NOTE**

When the Scan is enabled (or STEP), the next line to be tested will always be Line # +1. These bits are read/write and are cleared by INITIALIZE and by CLR SCAN.

04 BUSY     BUSY provides a program indicator that is set to 1 when the Scan is cycling. This bit is particularly useful to determine when a CLR SCAN (bit 11) has completed the task of cycling 0's into the Scanner's memory elements.

In addition, this bit must be tested for 0 if SCAN ENABLE was turned off preparatory to changing the Line #.

In Interrupt Mode, this procedure guarantees that detected transitions are serviced before the Line # is changed. (If functioning with interrupts OFF, then DONE should be tested after BUSY is found to be 0.)

05 SCAN EN   The SCAN ENABLE flip-flop allows the scan to "free run," testing all lines sequentially if the DONE flip-flop is cleared.

When the SCAN EN flip-flop is set to 1 and DONE is 0, a ring counter is allowed to cycle in the following order (from Rest):

1. Increment line counter.
<table>
<thead>
<tr>
<th>Bits</th>
<th>Status</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>06</td>
<td>INTER EN</td>
<td>If set to 1, Interrupt Enable allows DONE to cause an interrupt on priority four. This bit is read/write and cleared by INITIALIZE and CLR SCAN.</td>
</tr>
<tr>
<td>07</td>
<td>DONE</td>
<td>The DONE flag, when set to 1, indicates that the hardware Scan has detected a transition on CARRIER, DATA SET READY/SEC RX, CS, or the RING modem Status leads. Additionally, DONE freezes the SCAN which makes available to the programmer:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1. The Line # that caused the interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. The state of the flags (four bits).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. Modem Status (eight bits).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>This bit is read/write and cleared by INITIALIZE and CLR SCAN.</td>
</tr>
<tr>
<td>08</td>
<td>STEP</td>
<td>STEP, when set to 1, causes the Scan to increment the Line # and test that line for interrupts causing transitions. STEP can be used in place of SCAN EN, but care should be exercised that the Scan rate is great enough (milliseconds) so that double carrier transitions will be detected. Additionally, DONE does not inhibit STEP. A STEP requires 1.2μs ± 10% to execute. This bit is write 1’s only.</td>
</tr>
<tr>
<td>09</td>
<td>MAINT MODE</td>
<td>When the MAINT MODE flip-flop is set to 1, it conditions the Scan Input (RING, CLEAR TO SEND, CARRIER, and DATA SET READY/SEC RX) to a 1 or ON state. Utilizing STEP or SCAN EN with MAINT MODE exercises 100 percent of</td>
</tr>
<tr>
<td>Bits</td>
<td>Status</td>
<td>Description</td>
</tr>
<tr>
<td>------</td>
<td>--------------</td>
<td>-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>10</td>
<td>CLEAR MUX</td>
<td>CLEAR MUX clears the REQUEST TO SEND, TERMINAL READY, SEC TX, and LINE EN flip-flops for all lines, when this bit is set to 1. This bit is write 1's only.</td>
</tr>
<tr>
<td>11</td>
<td>CLEAR SCAN</td>
<td>CLEAR SCAN clears all active functions (Line #, SCAN EN, etc.) and the memory logic, when this bit is set to 1. The memory logic requires 18.8 µs ± 10% to cycle a CLEAR through the memory locations. This function is especially useful if the programmer requires knowledge of the ON states of CARRIER, CLEAR TO SEND, RING and SEC RX. When the Scan is enabled (or STEP) following a CLR SCAN, an interrupt will occur for all ON states as they will appear (to the logic) as OFF-to-ON transitions.</td>
</tr>
<tr>
<td>12</td>
<td>DSF/SEC RX</td>
<td>The DATA SET READY/SEC RX flag is 1 if an ON-to-OFF or an OFF-to-ON transition has occurred on the Data Set Ready modem lead of a synchronous line or the Secondary Receive modem lead of an asynchronous line. This bit is not valid if the program has changed the Line # and the Scan has not cycled for one or more lines. This bit is read-only and presents 0 when INITIALIZED or CLR SCAN.</td>
</tr>
<tr>
<td>13</td>
<td>CS</td>
<td>The CLEAR TO SEND flag is 1 if an ON-to-OFF or OFF-to-ON transition has occurred on this modem lead. This bit is not valid if the program has changed the Line # and the Scan has not cycled for one or more lines. This bit is read-only and presents 0 when INITIALIZED or CLR SCAN.</td>
</tr>
<tr>
<td>14</td>
<td>CO</td>
<td>The CARRIER flag is 1 if an ON-to-OFF or OFF-to-ON transition has occurred on this modem lead. This bit is not valid if the program has changed the Line # and the Scan has not cycled for one or more lines. This bit is read-only and presents 0 when INITIALIZED and CLR SCAN.</td>
</tr>
<tr>
<td>Bits</td>
<td>Status</td>
<td>Description</td>
</tr>
<tr>
<td>------</td>
<td>--------</td>
<td>-------------</td>
</tr>
<tr>
<td>15</td>
<td>RING</td>
<td>The RING flag is 1 if an OFF-to-ON transition has occurred on this modem lead. This bit is not valid if the program has changed the Line # and the Scan has not cycled for one or more lines. This bit is read-only and presents 0 when INITIALIZED and CLR SCAN.</td>
</tr>
</tbody>
</table>

**LINE STATUS REGISTER (LSR)—ADDRESS 775022**  
(775062, 775122, 775162)

![LSR Diagram]

00 **LINE EN**  
The LINE ENABLE flip-flop, when asserted, enables RING, CO, CS, and DATA SET READY/SEC RX to be sampled (line status) by the program, and to be tested for transitions.  
This bit is read/write and is cleared by INITIALIZ and CLEAR MUX.

01 **TERM RDY**  
Controls switching of the data communications equipment to the communication channel (via modem).

Auto-Dial and Manual Call origination: Maintains the established call.

Auto-Answer: Allows “handshaking” in response to a RING signal.

This bit is read/write and is cleared by INITIALIZ and CLEAR MUX.

02 **RS**  
When REQUEST TO SEND is set to 1, it conditions the modem for transmit if the communications channel has been established (switched network). This bit is read/write and is cleared by INITIALIZ and CLEAR MUX.

03 **NS/SEC TX**  
On synchronous lines, this bit controls the New Sync (201) modem control lead. When this bit is set, a high is presented to the New Sync (201) modem control lead.
Bits | Status | Description
---|---|---
04 | DSR/SEC RX | On asynchronous lines, this bit controls the Secondary Transmit modem control lead. When this bit is set, a mark is presented to the Secondary Transmit modem control lead.

This bit is read/write and is cleared by INITIALIZE and CLEAR MUX.

On synchronous lines, this bit reflects the state of the modem's Data Set Ready lead. When the state of the modem's Data Set Ready lead is a high, this bit is a 1.

On asynchronous lines, this bit reflects the state of the modem's Secondary Receive lead. When the Secondary Receive lead is in the marking state, this bit is a 1.

This bit is inhibited when the LINE EN flip-flop is 0. This bit is read-only.

05 | CS | This bit reflects the current state of the modem CLEAR TO SEND lead. An ON indicates that the modem is ready to transmit data. This lead is most often the result of the REQUEST TO SEND lead. The CS bit is inhibited when the LINE EN flip-flop is 0. This bit is read-only.

06 | CO | This bit reflects the current state of the modem carrier detect lead. An OFF indicates that the received signal is unsuitable for demodulation. The CO bit is inhibited when the LINE EN flip-flop is 0. This bit is read-only.

07 | RING | Set to 1 whenever the ring line from the modem selected by bits 00-03 of the CSR is on, provided that the line enable bit for that modem has been set.

**NOTE**
The Line Status Register bits 04-07 are inhibited when LINE EN is 0.

**SPECIFICATIONS**

**System Addresses**
The DV11 uses the same address space as the DM11-A. The first DV11 in a system would be at 775000; the next at 775040; then 775100; and finally, 775140. If there are DM11-As in the system already, the first DV11 would be at 775040. The DV11 data handling and modem control use a total of ten registers.
Interrupt Vectors
Each DV11 requires three interrupt vectors—two for the data handling section and one for the modem control. The interrupt vectors are in the floating vector space that starts at 300. The DV11 modem control follows the DMA11-BB which follows the DN11. The DV11 data handling section follows the DUP11 which in turn follows the DU11.

Timing Considerations
The modem control timing considerations consist of scan control and CLR SCAN operations. Scan control through the CSR allows the scan either to run free (SCAN EN) or to be sequentially stepped through the line counter line-by-line (STEP bit of CSR). The read/write cycles of the modem control scan logic force the program to wait, after issuing CLR SCAN, until it has cycled through the memories. Also, the scan’s read/write cycles prevent halting the scan and changing the line number with one machine cycle.

Programs should not spin on flags in the DV11 secondary registers using loops less than 30 (octal) instructions; to do so may interfere with DV11 RAM microprocessor/UNIBUS access interlocks.

Order Numbers
DV11-AA Double System unit contains all DV11 logic except the line cards and distribution panels. A total of two DV11-BA s, DV11-BB s, and DV11-BC s may be used with a DV11-AA. No lines are implemented.

DV11-BA Line cards and distribution panel for eight synchronous lines.

DV11-BB Line cards and distribution panel for eight asynchronous lines.

DV11-BC Line cards and distribution panel for four asynchronous lines and four synchronous lines.

Bus Loads
Two bus loads.

Power Consumption

<table>
<thead>
<tr>
<th></th>
<th>+5 volts</th>
<th>−15 volts</th>
<th>+15 volts</th>
</tr>
</thead>
<tbody>
<tr>
<td>DV11-AA</td>
<td>12.3 amps</td>
<td>1.0 amps</td>
<td>0.6 amps</td>
</tr>
<tr>
<td>DV11-BA</td>
<td>2.6</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>DV11-BB</td>
<td>4.0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>DV11-BC</td>
<td>3.3</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Environmental
+10° to +50°C. with a relative humidity of 20% to 95%.

Space Requirements
DV11-AA: two system units (SU’s)
DV11-BA: 5 1/4 inches of cabinet space (SM PAN)
DV11-BB: 5 1/4 inches of cabinet space (SM PAN)
DV11-BC: 5 1/4 inches of cabinet space (SM PAN)
Cables
Order BC05D-25 modem cables. 7.6m 25-conductor cable terminated in cinch DB25S socket at one end and cinch DB25P plug at the other.

Internal Clock (Synchronous Lines Only)
The DV11 synchronous line units include an internal clock which can be used when two PDP-11s are connected locally without modems. It is also useful for diagnostic purposes. The clock speed can be set at 1200, 2400, 4800, or 9600 baud, switch-selectable for each 4-line group (0-3, 4-7, 8-11, 12-15).
DZ11

DZ11 ASYMMRONOUS MULTIPLEXER

HIGHLIGHTS
- Low cost 8 and 16 line multiplexed asynchronous interface for connecting UNIBUS PDP-11's to terminals or other computers
- Local operation at speeds up to 9600 baud for maximum responsiveness of CRT terminals
- Data set control for full duplex dial up remote operation
- Programmable line speeds and character formats on a per line basis for flexibility and ease of configuration
- Silo buffered input transfers for reduced interrupt overhead and improved latency, program interrupt output transfers for low cost
- Versions available for EIA/CCITT or 20 mA signalling
- Compact, single PC board, 8 line modularity
- 16 line cable distribution panel conserves cabinet space

INTRODUCTION
The DZ11 is a multiplexed, program controlled asynchronous interface that connects a PDP-11 processor to 8 or 16 asynchronous serial lines. It is ideally suited to applications needing a low cost method of connecting multiple local or remote terminals at moderate throughput. DZ11's can be used with PDP-11 systems in a variety of applications including communications processing, time sharing, transaction processing or real-time processing. The PDP-11 may be a stand-alone computer system, a front-end or remote concentrator to a larger system, or part of a network of computers performing distributed processing.

Local Operation
Applications needing a few terminals benefit from the small size and 8 line modularity of the DZ11, while applications needing more terminals on a single PDP-11 system can use multiple DZ11's. Up to 128 asynchronous lines can be connected to a PDP-11 system, with the number in a particular case determined by the system software, hardware configuration, and application. The DZ11 can also be used in applications requiring asynchronous links between computer systems. Local operation to terminals or computers is possible at speeds up to 9600 baud. The higher speeds will enhance the responsiveness of CRT terminals. Local operation can use either EIA RS-232-C/CCITT V.24 interfaces or 20 mA current loop signalling depending on the DZ11 model selected. Local operation using EIA interfaces is particularly convenient, because it permits a single DZ11 to serve a mixture of local and remote devices.

Remote Operation—Dial-up
Remote operation using the public switched telephone network is possible with DZ11 models offering EIA RS-232-C/CCITT V.24 interfaces. These DZ11 models contain sufficient data-set control as a standard feature to permit dial up (auto-answer) operation with modems capable of full-duplex operation (such as the Bell models 103 or 113 or equiv-
The speed of operation will be limited by the modem and communications line typically to 300 Baud (Bell 103 or 113). Where dial out (auto-dial) operation is required, the DZ11 can be used together with the DN11 auto dial interface and appropriate automatic calling unit. The standard DZ11 data set control does not support half-duplex dial up operation or the secondary transmit and receive channels available with some modems (such as Bell models 202).

Remote Operation—Leased Lines
Remote operation over private lines is possible with DZ11 models offering EIA RS-232-C/CCITT V.24 interfaces. These models are suitable for full-duplex point-to-point operation or full-duplex multipoint operation as a control (master) station. In some applications, a DZ11 can also be used as a multipoint tributary (slave) station or in half-duplex point-to-point operation by connecting modems to the DZ11 with specially wired cables. The standard DZ11 data-set control will not support half duplex applications requiring secondary channels. Remote operation using the Bell model 202 modem can be supported for private line operation with the above restrictions.

MODELS AVAILABLE
DZ11 models are available with EIA/CCITT or current loop interfaces in 8 or 16 line configurations. An 8 line configuration consists of a single hex-sized printed-circuit board module and a 5⅛” high cable distribution panel. The printed circuit board module plugs into any hex-sized small peripheral controller (SPC) slot in CPU back planes or expansion system units. The module contains all the logic required to control and interface 8 lines. The cable distribution panel is connected to the module by a fifteen foot ribbon cable and can mount in the same cabinet or in a nearby cabinet. The cable distribution panel contains connectors terminating 16 lines. Cables from the panel to modems or local devices must be ordered separately.

A 16 line DZ11 configuration consists of two printed circuit board modules connected by two fifteen-foot ribbon cables to a single distribution panel. The two hex SPC slots required do not have to be adjacent. A 16 line DZ11 configuration appears to the programmer as two 8 line multiplexors. A 16 line configuration saves cabinet space and cost. It is possible to field expand an 8 line configuration to 16 lines by adding an additional interface module and ribbon cable.

The DZ11-A is an 8 line configuration with EIA RS-232-C/CCITT V.24 interfaces. It can be expanded to 16 lines (all EIA/CCITT) by adding a DZ11-B. The DZ11-E is a 16 line EIA/CCITT configuration. The distribution panel supplied with EIA configurations has 16 cinch DB25P connectors for connection to modems or local devices.

The DZ11-C is an 8 line configuration with 20 ma current loop interfaces. It can be expanded to 16 lines (all 20 ma) by adding a DZ11-D. The DZ11-F is a 16 line 20 ma configuration. The distribution panel supplied with 20 ma configurations has 16 four-screw terminal strips for connection to local devices.
OPERATION

GENERAL
The DZ11 is a buffered, multiplexed, interface between asynchronous serial communications channels and the PDP-11 UNIBUS. Modularity is on an 8 channel basis. The DZ11 performs serial-to-parallel and parallel-to-serial conversion of serial start-stop data with double character buffered MOS/LSI circuits called UART’s (Universal Asynchronous Receiver Transmitters). These circuits provide the logic necessary to double buffer characters in and out, to serialize-deserialize data, to provide selection of character length and stop code configuration under program control, and to present status information about the UART and the characters. MOS/LSI circuits generate separate timing signals for each line from a common crystal oscillator permitting the speed of operation of each line to be individually controlled by the program. A 64-character first in/first out buffer is provided in the hardware (for each 8 lines) to hold characters as they are received. DZ11 models with EIA RS-232-C/CCITT V.24 interfaces include data set control logic permitting the program to sense the state of two data set control signals and to control the state of one data set control signal for each line.

RECEIVER
The receiver section performs serial-to-parallel conversion of 5-, 6-, 7-, or 8-level codes. The duration of the stop element may be 1 or 11/2 bit times for characters with 5 data bits and 1 or 2 bit times for characters with 6, 7, or 8 data bits. The receiver can check for even or odd character parity or alternatively no parity checking may be performed. If parity is selected, the total character length is the sum of the start bit, plus the number of data bits selected, plus the parity bit, plus the number of stop bits selected. The data rate (Baud rate) is program selected from among 15 standard speeds. The above parameters are controlled separately for each channel by the PDP-11 program and are the same for that channel’s transmitter and receiver. They are controlled by writing into the Line Parameter Register (LPR). The line parameter register is also used to selectively enable reception on each line.

Operation
The DZ11 is initialized by setting the CLR bit in the Control and Status Register (CSR) or by the INIT signal on the UNIBUS. Initialization resets all line parameters, clears the 64 character buffer, and disables all transmitters and receivers. Following initialization, the program must specify the desired character format and speed of operation and enable the receiver for each line on which it desires to receive data. It should also enable receiver interrupts, if desired (by using the CSR). It must set the Master Scan Enable (MSE) bit in the CSR so the DZ11 receivers and transmitters will function.

As each character is received, the start and stop bits are stripped off and the data bits are placed, together with the three-bit number of the line it came from and three bits of status information, in a 16-bit wide by 64-word deep first-in/first-out hardware buffer, called a “silo.” The character is stored at the time the center of the first stop bit of the
character is sampled. Each complete character is loaded into the top of the silo and propagates (falls) automatically toward the “bottom” of the silo, until it comes to rest against the bottom, or against the last previous character stored in the silo. The bottom of the silo is actually the Receiver Buffer Register (RBUF) and is seen by the program as a device register on the UNIBUS.

Silo Status Bits
In addition to the character and line number, a silo entry (and hence RBUF entry) contains several status bits.

The PARITY ERROR bit will be set if parity is enabled and a character is received on the serial line with incorrect parity. If parity is enabled, the DZ11 receiver will strip off and check the incoming parity bit, placing only the data portion of the character in the silo entry.

The FRAMING ERROR bit will be set if the serial line is in the spacing state (0) at the time of the first stop bit. The FRAMING ERROR bit can be used to detect break. Following a framing error, the serial line must return to the mark state (1) for at least 1/16 bit time before the DZ11 receiver will resume assembling characters.

The OVERRUN bit will be set if one or more characters for this line had to be discarded because the silo was full. The UARTs are double character buffered so this will occur only if the program fails to service the silo for an extended period of time or falls behind in servicing the silo. The character assembled in the entry with the OVERRUN bit set was received correctly. One or more previous characters were discarded.

The RBUF has one additional status bit, DATA VALID. This bit indicates that a character is in the RBUF. The bit will be clear when the silo is empty or if characters are propagating down the silo but no character is available at the bottom. The program must ignore the contents of bits 0-14 of RBUF if DATA VALID (bit 15) is not set. The status of these bits are undefined unless DATA VALID is set. For example, initializing the DZ11 will clear the DATA VALID bit but not the other bits of RBUF.

Interrupt Conditions
The Receiver Interrupt Enable (RIE) and Silo Alarm Enable (SAE) bits in the CSR control the circumstances upon which the DZ11 receiver interrupts the PDP-11 processor.

RIE and SAE both clear
If RIE and SAE are both clear, the DZ11 receiver never interrupts the PDP-11 processor. The program must periodically check for the availability of data in the silo and empty the silo when data is present. If the program operates off a clock it should check for characters in the silo at least as often as the time it takes for the silo to fill, allowing a safety factor to cover processor response delays and time to empty the silo. The RDONE bit in the CSR will set when a character is available in the
silo. The program can periodically check this bit with a TSTB or BIT instruction. When RDONE is set the program should empty the silo.

The program can empty the silo by repeatedly performing MOV instructions from the RBUF to temporary storage. Each MOV instruction will copy the bottom character in the silo so it won’t be lost and will clear out the bottom of the silo, allowing the next character to move down for access by a subsequent MOV instruction. The program can determine when it has emptied the silo by testing the DATA VALID bit in each word moved out of the RBUF. A zero value indicates that the silo has been emptied. The test can be performed conveniently by branching on the condition code following each MOV instruction. A TST or BIT instruction must not access the RBUF because these instructions will cause the next entry in the silo to move down without saving the current bottom character.

**NOTE**

Following a MOV from the RBUF, the next character in the silo will be available within one microsecond. On fast CPU’s, the program must use sufficient instructions or NOPs to ensure that successive MOVs from the RBUF are separated by at least one microsecond. This will prevent a false indication of an empty silo.

**RIE set, SAE clear**

If RIE is set and SAE is clear, the DZ11 will interrupt the PDP-11 processor to the DZ11 receiver vector address when RDONE is set, indicating the presence of a character at the bottom of the silo. The interrupt service routine can obtain the character by performing a MOV instruction from the RBUF. If the program then dismisses the interrupt, the DZ11 will interrupt when a subsequent character is available (which may be immediately if additional characters were placed in the silo while the interrupt was being serviced). Alternately, the interrupt service routine may respond to the interrupt by emptying the silo before dismissing the interrupt. In this case, the previously described procedure should be used to empty the silo. Emptying the silo will reduce the interrupt overhead of a heavily loaded system. With either programming approach, the DZ11 silo will buffer the incoming characters and prevent overruns should the system become temporarily overloaded.

**RIE and SAE both set**

If RIE and SAE are both set, the DZ11 will interrupt the PDP-11 processor to the DZ11 receiver vector when the SILO ALARM (SA) bit in the CSR is set. The SA bit will be set when sixteen characters have been placed in the silo since the last time the program has accessed the RBUF. Accessing the RBUF will clear the SA bit and the associated counter. The program should follow the procedure described above to empty the silo completely in response to a silo alarm interrupt. This will ensure that any characters placed in the silo while it is being emptied are processed by the program.
NOTE
If the program processes only 16 entries in response to each silo alarm interrupt, characters coming in while interrupts are being processed will build up without being counted by the silo alarm circuit and the silo may eventually overflow without the alarm being issued.

If the silo alarm interrupt is used, the program will not be interrupted if fewer than 16 characters are received. In order to respond to short messages during periods of moderate activity the PDP-11 program should periodically empty the silo. The scanning period will depend on the required responsiveness to received characters.

While the program is emptying the silo it should ensure that DZ11 receiver interrupts are inhibited. This should be done by raising the PDP-11 processor priority. The silo alarm interrupt feature can significantly reduce the PDP-11 processor overhead required by the DZ11 receiver by eliminating the need to enter and exit an interrupt service routine each time a character is received.

TRANSMITTER
The transmitter section performs parallel-to-serial conversion of data supplied by the PDP-11 program. The Line Parameter Register (LPR) enables the program to specify speed, character size, stop code and parity on a per line basis. The speed and character format for any given line are the same for the receiver and transmitter.

The transmitter for each line is double character buffered. The program has a full character time to respond to the Transmit Ready (TRDY) flag from any line and still transmit data on that line at the maximum character rate.

The program controls the DZ11 transmitter through five registers on the UNIBUS: the Control and Status Register (CSR) previously mentioned, the Line Parameter Register (LPR) previously mentioned, the Transmitter Control Register (TCR), the Transmitter Buffer (TBUF) and the Break Register (BRK).

Transmitter Operation
Following DZ11 initialization, the program must use the LPR register to specify the speed and character format for each line to be used and must set the Master Scan Enable (MSE) bit in the CSR. The program should set the Transmitter Interrupt Enable (TIE) bit in the CSR if it wants the DZ11 transmitter to operate on a program interrupt basis. If enabled, the DZ11 will interrupt the PDP-11 processor to the DZ11 transmitter interrupt vector when the Transmitter Ready (TRDY) bit in the CSR is set, indicating that the DZ11 is ready to accept a character to be transmitted.

The Transmitter Control Register (TCR) is used to enable and disable transmission on each line. One bit in this eight bit register is associated
with each line. The program can set and clear bits in this register by using MOV, MOVB, BIS, BISB, BIC and BICB instructions. (If word instructions are used, the TCR and DTR registers will be simultaneously accessed.)

The DZ11 transmitter is controlled by a scanner which is constantly looking for an enabled line (TCR bit set) which has an empty UART transmitter buffer. When the scanner finds such a line it loads the number of the line into the 3-bit Transmit Line Number (TLINE) field of the CSR and sets the TRDY bit, interrupting the PDP-11 processor if the TIE bit is set. The program can clear the TRDY bit by moving a character for the indicated line into the TBUF or by clearing the TCR bit for the line. Clearing the TRDY bit frees the scanner to resume its search for lines needing service.

**Transmission of Characters**

To initiate transmission on an idle line, the program should set the TCR bit for that line and wait for the scanner to request service on the line, as indicated by the scanner loading the number of the line into TLINE and setting TRDY. The program should then load the character to be transmitted into the TBUF by using a MOVB instruction. If interrupts are to be used, a convenient way of starting up a line is to set the TCR bit in the main program and let the normal transmitter interrupt routine load the character into the TBUF.

**NOTE**

The scanner may find a different line needing service before it finds the line being started up. This will occur if other lines request service before the scanner can find the line being started. The program must always check the TLINE field of the CSR when responding to TRDY to ensure it loads characters for the correct line. Assuming the program services lines as requested by the scanner, the scanner will eventually find the line being started. If several lines require service, the scanner will request service in priority order as determined by line number. Line 7 has the highest priority and line 0 the lowest.

To continue transmission on a line, the program should load the next character to be transmitted into the TBUF each time the scanner requests service for the line as indicated by TLINE and TRDY.

To terminate transmission on a line, the program should load the last character normally and wait for the scanner to request an additional character for the line. The program clears the TCR bit at this time instead of loading the TBUF.
the line. The program clears the TCR bit at this time instead of loading the TBUF.

Transmission of Breaks
The normal rest condition of the Transmitted Data lead for any line is the marking (1) state. The Break Register (BRK) is used to apply a continuous spacing signal to the line. One bit in this eight bit register is associated with each line. The line will remain in the spacing condition so long as the bit remains set. The program should use a MOVB instruction to access the BRK register. If the program continues to load characters for a line after setting the break bit, transmitter operation will appear normal to the program despite the fact that no characters can be transmitted while the line is in the continuous spacing state. The program may use this facility for sending precisely timed spacing signals by setting the break bit and using Transmit Ready interrupts as a timer.

It should be remembered that each line in the DZ11 is double buffered. The program must not set the BRK bit too soon or the two data characters proceeding the spacing may not be transmitted. The program must also ensure that the line returns to the mark state at the end of the spacing period before transmitting any additional data characters. The following procedure will accomplish this. When the scanner requests service the first time after the program has loaded the last data character, the program should load an all-zero character. When the scanner requests service the second time, the program should set the BRK bit for the line. At the end of the spacing period the program should load an all-zero character to be transmitted. When the scanner requests service indicating this character has begun transmission the program should clear the BRK bit and load the next data character.

DATA SET CONTROL
DZ11 models with EIA/CCITT interfaces include data set control as a standard feature. The program may sense the state of the Carrier and Ring Indicator signals from each data set and may control the state of the Data Terminal Ready signal to each data set. These signals enable the DZ11 to interface to full duplex data sets used for switched network operation, such as the Bell models 103 and 113, or equivalent.

Data Set Control Registers
The program uses three 8-bit registers to access the DZ11 data set control logic. One bit in each register is associated with each of the 8 lines. There are no hardware interlocks between the data set control logic and the receiver and transmitter logic. Any required coordination should be done under program control.

The Data Terminal Ready (DTR) register is a read/write register. Setting or clearing a bit in this register will turn the appropriate Data Terminal Ready signal on or off. The program may access this register with word or byte instructions. (If word instructions are used the DTR and TCR registers will be simultaneously accessed.) The DTR register is cleared by the INIT signal on the UNIBUS but is not cleared if the program clears the DZ11 by setting the CLR bit of the CSR.
The Carrier Register (CAR) and Ring Register (RING) are read-only registers. The program can determine the current state of the carrier signal for a line by examining the appropriate bit of the CAR register. It can determine the current state of the ring signal by examining the appropriate bit of the RING register. The program can examine these registers separately by using MOVB or BITB instructions or can examine them as a single 16 bit register by using MOV or BIT instructions. The DZ11 data set control logic does not interrupt the PDP-11 processor when a carrier or ring signal changes state. The program should periodically sample these registers to determine the current status. Sampling at a high rate is not necessary.

EIA LINE INTERFACE
The distribution panel supplied with the DZ11-A and DZ11-E includes 16 Cinch DB25P plugs for connection to modems or local terminals. For connection to modems an “extension cable” is required which has a DB25S socket at one end and a DB25P plug at the other. The DB25S socket connects to the DB25P plug on the DZ11 distribution panel and the DB25P plug connects to the modem. The BC05D-25 is such a cable and is 25 feet long. The maximum cable length between the DZ11 and a modem must not exceed 50 feet to ensure that operation conforms to the EIA RS-232-C and CCITT V.24 interface specifications.

Local Terminals
For connection to local terminals which have an EIA/CCITT interface a “null modem” cable is required which has a DB25S socket on each end. The cable must be wired to connect the transmitted data lead of each end to the received data lead of the opposite end. The DB25S sockets connect to the DB25P plugs on the DZ11 distribution panel and the terminal. The BC03M Null modem cable is such a cable and is available in lengths from 25 to 1000 feet. An alternate wiring approach would be to use a BC05D extension cable together with an H312-A Null Modem.

Operation over Long Cables
Operation beyond 50 feet does not conform to the RS-232-C or CCITT V.24 specifications. However operation will often be possible at longer distances depending on the terminal equipment, type of cable, speed of operation and electrical environment. Reliable communication over long cables depends on the absence of excessive electrical noise. For these reasons, DIGITAL can not guarantee error free communication beyond 50 feet. However, the EIA/CCITT versions of the DZ11 may be connected to local DIGITAL terminals (and most other terminals) at distances beyond 50 feet with satisfactory results if the terminal and computer are located in the same building, in a modern office environment. Shielded twisted pair (Belden 8777 or equivalent) is recommended and is used in the BC03M cable.
NOTE
The ground potential difference between the DZ11 and terminal must not exceed two volts. This requirement will generally limit operation to within a single building served by one AC power service. In other cases, or in noisy electrical environments, 20 ma operation should be used.

20 MILLIAMPS LINE INTERFACE
The distribution panel supplied with the DZ11-C and DZ11-F includes 16 four-screw terminal strips for connection to local terminals having a 20 ma interface. Two types of cable are often used to connect 20 ma terminals to a DZ11, quad station wire #22 AWG (DEC part number 91-5856-04) and 3 shielded twisted pair (Belden 8777, DEC part number 91-07723). The cables can connect directly to the DZ11 screw terminals. A pair of Mat-N-Lok connectors (order number 959-A and 959-B) may be inserted at convenient points in the cable for quick connection and disconnection.

The DZ11 transmitter and receiver have an active interface for connection to devices such as terminals which have a passive transmitter and receiver. An active interface supplies current to the loop and must be connected to a passive interface. The DZ11 can be connected directly to computer interfaces such as the DL11-WA and DF11-K which can be strapped for passive operation. To connect a DZ11 to an interface not capable of passive operation, such as another DZ11, a pair of H319 20 ma receivers should be used to convert from active to passive.

MAINTENANCE FEATURES
The DZ11 has a number of features that ensure reliable operation and ease of maintenance. The DZ11 circuitry makes extensive use of large scale integration (LSI), minimizing the number of components and reducing the likelihood of failure. Line speed and format parameters are program-controlled, reducing the number of switches on the module, thereby speeding installation and reducing the chance of an incorrect switch setting. A single module contains the complete logic for 8 lines, permitting fault isolation to the module level on the basis of function.

The Maintenance (MAINT) bit of the CSR permits a diagnostic program to loop back each transmitter to the associated receiver. This feature enables the program to diagnose 90% of the DZ11 logic without changing any cables. The BRK register does not function while the MAINT bit is set.

Two special test connectors are supplied with the EIA models of the DZ11 and are used to check out the remaining portions of the DZ11. An
8-line turnaround connector (H327) can be connected to the DZ11 logic module in place of the ribbon cable to the distribution panel. This connector loops back lines in pairs (0 to 1, 2 to 3, 4 to 5, 6 to 7) and permits a complete check of DZ11 logic. A single-line turnaround connector (with DB25S socket) (H325) can be connected to the distribution panel or the modem end of a BC05D cable and permits a complete check of the distribution panel and associated cabling.

PROGRAMMING

General
A program in the PDP-11 controls a DZ11 through nine device registers. In some cases, two registers share the same UNIBUS address, with register selection determined by whether the program is writing data to the DZ11 (DATA0 UNIBUS cycle) or reading data from the DZ11 (DATA1 UNIBUS cycle). Some of the registers are 8 bits wide, others are 16 bits wide. The 16 line models of the DZ11 have a separate set of device registers for each 8 lines.

The DZ11 uses 8 bytes of floating address space. The relative position of the DZ11 within the floating address system is number eight directly following DMC11.

The registers are:

<table>
<thead>
<tr>
<th>Name</th>
<th>Address</th>
<th>Size</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control and Status Register (CSR)</td>
<td>76XXX0</td>
<td>word</td>
<td>read/write</td>
</tr>
<tr>
<td>Line Parameter Register (LPR)</td>
<td>76XXX2</td>
<td>word</td>
<td>write only</td>
</tr>
<tr>
<td>Receiver Buffer Register (RBUF)</td>
<td>76XXX2</td>
<td>word</td>
<td>read only</td>
</tr>
<tr>
<td>Transmitter Control Register (TCR)</td>
<td>76XXX4</td>
<td>byte</td>
<td>read/write</td>
</tr>
<tr>
<td>Data Terminal Ready Register (DTR)</td>
<td>76XXX5</td>
<td>byte</td>
<td>read/write</td>
</tr>
<tr>
<td>Transmitter Buffer (TBUF)</td>
<td>76XXX6</td>
<td>byte</td>
<td>write only</td>
</tr>
<tr>
<td>Break Register (BRK)</td>
<td>76XXX7</td>
<td>byte</td>
<td>write only</td>
</tr>
<tr>
<td>Ring Register (RING)</td>
<td>76XXX6</td>
<td>byte</td>
<td>read only</td>
</tr>
<tr>
<td>Carrier Register (CAR)</td>
<td>76XXX7</td>
<td>byte</td>
<td>read only</td>
</tr>
</tbody>
</table>

Vector Assignment
The DZ11 uses two interrupt vectors; XX0 for the receiver section and XX4 for the transmitter section. If both interrupts occur simultaneously the receiver has priority (is closer to the processor on the UNIBUS). The interrupt priority for both vectors is controlled by one standard PDP-11 priority connector. The priority can be changed by substituting the appropriate connector. DZ11’s will be shipped with a priority 5 connector.

Register Definition
The following charts present the bit assignments within each register. All bits in read-only registers are read-only. All bits in write-only registers are write-only. Instructions which make DATAIP UNIBUS cycles, such as BIC and BIS, should not be used to access read-only and write-only registers. Attempting to write unused bits has no affect on the bits. Unused
bits read back as zero. However, users are cautioned against arbitrarily loading or testing unassigned bits as DIGITAL reserves the right to assign these bits in future models.

**CONTROL AND STATUS REGISTER (CSR) R/W ADDRESS 76XXX0**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-02</td>
<td>Unused</td>
</tr>
</tbody>
</table>
| 03   | Maintenance (MAINT) (R/W)  
When this bit is set, the serial output from each transmitter is fed back as the serial input of the associated receiver. The program may set and clear this bit. This bit is cleared by INIT and CLR. |
| 04   | Clear (CLR) (R/W)  
When the program sets this bit, all DZ11 logic is initialized with the exception of the DTR register. This bit is a 15 μsec one-shot and will self-clear. Do not address the DZ11 while this bit is set. |

**NOTE**  
CLR and INIT perform the same initialization function except that INIT also initializes the DTR register.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
</table>
| 05   | Master Scan Enable (MSE) (R/W)  
When this bit is set, the DZ11 scanner is turned on, allowing the transmitter and receiver logic to operate. The program may set and clear this bit. This bit is cleared by INIT and CLR. |
| 06   | Receiver Interrupt Enable (RIE) (R/W)  
When this bit is set, receiver interrupts are enabled. The program may set or clear this bit. This bit is cleared by INIT and CLR. A receiver interrupt is generated when the device sets RDONE if RIE is set and SAE is clear. A receiver interrupt is generated when the device sets SA if RIE and SAE are both set. |
| 07   | Receiver Done (RDONE) (Read only)  
This bit is set by the device when a character becomes available in the RBUF. It is cleared by the device when the program accesses the RBUF, but will set again when another character becomes available in the RBUF. This bit is cleared by INIT and CLR. |

2-247
08-10 Transmitter Line Number (TLINE) (Read only)
If TRDY is set, these bits contain the three-bit number of the line requiring a character for transmission. These bits are not valid if TRDY is clear. These bits are loaded by the device when the scanner finds an enabled line with an empty transmitter buffer. The bits are cleared by INIT and CLR.

11 Unused

12 Silo Alarm Enable (SAE) (R/W)
When this bit is set, the silo alarm is enabled, permitting the SA bit to operate and causing receiver interrupts to be generated (if enabled) when the SA bit is set instead of when the RDONE bit is set. The program may set and clear this bit. This bit is cleared by INIT and CLR.

13 Silo Alarm (SA) (Read only)
This bit is set by the device when the sixteenth character is placed in the silo following the last reference to the RBUF by the program. This bit is cleared when the program references the RBUF. This bit is cleared by INIT and CLR. This bit and the associated counter are both held clear when SAE is clear.

14 Transmitter Interrupt Enable (TIE) (R/W)
When this bit is set, transmitter interrupts are enabled. The program may set and clear this bit. This bit is cleared by INIT and CLR. A transmitter interrupt is generated when the device sets TRDY, if this bit is set.

15 Transmitter Ready (TRDY) (Read only)
This bit is set by the device when the scanner has found a line with an empty transmitter buffer which is enabled in the TCR. When this bit is set, the TLINE bits indicate the number of the line in question. This bit is cleared by the device when the program references the TBUF or clears the TCR bit for the indicated line, but will reset within 1.9 microseconds if there is another enabled line with an empty transmitter buffer. This bit is cleared by INIT and CLR.

LINE PARAMETER REGISTER (LPR) Write Only Address 76XXX2

The Line Parameter Register is a write-only register. The program should access this register with a MOV instruction. Instructions which require DATAIP UNIBUS cycles, such as BIC and BIS, may not be used. Byte
instructions may not be used. When the DZ11 is initialized by INIT or CLR the line parameters for each line will be initialized to the clear state.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-02</td>
<td>Line Number</td>
</tr>
<tr>
<td></td>
<td>These three bits contain a binary number used to select the line for which parameters are to be loaded.</td>
</tr>
<tr>
<td>03-04</td>
<td>Character Length</td>
</tr>
<tr>
<td></td>
<td>These two bits specify the character length (not counting start bit, stop bits, and parity bit if enabled) for the selected line.</td>
</tr>
<tr>
<td>Bit 4</td>
<td>Bit 3</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>05</td>
<td>Stop Code</td>
</tr>
<tr>
<td></td>
<td>This bit specifies the stop code length for selected line</td>
</tr>
<tr>
<td>0</td>
<td>1 stop bit</td>
</tr>
<tr>
<td>1</td>
<td>2 stop bits</td>
</tr>
<tr>
<td></td>
<td>(1.5 for 5 bit characters)</td>
</tr>
<tr>
<td>06</td>
<td>Parity</td>
</tr>
<tr>
<td></td>
<td>This bit specifies whether a parity bit is generated on transmission and checked and stripped on reception for the selected line</td>
</tr>
<tr>
<td>0</td>
<td>no parity bit</td>
</tr>
<tr>
<td>1</td>
<td>parity enabled</td>
</tr>
<tr>
<td>07</td>
<td>Odd Parity</td>
</tr>
<tr>
<td></td>
<td>This bit specifies whether the selected line is to have even or odd parity generated and checked. This bit has no effect unless PARITY is set.</td>
</tr>
<tr>
<td>0</td>
<td>even parity</td>
</tr>
<tr>
<td>1</td>
<td>odd parity</td>
</tr>
<tr>
<td>08-11</td>
<td>Speed Select</td>
</tr>
<tr>
<td></td>
<td>These four bits specify the speed of operation of the receiver and transmitter for the selected line.</td>
</tr>
<tr>
<td>bit 11</td>
<td>10 9 8 Baud rate</td>
</tr>
<tr>
<td>0</td>
<td>0 0 0 50</td>
</tr>
<tr>
<td>0</td>
<td>0 0 1 75</td>
</tr>
<tr>
<td>0</td>
<td>0 1 0 110</td>
</tr>
<tr>
<td>0</td>
<td>0 1 1 134.5</td>
</tr>
<tr>
<td>0</td>
<td>1 0 0 150</td>
</tr>
<tr>
<td>0</td>
<td>1 0 1 300</td>
</tr>
<tr>
<td>0</td>
<td>1 1 0 600</td>
</tr>
<tr>
<td>0</td>
<td>1 1 1 1200</td>
</tr>
<tr>
<td>1</td>
<td>0 0 0 1800</td>
</tr>
<tr>
<td>1</td>
<td>0 0 1 2000</td>
</tr>
</tbody>
</table>
12 RCVR ON
This bit specifies whether the clock for the receiver of the selected line is enabled. This bit must be set for the receiver to operate. The RCVR ON bit for each line is cleared by INIT and CLR.

13-15 Unused

RECEIVER BUFFER REGISTER (RBUF) Read Only Address 76XXX2

The Receiver Buffer Register is a read-only register. The program should access this register with a MOV instruction. Byte instructions may not be used. The register is a “read-once” register. Reading it will advance the silo and permit the next character to be presented. Unless bit 15 is set, bits 0-14 are not valid and should be ignored by the program.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-07</td>
<td>Rcv Char</td>
</tr>
<tr>
<td>08-10</td>
<td>Line Number</td>
</tr>
<tr>
<td>11</td>
<td>Unused</td>
</tr>
<tr>
<td>12</td>
<td>Parity Error</td>
</tr>
<tr>
<td>13</td>
<td>Framing Error</td>
</tr>
</tbody>
</table>

These bits contain the received character. Bits are received Least Significant Bit (LSB) first. If parity is enabled, the parity bit is stripped off. Characters less than 8 bits long are right adjusted with the high order bits set to 0.

These three bits contain the binary number of the line on which the character was received.
Bits | Description
---|---
14 | Overrun
This bit is set if one or more previous characters were lost on the line on which the character was received due to the silo being full. The received character is valid.

15 | Data Valid
When this bit is set, the remaining bits in the RBUF are valid. This bit is set when a character becomes available in the RBUF. This bit is cleared when the program references the RBUF, but will set again within 1 μsecond if additional characters are in the silo. This bit is cleared by INIT and CLR.

**NOTE**
INIT and CLR do not clear the other bits in the RBUF.

**TRANSMITTER CONTROL REGISTER (TCR) R/W Address 76XXX4**

Each bit in this eight bit register is associated with one line. If the transmit enable bit for a particular line is set, the transmitter scanner will stop and request service for the line when it finds the transmitter buffer for the line empty. The scanner will restart if the program clears the TCR bit for the line. The program may set and clear bits in this register. However, the program must not clear the TCR bit for a line except when the scanner has stopped and requested service for the line. The register is cleared by INIT and CLR.

**DATA TERMINAL READY REGISTER (DTR) R/W Address 76XXX5**

Each bit in this eight bit register is associated with a particular line. When the Data Terminal Ready bit is set for a particular line, the Data Terminal Ready data set control signal will be in the on state; when the
bit is clear the signal will be in the off state. The program may set and clear bits in this register. The register is cleared by INIT, but is unaffected by CLR.

NOTE
The 20 ma models of the DZ11 do not have data set control. The program may read or write the DTR register of these models, but the value read back will always be zero.

TRANSMITTER BUFFER (TBUF) Write Only Address 76XXX6

This register is loaded by the program with characters to be transmitted in response to the TRDY bit in the CSR. When TRDY is set, writing this register will transfer the character loaded to the transmitter buffer of the line indicated by the TLINE bits in the CSR and will clear TRDY. The character will be transmitted LSB first, preceded by a start bit and followed by a parity bit if parity is enabled and by stop bits. The character should be loaded into TBUF right-justified.

BREAK REGISTER (BRK) Write Only Address 76XXX7

Each bit in this write-only register is associated with one line. When the bit is set for a particular line the transmitted data lead for the line will be held in the spacing (0) state, although the transmitter will appear to the program to be functioning normally. The program may set or clear bits in this register. The register is cleared by INIT and CLR.

NOTE
Break bits affect only the data transmitted on the serial lines. They do not affect the loop-back data seen by DZ11 receivers when the MAINT bit in the CSR is set.

RING REGISTER (RING) Read Only Address 76XXX6

2-252
Each bit in this read-only register is associated with one line. The bit for a particular line reflects the state of the Ring lead of the line interface. The bit will be set when the Ring lead is in the on state.

**NOTE**
The 20 ma models of the DZ11 do not have data set control. If the program reads the RING register of these models the value read back will always be zero.

**CARRIER REGISTER (CAR) Read Only Address 76XXX7**

![Diagram of CARRIER REGISTER (CAR)]

Each bit in this read-only register is associated with one line. The bit for a particular line reflects the state of the Carrier lead of the line interface. The bit will be set when the Carrier lead is in the on state.

**NOTE**
The 20 ma models of the DZ11 do not have data set control. If the program reads the CAR register of these models the value read back will always be zero.

**SPECIFICATIONS**

**Function**
The DZ11 provides an interface between the PDP-11 UNIBUS and 8 or 16 asynchronous bit-serial communications channels, depending on the model:
- DZ11-A, DZ11-B, DZ11-C
- DZ11-D
- DZ11-E, DZ11-F

**Connectability**
A maximum of 128 lines may be connected to a single PDP-11 using DZ11 interfaces.

**Operating Mode**
Full or Half Duplex.

**Data Format**
Asynchronous, serial by bit. One start and 1, 1½ (5 level codes only), or 2 stop bits supplied by the hardware. The DZ11 will accommodate characters of 5, 6, 7 or 8 bits with or without even or odd parity. The data format is the same for transmitted and received data on any line. The data format is program controlled separately for each line.

2-253
The transmitted data lead may be held in the (0) state under program control.

**Order of Bit Transmission and Reception**

Low order bit first.

**Data rate**

Program-controlled on an individual line basis with the following speeds available: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200 and 9600 Baud. The receiver and transmitter of a given line operate at the same speed. Timing is provided by a crystal oscillator accurate to $\pm 0.01\%$. However, the nominal speed at 134.5 Baud is $0.016\%$ fast and at 2000 Baud $0.253\%$ fast.

**Distortion**

The DZ11 receiver operates properly in the presence of $40\%$ ($38\%$ at 2000 baud) space-to-mark or mark-to-space distortion between any two received bits and with up to $\pm 4.5\%$ ($4.3\%$ at 2000 baud) long-term speed distortion provided the data format contains at least 1.5 stop units. If the data format contains only one stop unit, the speed tolerance is $\pm 4\%$ ($3.8\%$ at 2000 baud). The DZ11 transmitter operates with less than $3\%$ bit-to-bit distortion.

**BUS Loading**


**Mounting Space**

DZ11-A, DZ11-C: one hex-sized SPC slot in a DD11 backplane or processor backplane plus one small panel ($5\frac{1}{4}''$) space in a cabinet. DZ11-B, DZ11-D: one hex-sized SPC slot. DZ11-E, DZ11-F: two hex-sized SPC slots (not necessarily adjacent) plus one small panel space.

**Electrical Interface**

DZ11-A, DZ11-B, DZ11-E:

These models provide a voltage level interface whose levels and connector pinnings conform to Electronics Industries Association (EIA) Standard RS-232-C and CCITT recommendation V.24. The leads supported are:

<table>
<thead>
<tr>
<th>Pin</th>
<th>RS232C</th>
<th>CCITT V.24</th>
</tr>
</thead>
<tbody>
<tr>
<td>Protective ground</td>
<td>1</td>
<td>Circuit AA</td>
</tr>
<tr>
<td>Signal ground</td>
<td>7</td>
<td>Circuit AB</td>
</tr>
<tr>
<td>Transmitted data</td>
<td>2</td>
<td>Circuit BA</td>
</tr>
<tr>
<td>Received data</td>
<td>3</td>
<td>Circuit BB</td>
</tr>
<tr>
<td>Data Terminal Ready</td>
<td>20</td>
<td>Circuit CD</td>
</tr>
<tr>
<td>Ring Indicator</td>
<td>22</td>
<td>Circuit CE</td>
</tr>
<tr>
<td>Carrier</td>
<td>8</td>
<td>Circuit CF</td>
</tr>
</tbody>
</table>

2-254
NOTE
Signal ground and Protective ground are connected together at the distribution panel.

NOTE
Request to Send, pin 4, circuit CA, CCITT 105, is connected to Data Terminal Ready through a removable jumper on the distribution panel.

DZ11-C, DZ11-D, DZ11-F:
These models provide a 20 ma current loop interface terminated by four-screw terminal blocks. The transmitter has an active interface and is balanced. The receiver has an active interface which is pseudo-differential for improved noise immunity. The maximum permissible loop resistance is:
transmitter: 560 Ohms
receiver: 750 Ohms

Power Requirements

<table>
<thead>
<tr>
<th>Model</th>
<th>+5V</th>
<th>-15V</th>
<th>+15V</th>
</tr>
</thead>
<tbody>
<tr>
<td>DZ11-A, DZ11-B</td>
<td>2.5 amps</td>
<td>.15 amps</td>
<td>.13 amps</td>
</tr>
<tr>
<td>DZ11-C, DZ11-D</td>
<td>3.0</td>
<td>.3</td>
<td>.13</td>
</tr>
<tr>
<td>DZ11-E</td>
<td>5.0</td>
<td>.3</td>
<td>.26</td>
</tr>
<tr>
<td>DZ11-F</td>
<td>6.0</td>
<td>.6</td>
<td>.26</td>
</tr>
</tbody>
</table>

Heat Dissipation

<table>
<thead>
<tr>
<th>Model</th>
<th>BTU/hr.</th>
</tr>
</thead>
<tbody>
<tr>
<td>DZ11-A, DZ11-B</td>
<td>57</td>
</tr>
<tr>
<td>DZ11-C, DZ11-D</td>
<td>74</td>
</tr>
<tr>
<td>DZ11-E</td>
<td>114</td>
</tr>
<tr>
<td>DZ11-F</td>
<td>148</td>
</tr>
</tbody>
</table>

Environment

Operating temperature +5 to +50°
Humidity 10 to 95%
Reference: DEC STD 102—Class C device

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Option</th>
<th>Prerequisite</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DZ11-A</td>
<td>PDP-11</td>
<td>8 Line Async Mux (EIA)</td>
</tr>
<tr>
<td>DZ11-B</td>
<td>DZ11-A</td>
<td>8 Line Expander (EIA)</td>
</tr>
<tr>
<td>DZ11-C</td>
<td>PDP-11</td>
<td>8 Line Async Mux (20 ma)</td>
</tr>
<tr>
<td>DZ11-D</td>
<td>DZ11-C</td>
<td>8 Line Expander (20 ma)</td>
</tr>
<tr>
<td>DZ11-E</td>
<td>PDP-11</td>
<td>16 Line Async Mux (EIA)</td>
</tr>
<tr>
<td>DZ11-F</td>
<td>PDP-11</td>
<td>16 Line Async Mux (20 ma)</td>
</tr>
</tbody>
</table>

2-255
Related Options

Option No. | Description
--- | ---
BC05D-25 | Modem cable (25 ft.), 25-conductor cable terminated in Cinch DB25S socket at one end and DB25P plug at the other end for connection of one line from DZ11-A or DZ11-E distribution panel to modem, data set, or null modem, listed below.

BC03M-XX | Null Modem Cable 3—shielded twisted pair cable terminated in Cinch DB25S sockets at each end for connecting local terminals with EIA/CCITT interfaces to the DZ11-A or DZ11-E distribution panel. This cable is supplied in standard lengths of 25 feet (BC03M-25), 100 feet (BC03M-A0), 250 feet (BC03M-B5), 500 feet (BC03M-E0), and 1000 feet (BC03M-L0).

H312-A | Null Modem for connecting local terminals with EIA interfaces to DZ11-A and DZ11-E distribution panels when BC05D modem cables are used.

H319 | 20 ma current loop receiver. Converts a 20 ma active interface into a 20 ma passive interface. A pair of H319's should be used when connecting one line of a 20 ma DZ11 to one line of another DZ11 or to another 20 ma interface with active transmitter and receiver.
ASYNCHRONOUS NULL MODEM, H312-A

ASYNCHRONOUS NULL MODEM, H312-A
The H312 null modem allows a user to connect a terminal device to a computer without the use of two modems as would be normally required. It consists of two female 25-pin data-phone sockets mounted on a printed circuit board with the 15 most commonly used wires brought out to split lugs in the center of the board. The split lug allows the user to interconnect the two sockets in any way he wishes as long as the pins used are on the split lug interconnection points.

The H312 is wired (as shown below) to simulate back-to-back Bell 103A's. However, the user may make wiring modifications.

---

UNLESS OTHERWISE INDICATED:
CONNECTORS ARE DB25S-3
○ = SPLIT LUGS
----- = WIRE JUMPERS TO BE SOLDERED TO SPLIT LUGS.
COMMUNICATIONS ARITHMETIC OPTION, KG11-A

FEATURES
- Computes three different Cyclic Redundancy Check (CRC) polynomials and two Longitudinal Redundancy Checks (LRC)—CRC-16, CRC-12, CRC-CCITT, LRC-8, LRC-16
- Program selection of desired polynomial
- Fits in small peripheral slot
- Computes an 80-character message block in less than 100 microseconds

DESCRIPTION
The KG11-A is attached to the UNIBUS and is used to compute a Cyclic Redundancy Check (CRC) or Longitudinal Redundancy Check (LRC) for detecting errors in serially transmitted data. It is used with a DU11 serial synchronous line interface to compute the Block Check Character(s) (BCC) appearing at the end of a block of data transmitted over a serial synchronous line.

A typical configuration might be:

For received data, the characters are moved to the KG11-A and a BCC is computed for the data and compared to the BCC received. If they are equal, the data is assumed to be correct and is accepted. If they do not match, the message is not accepted and the data is retransmitted.

When data is being transmitted, the BCC is generated by moving all the characters to the KG11-A. The resulting BCC is transmitted at the end of the message.

* Not all characters are included in the BCC. The exclusions will depend on the line protocol used.

The KG11-A, under program control, can compute the most popular CRC and LRC polynomials:

1. CRC-16 \( X^{16} + X^{15} + X^2 + 1 \)
2. CRC-12 \( X^{12} + X^{11} + X^3 + X^2 + X + 1 \)
3. CRC-CCITT \( X^{16} + X^{12} + X^5 + 1 \)
4. LRC-8 \( X^8 + 1 \)
5. LRC-16 \( X^{16} + 1 \)
CRC-16

CRC-16 is used for synchronous systems that employ 8-bit characters. It is used in IBM binary synchronous systems when the transmission code is EBCDIC or 8-bit transparency. For IBM compatible systems, the message format is:

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>Ebb</td>
</tr>
<tr>
<td>(1) T—text—Tcc</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>Bcc</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>Ebb</td>
</tr>
<tr>
<td>(2) T—text—Tcc</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>Xcc</td>
</tr>
</tbody>
</table>

| S | Ebb |
| (3) T—text—Tcc | text—Tcc |
| X | Bcc |
| Bcc |

| S | Ebb |
| (4) T—text—Tcc | text—Tcc |
| X | Bcc |
| Xcc |

In the preceding examples, each character represents an 8-bit character. The first BCC character is the least significant 8 bits of the BCC computed in the KG11-A. The STX is not included in the BCC. The BCC includes the first text character through the ETB, ITB or ETX. In examples (3) and (4), the second BCC begins with the character following the first BCC in the block (even if it is an STX or DLE). The examples are for normal transmission. For transparent transmission, the characters indicated by (*) in the following example are not included in the BCC.

| DS | DD | D I b b | DS | D E b b |
| LT—text—LL | text—L T c c | L T | text—L T c c |
| EX | EE | E B c c | E X | E X c c |

1 At this point, a new BCC sequence is begun which includes initialization of the BCC registers.

The DLE DLE indicates that the second DLE is really data and not the control character and is, therefore, included in the BCC. It may appear in text as often as that 8-bit representation is required. Because the DLE ITB sequence takes the system out of the transparent mode, the DLE STX following the BCC is included in the next BCC and also puts the system back into the transparent mode.

CRC-12

CRC-12 is used for six-bit characters. It is compatible with IBM Binary Synchronous Communications (BSC) when the transmission code used is Six-Bit Transcode. The characters included in or excluded from the BCC are the same as for CRC-16. The difference is only in the length of character (6 versus 8 bits).

CRC-CCITT

CRC-CCITT is the standard polynomial used to compute BCC for European systems. The characters included or excluded will depend on the line protocol used for the system in which the KG11-A is used.
LRC-8
Some systems use only an 8-bit LRC on the characters. LRC-8 performs an exclusive OR on an 8-bit or less character. The LRC is usually used in combination with a Vertical Redundancy Check (VRC). VRC is possible only when the characters are 7-bit or less plus one parity bit. LRC/VRC is used for IBM BSC when the transmission code is USACII. For IBM systems, the parity bit makes the character contain an odd number of bits.

LRC-16
LRC-16 performs an exclusive OR on a 16-bit or less character. It can be used to perform a word exclusive OR, or to compute LRC for 10, 11 and 12 bit characters transmitted via a DP11 with the DP11-CA option.

KG11-A Programming Techniques—Recommended Practice
There are two ways to use the KG11-A: Message Basis and Character by Character (Partial BCC). It is recommended that the KG11-A be used to compute on a message basis. The BCC register is Write Only. Therefore, a partial BCC has to be loaded through the data register in the LRC-16 mode. To do a partial polynomial computation (character by character), for example, a character is added to the accumulation as it is received. This can be done efficiently for one line (half duplex) because the BCC can be left in the KG11-A until all the characters have been processed. However, for full duplex and/or multiple lines, the BCC accumulation cannot be left in the KG11-A because it may have to be used for another line before the next character appears. Therefore, the partial BCC has to be saved and reloaded when the next character appears. The following sequence is required to load a partial BCC, add a character, and store the new partial BCC:

1. Set mode to LRC-16 and clear BCC
2. Load the partial BCC
3. Test DONE flag
4. Set mode to proper polynomial (don’t clear BCC)
5. Load character
6. Test DONE flag*
7. Store partial BCC

* Depending on which PDP-11 processor is used, these tests may not be required for single-byte operations because the KG11-A completes the operation in one microsecond. For word operations, the maximum cycle time of the KG11-A is 2 µsec. The KG11-A does not generate an interrupt so, if a programmer wants confirmation, he must test the DONE bit.

It is recommended that the message be passed through the KG11-A in one continuous loop operation after the entire message is received or prior to commencing transmission. If this method is undesirable, multiple KG11’s can be used. For full duplex, two KG11-A’s can be used, one for each direction. Addresses for eight KG11-A’s have been allocated.

Figure 1 is a flow chart of the recommended practice (complete BCC). The numbers in parenthesis represent the KG11-A operations.

* Not required but may be used (see description).
KG11-A Programming

Registers

The KG11-A consists of these three registers:

<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7707x0</td>
<td>Status register</td>
</tr>
<tr>
<td>7707x2</td>
<td>BCC register</td>
</tr>
<tr>
<td>7707x4</td>
<td>Data register</td>
</tr>
</tbody>
</table>

Where \( x = 0-7 \), assignments for 8 KG11-A's.

Status Register—This is a 16-bit register used to control (set mode) and to present status. Some bits are Read Only (QUO, DONE), some are Write Only (STEP, CLR) and the rest are Read/Write. Figure 2 describes the status register.
**KG11**

**BCC Register**—This is the result register and is Read Only. The format of this register will be described later for each KG11-A operational mode.

**Data Register**—This is a 16-bit Write Only register. It is used as the input register for the data on which the BCC is calculated. The format of the input data will be described later for each KG11-A operational mode.

---

**STATUS REGISTER**

```
<p>| | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>15-9</td>
<td>R</td>
<td>R/W</td>
<td>W</td>
<td>W</td>
<td>R/W/R/W/R/W/R/W</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

- **R** = Read Only
- **W** = Write Only (ONES)
- **R/W** = Read/Write

---

**Figure 2**

**Initialize KG11-A ((1) in Figure 1)**

The initialization procedure consists of moving a command word to the Status Register that selects the desired polynomial, indicates whether bytes or words will be presented for accumulation, indicates whether the unit is to cycle or be single stepped and clears the BCC register.

**Select the Desired Polynomial**

The polynomial is selected by a combination of bits 2, 1, 0 (CRC1/C, LRC, 16 BCC respectively) of the Status Register. The bit selection is as follows:
<table>
<thead>
<tr>
<th>Polynomial</th>
<th>STATUS BIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2</td>
</tr>
<tr>
<td>CRC I/C</td>
<td>CRC LRC</td>
</tr>
<tr>
<td>1. CRC-12</td>
<td>0</td>
</tr>
<tr>
<td>2. CRC-16</td>
<td>0</td>
</tr>
<tr>
<td>3. LRC-8</td>
<td>0</td>
</tr>
<tr>
<td>4. LRC-16</td>
<td>0</td>
</tr>
<tr>
<td>5. Undefined*</td>
<td>1</td>
</tr>
<tr>
<td>6. CRC-CCITT</td>
<td>1</td>
</tr>
<tr>
<td>7. Undefined*</td>
<td>1</td>
</tr>
<tr>
<td>8. Undefined*</td>
<td>1</td>
</tr>
</tbody>
</table>

* The "undefined" polynomials mean the combinations will have undefined results.

**Indicate Word or Byte Operation (DDB)**

The purpose of this indicator is to tell the KG11-A if the data register will be loaded each time with a word (16 bits) or a byte (8 bits). Bit 3 (DDB) selects word (DDB = 1) or byte (DDB = 0). Even if characters are being accumulated, the program loop (Figure 1) is shorter if the characters can be presented two-at-a-time (WORD option).

**Caution:**

CRC computations are correct only if the characters are presented to the KG11-A in the order in which they are put on or received from the communications line. If the messages are formed (received) in byte mode, then a word move can be made to the Data Register. In other words, the message must be stored in memory in ascending order of byte address. Figure 3 shows the order of characters on the basis of words moved to the KG11-A.

### Character Order

**Relative Word Address**

<table>
<thead>
<tr>
<th>0</th>
<th>2</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>6</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>8</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Figure 3*

The position of the data for the KG11-A option is given in Figure 4. Note that if CRC-12 is selected, double mode (DDB = 1) produces undefined results.
Cycle or Single-Step Mode
For diagnostic purposes, the unit can be single stepped and the operation can be monitored at each step. For normal operation, a complete cycle can be initiated. The two states are set up as follows:

<table>
<thead>
<tr>
<th>Operation</th>
<th>Status Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycle</td>
<td>SEN 1</td>
</tr>
<tr>
<td>Single Step</td>
<td>STEP Ignored</td>
</tr>
</tbody>
</table>

Cycle Mode
Once the status register is initialized with SEN = 1, the KG11-A will perform a complete cycle each time the data register is loaded as specified in Figure 4. Once the data register is loaded, the DONE flag is inactivated until all shifting ceases and the new BCC is in the BCC Register. Elapsed time is 2 μsec (max) for 16 data bits and 1 μsec (max) for 8 or less data bits. The programmer can test the DONE flag (there is no interrupt unless requested) but it is not necessary for proper operation of the KG11-A.

Step Mode
The STEP bit is a gate, not a flip-flop. Each time it is set by a Bit Set instruction, the KG11-A performs one shift and exclusive OR.

The programmer can monitor the operation by examining the contents of the BCC register after each step and by testing the QUO bit (8) in the status register. The QUO bit is the result of the exclusive OR of the LSB Data Bit shifted out of the data register and the LSB Data Bit shifted out of the BCC register. This value is fed back and an exclusive OR is performed with bits in the BCC register as specified by the polynomial. By examining QUO and the BCC register, the programmer can determine whether the KG11-A is functioning properly.
Initialize BCC Register
To begin a new BCC accumulation, the BCC Register has to be cleared to zero. This can be done under program control by setting the CLR bit (4) at the same time (or independently) the polynomial is selected. CLR is a gate and the BCC register is reset each time CLR is set by the program.

Test for KG11-A Completion ((2) in Figure 1)
When the BCC register is cleared or a KG11-A cycle is complete, the DONE flag is set. When it is set, the contents of the BCC register can be used, or the data register can be loaded with the next character, pair of characters or word. On the flow chart (Figure 2), the DONE flag is set the first time because of the initialization in (1). Each time thereafter, it is set because a new character has been loaded into the data register and is added to the BCC accumulation.

If the programmer wishes, he does not have to test the DONE flag before proceeding. The KG11-A is fast enough to complete its cycle while the program is testing to see if there are more characters to accumulate.* The DONE flag is provided for testing purposes in case of malfunctions of the KG11-A.

* This may not be true for all PDP-11 processors.

Load Data Register With Next Character(s) ((3) in Figure 1)
The manner used to load the data register depends on the polynomial and the DDB flag. Figure 4 shows the bits that have to be loaded for each operation.

Once initialized, the act of loading the data register by a MOV(B) instruction initiates a cycle that results in the data being processed and added to the BCC accumulation in the BCC register. When shifting starts, DONE is cleared. When the shifting is complete, the data register is clear and DONE is set.

Note: The data is to be right justified in the data register. If double byte mode is used, the leading character is to be in the right byte and the trailing character in the left byte. The Data Register operation assumes the least significant bit of each byte to be to the right (low bit number of the register).

Unload BCC Register ((4) in Figure 1)
Once the CRC (or LRC) has been performed on the message, it is ready to use. If the value is the BCC of a received message, the value can be compared to the received BCC characters. In this case, the value does not have to be moved out of the register to perform the comparison. Alternatively, the received BCC may be included in the accumulation. A good BCC will result in a zero accumulation.**

** When ITB is used, the BCC that follows can be included in the accumulation. The results should be zero. If the rest of the message is accumulated without testing for zero, the only way the final BCC (after ETB or ETX) can compare is if the intermediate BCC's caused the accumulation to go to zero. This method will reduce the operations on the KG11 because the BCC does not have to be reset after the ITB, and only one loop has to be set up.
If the BCC is for a message to be transmitted, the contents of the BCC register can be moved to the message buffer for subsequent transmittal.

The format of the data in the BCC register is different for each polynomial type. The formats are displayed in Figure 5.

![BCC REGISTER](image)

* Read Only

**Applications**
The KG11-A can be used in any application where error detection and correction of serially encoded data are required. The source can be conventional communication channels, paper tapes or magnetic tape recording provided the required CRC or LRC polynomial is one of the options of the KG11-A.

**Configurations**
The number of KG11-A's required on a system will depend upon the number of messages requiring concurrent calculation of block check characters. When used in conjunction with the DU11, the following number of KG11-A's is recommended:

<table>
<thead>
<tr>
<th>Number of DU11's at 3KB</th>
<th>Number of KG11-A's</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FULL</td>
</tr>
<tr>
<td></td>
<td>DUPLEX</td>
</tr>
<tr>
<td>1-4</td>
<td>1</td>
</tr>
<tr>
<td>5-8</td>
<td>2</td>
</tr>
</tbody>
</table>

2-266
CHAPTER 3

COMPUTER SPECIAL SYSTEMS

3.1 INTRODUCTION
The following options are available from Computer Special Systems. These options are manufactured and supported by DIGITAL's CSS group.

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS11-M</td>
<td>Manual Communications Line Switch Options</td>
</tr>
<tr>
<td></td>
<td>Provides facilities for switching communication lines from one set of communication interfaces to another.</td>
</tr>
<tr>
<td>IMP11-A</td>
<td>Host to IMP Full-duplex NPR interface</td>
</tr>
<tr>
<td></td>
<td>Provides a direct connection between PDP-11 and the Interface Message Processor (IMP) used to connect Host Computers to the Advanced Research Projects Agency (ARPA) network.</td>
</tr>
</tbody>
</table>
COMMUNICATIONS LINE MANUAL SWITCH OPTIONS

GENERAL DESCRIPTION
The CS11 family of switch options provides facilities for switching communication lines from one set of communication interfaces to another. These switch options are particularly useful in multiprocessor configurations (Figure 3-1) where one computer backs up another.

![Diagram of CS11 Switch Implementation](image)

Figure 3-1 CS11 Switch Implemented in a Multiprocessor Configuration

The CS11 switches are offered for EIA standard RS-232-C, BELL TYPE 303, and four-wire 20 mA current-loop lines. These switches are compatible with either synchronous or asynchronous data lines and devices operating up to 460.8 KB/S.

An important CS11 feature is the use of special switches with bifurcated, gold-plated contacts which have been specifically designed for telephone and data line applications where maximum reliability and minimum signal degradation are important.

OPERATION
The CS11 manually operated switches are constructed from basic building block modules (48.3cm x 13.3cm) which are rack mounted in a standard 19 in. x 5 1/4 in. mounting panel. Unused space in the mounting panel is filled with blank panels.

The four wire 20 mA current loop switches have screw-type terminal blocks on the rear panel, while the EIA standard RS-232-C switches are equipped with 25 pin interface connectors. The BELL TYPE 303 switch is equipped with 12 pin coaxial connectors. The units are supplied with the appropriate additional cables to connect to user specified devices.
Environmental requirements for the CS11 switch options are the same as those specified for the PDP-11 computer system in the PDP-11 maintenance literature.

CABLES
The CS11 manual switch options are designed to connect either of two PDP-11 line interfaces to one communications terminal. The cable description for the 20 mA current loop line options (CS11-MA/MB), EIA, RS-232-C options (CS11-MC/MD), Bell Type 303 options (CS11-ME/MF) and DC14 switch (CS11-MH/MJ), are described separately in the following paragraphs.

CS11-MA/MB SWITCH OPTIONS
The CS11-MA/MB switch options for the 20 mA current loop lines are provided with three cables as shown in Figure 3.2. The 18 foot cable, terminated in a male Mate-N-Lok connector, allows this option to connect to a PDP-11 line interface. The interface can be mounted in the same or adjacent cabinet and must be terminated in a female Mate-N-Lok connector. The 2 foot (.6 m) cable allows the option to be connected to any communications terminal which is terminated in a male Mate-N-Lok connector. Therefore, with both female and male connectors available to the user, any interfaces and terminals with Mate-N-Lok connectors may be incorporated into a CS11 manual switch configuration by redirecting the existing cables. No additional or alternate cables are required.

![CS11-MA/MB Cable Connections Diagram]

**Figure 3-2 CS11-MA/MB Cable Connections**

CS11-MC/MD SWITCH OPTIONS
The CS11-MC/MD switch options for the EIA standard RS-232-C interface lines are provided with two 25-pin (female) connectors. The CS11-MC/MD female connectors mate with the EIA standard male connector DB-25S which is provided at the end of a EIA cable associated with a PDP-11 line interface. Each CS11-MC/MD option is equipped with a 25 foot (7.6 m) cable which provides the interconnection to the modem. Figure 3-3 illustrates the cable arrangement of the CS11-MC/MD options.
CS11-M

Figure 3-3 CS11-MC/MD Cable Connections

CS11-MH/MJ SWITCH OPTIONS
The CS11-MH/MJ switch options for BC14L type lines are provided with three cables shown in Figure 3-4. Two cables, terminated in male 6 pin connectors, allow the switch to be connected to DC14-CE channel interfaces. One cable, terminated in a female 6 pin connector, connects the switch with a DC14 controller interface through a BC14L cable. Four controller interfaces may be switched per CS11-MJ/MH.

Figure 3-4 CS11-MH/MJ Cable Connections

CS11-ME/MF SWITCH OPTIONS
The CS11-ME/MF switch options for Bell Type 303 lines are provided with three 12-pin (female) coaxial connectors. These connectors mate with a plug, Burndy P/N MD 12 MXP-17TC. Each CS11-ME/MF option is equipped with a 20 foot (6.1 m) cable which provides the interconnection to the modem.

3-4
CONTROLS AND INDICATORS
One manual switch is associated with each communication line controlled by the CS11 options. The switches are contained on a mounting panel located on the front of an H960 cabinet. Each CS11-MA/MB and CS11-MH/MJ option contains four switches, providing the facility to switch four communication lines. The CS11-MC/MD, CS11-ME/MF options contain one switch and control one line. The positions on all switches are marked A and B, indicating which line interface is connected to the terminal device.

PROGRAMMING
No programming procedures are associated with the CS11 manual switch options. The operator must inform the operating software of any change in the switch settings.

MAINTENANCE TESTS
No special tools or test equipment are required for maintaining the CS11 manual switch options. Margin tests are not performed on this device. Maintenance tests performed on the line interface units and the terminal devices through the CS11 switches verify the switch operation.

MAINTENANCE TECHNIQUES
If a problem develops on a communication line associated with a CS11 manual switch, check to see if the switch has the proper line interface selected and that all cables are properly installed. If the CS11 option is still suspect after making these visual checks, the switch may be removed from the communication line. The cable from the line interface under test and the cable from the communication terminal can be removed from the switch and connected directly together. If the communication device then works properly, the problem is due to the CS11 option. Performing the checkout and acceptance procedure should isolate the problem area.
IMP11-A

PDP-11 HOST TO IMP FULL DUPLEX NPR INTERFACE

NOTE
ARPANET is a U.S.A.-only research network which may be accessed only by users with U.S. Government sponsorship and approval. Therefore, the IMP11-A is available in the U.S.A. only.

GENERAL DESCRIPTION
The IMP11-A interface, provides a direct connection between PDP-11 Computer Systems and the Interface Message Processor (IMP) used to connect Host Computers to the Advanced Research Projects Agency (ARPA) network. This UNIBUS option allows the user (with addition of appropriate software) to communicate via the network with other Host systems, and is supplied with level conversion modules to connect to either the Local or Distant Host interface of network IMP's.

The IMP11-A (Figure 3-6) is supplied in a BA11-ES mounting box, complete with power supply, UNIBUS cable and Light Emitting Diode (LED) indicator panel, and includes all the logic elements required to implement the full duplex bit serial signal interchange defined for IMP to HOST connections. Diagnostic and exerciser software is also included to facilitate acceptance and maintenance procedures.

![Figure 3-6 System Block Diagram](image)

THEORY OF OPERATION
GENERAL
The IMP11-A is a PDP-11 family device for interfacing a PDP-11 to the Advanced Research Projects Agency Network (ARPANET). The IMP11-A is designed to connect to an Interface Message Processor (IMP) which is the communications processor in the ARPANET. The signalling scheme is in adherence with the specifications in the Bolt, Beranek, and Newman Report 1822, "Specifications for Interconnection of a Host and an IMP."
The interface to the UNIBUS is through 2 DR11-Bs. Associated with the DR11-B is an interface logic assembly. This logic controls the DR11-Bs, serializes and de-serializes the data, and generates the control signals required by the Host Interface in the IMP.

**INTERFACE LEVELS**
The IMP11-A is capable of operating in two modes, Local Host or Distant Host. The Local Host signals (out of the IMP) are standard TTL levels of 0 and +3 V to ground driven by high current drivers. The Distant Host signals are differential levels as follows:

<table>
<thead>
<tr>
<th>Logic 1</th>
<th>Logic 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal Line</td>
<td>+0.5 V</td>
</tr>
<tr>
<td>Pair</td>
<td>-0.5 V</td>
</tr>
</tbody>
</table>

**TRANSMIT LOGIC**
The transmit section of the interface logic assembly consists of a 16-bit shift register, a 4-bit counter, and a number of flip-flops for status and control bits.

The transmitting sequence is initiated when the GO bit is set and the DR11-B READY signal goes low. This removes the reset from the transmit logic. The READY bit going low causes a pulse on TX READY FALL and a request is sent to the DR11-B for the first word. The DR11-B performs an NPR cycle, inputting the first word from computer memory and passing it to the transmit shift register of the interface logic assembly. The data is shifted out according to the four way handshaking protocol.
of the Host Interface of the IMP.

The four way handshaking sequence associated with each data bit proceeds as follows. The assertion of Ready-for-Next-Bit (RFNB) from the Host interface in the IMP is detected in the IMP11-A and the next data bit is shifted onto the data line. After a short delay, the IMP11-A asserts There's-your-Bit (TYB). The Host interface uses this signal to strobe in the data bit and then drops RFNB. The negation of RFNB at the IMP11-A results in the dropping of TYB. The interface logic in the IMP11-A starts on the next four-transition cycle when RFNB signal is re-asserted by the Host interface.

Figure 3-8 shows a simplified diagram of this sequence.

![Four Way Handshaking Sequence Diagram](image)

Figure 3-8  Four Way Handshaking Sequence

The 4-bit counter is incremented and the shift register is shifted during each cycle. When the counter overflows, (16-bits transmitted) a new word request is given to the DP11-B and further transfers are inhibited until that word has been received from the DR11-B and loaded into the shift register.

**NOTE**

The counter is incremented by one as soon as the word is loaded, since the first bit is present on the data lines at that time.

The TX LAST WORD flip-flop is set as soon as the last word is being transmitted (indicated by the assertion of the DR11-B READY signal). On the last bit of the last word, the LAST BIT (LB) signal is transmitted along with the data if the ENABLE LAST BIT was set in the DR11-B Status register. The LAST WORD flip-flop is cleared automatically following the transmitting of this bit so that it will be initialized for the next block of data. As soon as the Last Word signal is cleared, the Reset signal is asserted and the logic is disabled until the next block transfer.
RECEIVE LOGIC
The basic operation of the receive logic is very similar to the transmit logic with several minor differences and additional features. One of the differences is the 4-bit counter starts at 0 rather than 1 because the first bit must be shifted in before it is counted.

When the Last Bit signal has been recognized by the IMP11-A logic, it is not presented to the processor as an interrupt until the word has been transferred by the DR11-B. Therefore, if it is sent before all 16-bits have been received, the interrupt will not occur until all 16 bits have been received.

If the Last Bit signal is received by the IMP11-A before a full data word has been received, the IMP11-A will fill the remainder of the shift register with 0’s to complete the word.

A relay is included in the logic to signify to the IMP that the host PDP-11 is ready. The two sides of the relay contacts are brought out to the IMP as signal lines. The normal way to implement these lines is to ground one side and sample the output of the other side. The side being sampled will then be switched between an open circuit and ground depending on the state of the relay. The relay is set by setting the HOST READY bit in the RXCSR. Naturally, if power is lost to the IMP11-A, the relay will open and indicate to the IMP that it is not ready.

A flip-flop (READY LINE ERROR) has been included in the logic to store the fact that either HOST NOT READY or IMP NOT READY has been asserted.

DR11-B LOGIC
The DR11-Bs are standard and have not been modified. Refer to the DR11-B Maintenance Manual for a thorough analysis of the DR11-B logic. Since some of the normal DR11-B signals have different names in the IMP11-A, Table 3-1 is provided to show the correlation of the standard DR11-B signal names and the names given to the signals in the IMP11-A logic.

NOTE
The protocol of the ARPANET requires that bits be shifted out by byte with the most significant bit first. Therefore, the order of shifting is bits 07, 06, 05, 04, 03, 02, 01, 00. Then bits 15, 14, 13, 12, 11, 10, 09, 08. The data lines from the DR11-B have been wired into the shift register to provide this order.

*A short jumper wire is installed on each DR11-B from E03A1 to E03C2 for noise immunity.
# IMP11-A

## Table 3-1

### IMP11-A/DR11-B Signal Names

<table>
<thead>
<tr>
<th>IMP11-A RECEIVE SECTION NAME</th>
<th>NAME IN RECEIVE DR11-B</th>
</tr>
</thead>
<tbody>
<tr>
<td>GROUND</td>
<td>C0 CONTROL H</td>
</tr>
<tr>
<td>WRITE ENABLE</td>
<td>C1 CONTROL H</td>
</tr>
<tr>
<td>RX WORD READY</td>
<td>CYCLE REQUEST AH</td>
</tr>
<tr>
<td>+3 V</td>
<td>CYCLE REQUEST BH</td>
</tr>
<tr>
<td>+3 V</td>
<td>WC INC ENB H</td>
</tr>
<tr>
<td>GROUND</td>
<td>BA INC ENB H</td>
</tr>
<tr>
<td>RX END OF MESSAGE</td>
<td>A00 H</td>
</tr>
<tr>
<td>IMP NOT READY</td>
<td>DSTAT A H</td>
</tr>
<tr>
<td>READY LINE ERROR</td>
<td>DSTAT B H</td>
</tr>
<tr>
<td>RX ATTN H</td>
<td>DSTAT C H</td>
</tr>
<tr>
<td>+3 V</td>
<td>ATTN H</td>
</tr>
<tr>
<td>RX WRITE ENABLE</td>
<td>SINGLE CYCLE H</td>
</tr>
<tr>
<td>HOST READY</td>
<td>FNCT 3 H</td>
</tr>
<tr>
<td>RX CLEAR STATUS</td>
<td>FNCT 2 H</td>
</tr>
<tr>
<td>RX INACTIVE</td>
<td>FNCT 1 H</td>
</tr>
<tr>
<td>RX CYCLE BUSY</td>
<td>READY H</td>
</tr>
<tr>
<td>RX WORD ACCEPT</td>
<td>BUSY H</td>
</tr>
<tr>
<td>RX GO H</td>
<td>END CYCLE H</td>
</tr>
<tr>
<td>RX BIT 08</td>
<td>GO H</td>
</tr>
<tr>
<td>RX BIT 09</td>
<td>NO LOCK H</td>
</tr>
<tr>
<td>RX BIT 10</td>
<td>INIT H</td>
</tr>
<tr>
<td>RX BIT 11</td>
<td>DAT15 IN H</td>
</tr>
<tr>
<td>RX BIT 12</td>
<td>DAT14 IN H</td>
</tr>
<tr>
<td>RX BIT 13</td>
<td>DAT13 IN H</td>
</tr>
<tr>
<td>RX BIT 14</td>
<td>DAT12 IN H</td>
</tr>
<tr>
<td>RX BIT 15</td>
<td>DAT11 IN H</td>
</tr>
<tr>
<td>RX BIT 00</td>
<td>DAT10 IN H</td>
</tr>
<tr>
<td>RX BIT 01</td>
<td>DAT09 IN H</td>
</tr>
<tr>
<td>RX BIT 02</td>
<td>DAT08 IN H</td>
</tr>
<tr>
<td>RX BIT 03</td>
<td>DAT07 IN H</td>
</tr>
<tr>
<td>RX BIT 04</td>
<td>DAT06 IN H</td>
</tr>
<tr>
<td>RX BIT 05</td>
<td>DAT05 IN H</td>
</tr>
<tr>
<td>RX BIT 06</td>
<td>DAT04 IN H</td>
</tr>
<tr>
<td>RX BIT 07</td>
<td>DAT03 IN H</td>
</tr>
<tr>
<td>RX BIT 08</td>
<td>DAT02 IN H</td>
</tr>
<tr>
<td>RX BIT 09</td>
<td>DAT01 IN H</td>
</tr>
<tr>
<td>RX BIT 10</td>
<td>DAT00 IN H</td>
</tr>
<tr>
<td>RX BIT 11</td>
<td>DAT15 OUT H</td>
</tr>
<tr>
<td>RX BIT 12</td>
<td>DAT14 OUT H</td>
</tr>
<tr>
<td>RX BIT 13</td>
<td>DAT13 OUT H</td>
</tr>
<tr>
<td>RX BIT 14</td>
<td>DAT12 OUT H</td>
</tr>
<tr>
<td>RX BIT 15</td>
<td>DAT11 OUT H</td>
</tr>
<tr>
<td>RX BIT 00</td>
<td>DAT10 OUT H</td>
</tr>
<tr>
<td>RX BIT 01</td>
<td>DAT09 OUT H</td>
</tr>
</tbody>
</table>

3-10
### Table 3-1 (Cont.)
**IMP11-A/DR11-B Signal Names**

<table>
<thead>
<tr>
<th>IMP11-A RECEIVE SECTION NAME</th>
<th>NAME IN RECEIVE DR11-B</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAT08 OUT H</td>
<td></td>
</tr>
<tr>
<td>DAT07 OUT H</td>
<td></td>
</tr>
<tr>
<td>DAT06 OUT H</td>
<td></td>
</tr>
<tr>
<td>DAT05 OUT H</td>
<td></td>
</tr>
<tr>
<td>DAT04 OUT H</td>
<td></td>
</tr>
<tr>
<td>DAT03 OUT H</td>
<td></td>
</tr>
<tr>
<td>DAT02 OUT H</td>
<td></td>
</tr>
<tr>
<td>DAT01 OUT H</td>
<td></td>
</tr>
<tr>
<td>DAT00 OUT H</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>IMP11-A TRANSMIT SECTION NAME</th>
<th>NAME IN TRANSMIT DR11-B</th>
</tr>
</thead>
<tbody>
<tr>
<td>GROUND</td>
<td>C0 CONTROL H</td>
</tr>
<tr>
<td>GROUND</td>
<td>C1 CONTROL H</td>
</tr>
<tr>
<td>WORD REQUEST</td>
<td>CYCLE REQUEST AH</td>
</tr>
<tr>
<td>+3 V</td>
<td>WC INC ENB H</td>
</tr>
<tr>
<td>+3 V</td>
<td>BA INC ENB H</td>
</tr>
<tr>
<td>GROUND</td>
<td>A00 H</td>
</tr>
<tr>
<td></td>
<td>DSTAT A H</td>
</tr>
<tr>
<td></td>
<td>DSTAT B H</td>
</tr>
<tr>
<td></td>
<td>DSTAT C H</td>
</tr>
<tr>
<td>TX ATTN H</td>
<td>ATTN H</td>
</tr>
<tr>
<td>+3 V</td>
<td>SINGLE CYCLE H</td>
</tr>
<tr>
<td>TX ENABLE LAST BIT</td>
<td>FNCT 3 H</td>
</tr>
<tr>
<td>TX CLEAR STATUS</td>
<td>FNCT 2 H</td>
</tr>
<tr>
<td>TX READY</td>
<td>FNCT 1 H</td>
</tr>
<tr>
<td></td>
<td>READY H</td>
</tr>
<tr>
<td>TX CYCLE BUSY</td>
<td>BUSY H</td>
</tr>
<tr>
<td>TX WORD VALID</td>
<td>END CYCLE H</td>
</tr>
<tr>
<td></td>
<td>GO H</td>
</tr>
<tr>
<td></td>
<td>NO LOCK H</td>
</tr>
<tr>
<td></td>
<td>INIT H</td>
</tr>
<tr>
<td></td>
<td>DAT15 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT14 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT13 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT12 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT11 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT10 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT09 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT08 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT07 IN H</td>
</tr>
</tbody>
</table>

3-11
IMP11-A

Table 3-1 (Cont.)
IMP11-A/DR11-B Signal Names

<table>
<thead>
<tr>
<th>IMP11-A TRANSMIT SECTION NAME</th>
<th>NAME IN TRANSMIT DR11-B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DAT06 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT05 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT04 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT03 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT02 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT01 IN H</td>
</tr>
<tr>
<td></td>
<td>DAT00 IN H</td>
</tr>
<tr>
<td>TX BIT 08</td>
<td>DAT15 OUT H</td>
</tr>
<tr>
<td>09</td>
<td>DAT14 OUT H</td>
</tr>
<tr>
<td>10</td>
<td>DAT13 OUT H</td>
</tr>
<tr>
<td>11</td>
<td>DAT12 OUT H</td>
</tr>
<tr>
<td>12</td>
<td>DAT11 OUT H</td>
</tr>
<tr>
<td>13</td>
<td>DAT10 OUT H</td>
</tr>
<tr>
<td>14</td>
<td>DAT09 OUT H</td>
</tr>
<tr>
<td>15</td>
<td>DAT08 OUT H</td>
</tr>
<tr>
<td>00</td>
<td>DAT07 OUT H</td>
</tr>
<tr>
<td>01</td>
<td>DAT06 OUT H</td>
</tr>
<tr>
<td>02</td>
<td>DAT05 OUT H</td>
</tr>
<tr>
<td>03</td>
<td>DAT04 OUT H</td>
</tr>
<tr>
<td>04</td>
<td>DAT03 OUT H</td>
</tr>
<tr>
<td>05</td>
<td>DAT02 OUT H</td>
</tr>
<tr>
<td>TX BIT 06</td>
<td>DAT01 OUT H</td>
</tr>
</tbody>
</table>

OPERATION AND PROGRAMMING
All software access to the IMP11-A logic is through the two DR11-B’s. The option appears and functions as two standard DR11-B’s with the exception of the function and status bits, which are redefined for the IMP11-A. The reader is referred to the DR11-B Maintenance Manual, which is provided with the IMP11-A, for a more thorough understanding of the standard DR11-B functions.

HARDWARE REGISTERS
The following is a list of the IMP11-A hardware registers along with their standard address assignments:

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmit Word Count Register (TXWCR)</td>
<td>172410&lt;sub&gt;8&lt;/sub&gt;</td>
</tr>
<tr>
<td>Transmit Bus Address Register (TXBAR)</td>
<td>172412&lt;sub&gt;8&lt;/sub&gt;</td>
</tr>
<tr>
<td>Transmit Command/Status Register (TXCSR)</td>
<td>172414&lt;sub&gt;8&lt;/sub&gt;</td>
</tr>
<tr>
<td>Transmit Data Buffer Register (TXDBR)</td>
<td>172416&lt;sub&gt;8&lt;/sub&gt;</td>
</tr>
<tr>
<td>Receive Word Count Register (RXWCR)</td>
<td>172430&lt;sub&gt;8&lt;/sub&gt;</td>
</tr>
<tr>
<td>Receive Bus Address Register (RXBAR)</td>
<td>172432&lt;sub&gt;8&lt;/sub&gt;</td>
</tr>
<tr>
<td>Receive Command/Status Register (RXCSR)</td>
<td>172434&lt;sub&gt;8&lt;/sub&gt;</td>
</tr>
<tr>
<td>Receive Data Buffer Register (RXDBR)</td>
<td>172436&lt;sub&gt;8&lt;/sub&gt;</td>
</tr>
</tbody>
</table>
Standard vector addresses are:

Transmit $124_8$
Receive $274_8$

**Transmit Word Count Register (TXWCR)—172410**
The TXWCR is a 16-bit Read/Write register. It is initially loaded with the 2's complement of the number of words to be transmitted and increments toward zero after each bus cycle. When the overflow occurs (all 1's to all 0's), the READY bit of the TXCSR sets, bus cycles cease, and if Interrupt Enable (bit 06 of the TXCSR) is set an interrupt is generated. TXWCR is cleared by bus INIT.

**Transmit Bus Address Register (TXBAR)—172412**
The TXBAR is a 16-bit Read/Write register. Bit 0, corresponding to Address bit A00 is set permanently to a zero. With the two Extended Memory bits in the TXCSR (XBA 16 and XBA 17), the TXBAR specifies the BUS A 17:01 lines in direct bus access. The TXBAR register is incremented by two following each bus cycle advancing the address to the next sequential word location in the UNIBUS address space. If the TXBAR overflows (all 1's to all 0's), the ERROR bit in the TXCSR sets. This error condition is cleared by loading the TXBAR or by bus INIT.

**NOTE**
The TXBAR is a word register; do not use byte instructions when loading this register.

The TXBAR is cleared by bus INIT. Overflow does not increment Extended Address bits XBA16 and XBA17. Therefore, the maximum block that can be transferred is 32K words and a block cannot be transmitted that overlaps a 32K boundary.

**Transmit Command/Status Register (TXCSR)—172414_8**
Figure 3-9 shows the TXCSR format. The significance of each TXCSR bit is described in the following paragraphs.

```
   15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
   ERROR ATTN NOT USED CYCLE IE XBA16 ENABLE LAST BIT TX CLEAR
   NEX MAINT READY XBA17 TX ERROR CLEAR TX CLEAR STATUS
```

**Figure 3-9  Transmit Command/Status Register Bit Assignments**

**ERROR (Bit-15)**—The ERROR bit is Read-Only, and specifies an error condition when:

a. The DR11-B has attempted to address Non-Existental Memory (also indicated by NEX Bit-14), or
b. The test module is not inserted in slots AB02 or CD04 of the DR11-B, or

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c. The Bus Address register (TXBAR) has overflowed by incrementing from all 1's to all 0's.

ERROR sets READY (Bit-07) and causes an interrupt if INTERRUPT ENABLE (Bit-06) is set.

The ERROR bit is cleared by removing the condition(s) that caused it to set:
- NEX is cleared by loading Bit-14 with a 0.
- Insert the test module in slot AB02 for normal operation or slot CD04 for diagnostic tests.
- Reload the Bus Address register (TXBAR).

NEX (Bit-14) — NEX is a Read/Write to 0 bit. The Non-Existent Memory condition specifies that, as UNIBUS master, the DR11-B did not receive a SSYN response within 20 μs following assertion of MSYN. NEX sets ERROR (Bit-15), READY (Bit-07), and causes an interrupt request if IE (Bit-06) has been set. This bit is cleared by INIT or by loading it with a 0. NEX cannot be loaded with a 1.

ATTN (Bit-13) — The ATTN bit is pulsed by the transmit logic to set the READY bit in the DR11-B when TX CLEAR STATUS (Bit-01) is asserted. It will cause an interrupt if IE (Bit-06) is set. This bit is a Read-Only and should normally be 0.

MAINT (Bit-12) — The MAINT bit is a Read/Write bit that is used exclusively with diagnostic program. This bit is cleared by INIT (refer to Chapter 5 in the DR11-B Maintenance Manual for further information).

Bits 09, 10, and 11 — These bits are Read-Only bits and are not used in the transmit logic.

CYCLE (Bit-08) — The CYCLE bit should not be used in the IMP11-A logic. Setting this bit while the IMP11-A is running will cause a malfunction.

READY (Bit-07) — This Read-Only bit specifies that the DR11-B is ready to accept a new command. When set, READY forces the DR11-B to release control of the UNIBUS and inhibits further DMA cycles. This bit is set by INIT, ERROR (Bit-15), or Word Count Overflow and is cleared by GO (Bit-00).

NOTE

READY must be cleared prior to initiating the block transfer. When set, READY causes an interrupt request if IE (Bit-06) has been set.

IE (Bit-06) — The IE bit (Read/Write) enables an interrupt to occur when either ERROR or READY is asserted. This bit is cleared by INIT.

XBA17, XBA16 (Bits 5 and 4) — These two Read/Write Extended Bus Address bits (17 and 16) are used with TXBAR to specify A 17:01 in direct memory transfers. XBA17 and XBA16 do not increment when the TXBAR overflows; instead, ERROR is set.
**IMP11-A**

**Bit-03—TX ERROR CLEAR**—This bit may be used to clear the READY LINE ERROR signal (RXCSR bit 09).

**ENABLE LAST BIT (Bit-02)**—When set, the IMP11-A will generate the LAST BIT signal to indicate the end of message when the word count overflows. This bit is cleared to stop the IMP11-A from signaling End of Message when transmitting multiple buffers. This bit should be set when transmitting the last buffer in the message. If the message consists of only one buffer, ENABLE LAST BIT can be set before starting transmission (setting the GO bit).

**NOTE**
The IMP11-A examines the state of this bit when the last word (Word Count Overflow) has been received from the DR11-B.

**TX CLEAR STATUS (Bit-01)**—This bit initializes the transmit logic. It should be set and cleared to initialize the IMP11-A transmit logic.

**NOTE**
Leaving this bit set will disable the transmit logic. Setting this bit will also cause the transmit DR11-B to abort any operation and set its READY bit. This bit will cause an interrupt if IE (Bit-06) is set.

**GO (Bit-00)**—The GO bit (Write-Only) causes a pulse to initiate the first DMA cycle in the block transfer. This bit always reads as a 0. When set, this bit clears READY (Bit-07).

**Transmit Data Buffer Register (TXDBR)—172416<sub>8</sub>**
The TXDBR serves as temporary storage register in the DR11-B to hold the word being transferred under program control. There should be no need for access to this register in the IMP11-A.

**Receive Word Count Register (RXWCR)—172430<sub>8</sub>**
The function of the RXWCR is equivalent to the TXWCR.

**Receive Bus Address Register (RXBAR)—172432<sub>8</sub>**
The function of the RXBAR is equivalent to the TXBAR.

**Receive Command/Status Register (RXCSR)—172434<sub>8</sub>**
Figure 3-10 shows the RXCSR format. The significance of each RXCSR bit is described in the following paragraphs.

**ERROR (Bit-15)**—The ERROR bit is Read-Only, and specifies an error condition when:

- a. The DR11-B has attempted to address non-existent memory (also indicated by NEX Bit-14), or
- b. The test module is not inserted in slot AB02 or CD04 of the DR11-B, or
- c. The Bus Address register RXBAR has overflowed by incrementing from all 1's to all 0's.
Figure 3-10  Receive Command/Status Register Bit Assignments

ERROR sets READY (Bit-07) and causes an interrupt if INTERRUPT ENABLE (Bit-06) is set.

The ERROR bit is cleared by removing the condition(s) that caused it to set:

a. NEX is cleared by loading Bit-14 with a 0.
b. Insert the test module in slot AB02 for normal operation or slot DC04 for diagnostic tests.
c. Reload the Bus Address register RXBAR.

NEX (Bit-14)—NEX is a Read/Write to O-bit. The Non-Existent Memory condition specifies that, as UNIBUS master, the IMP11-A did not receive a SSYN response within 20 µs following assertion of MSYN. NEX sets ERROR (Bit-15), READY (Bit-07), and causes an interrupt request if IE (Bit-06) has been set. This bit is cleared by INIT or by loading it with a 0. NEX cannot be loaded with a 1.

ATTN (Bit-13)—This Read/Only bit is pulsed by the IMP11-A when the Last Bit signal has been received from the IMP. ATTN causes an interrupt if INTERRUPT ENABLE (Bit-06) is set. The ERROR bit will not be set and END OF MSG (Bit-11) will be set when the last bit has been received. The ATTN Bit is also pulsed by the receive logic to set the DR11-B READY Bit when RX CLEAR STATUS is asserted.

MAINT (Bit-12)—The MAINT bit is a Read/Write bit that is used exclusively with diagnostic programs and is cleared by INIT (refer to Chapter Five in the DR11-B Maintenance Manual for further information).

END OF MSG (Bit-11)—This bit indicates that the Last Bit signal has been received from the IMP which signifies the end of a message. Cleared by RX CLEAR STATUS (Bit-01) or GO (Bit-00).

IMP NOT READY (Bit-10)—When set, this bit indicates that the IMP is not ready.

READY LINE ERROR (Bit-09)—When set, this bit indicates that either HOST READY is not set or IMP NOT READY has been set. Cleared by RX CLEAR STATUS (RXCSR Bit 01) or TX ERROR CLEAR (TXCSR Bit 03).
CYCLE (Bit-08)—The CYCLE bit is not used in the IMP11-A and should be ignored. Setting this bit while the IMP11-A is running will cause a malfunction.

READY (Bit-07)—The READY bit (Read-Only) specifies that the DR11-B is ready to accept a new command. When set, READY forces the DR11-B to release control of the UNIBUS and inhibits further DMA cycles. This bit is set by INIT, ERROR (Bit-15), or Word Count Overflow and is cleared by GO (Bit-00).

**NOTE**
READY must be cleared prior to initiating the block transfer. When set, READY causes an interrupt request if IE (Bit-06) has been set.

IE (Bit-06)—The IE bit (Read/Write) enables an interrupt to occur when either ERROR or READY is asserted. This bit is cleared by INIT.

XB17, XB16 (Bit 05 and 04)—These two Read/Write Extended Bus Address bits (17 and 16) are used with RXBAR to specify A 17:01 in direct memory transfers. XBA17 and XBA16 do not increment when RXBAR overflows; instead, ERROR (Bit-15) is set.

RX WRITE ENABLE (Bit-03)—This Read/Write bit must be set for proper operation of the receive logic. If this bit is not set, the IMP11-A will effectively discard any data that is received although it will otherwise appear to operate normally.

HOST READY (Bit-02)—This Read/Write bit when set, indicates to the IMP that the host is on-line and ready. Cleared by INIT.

RX CLEAR STATUS (Bit-01)—Initializes the receive logic. This bit should be set and then cleared to initialize the logic.

**NOTE**
Leaving this bit set will disable the receive logic. Setting this bit will cause the receive DR11-B to abort any operation and set it's READY bit. If IE (Bit-06) is set, RX CLEAR STATUS will cause an interrupt.

GO (Bit-00)—This Write-Only bit causes a pulse to initiate the first DMA cycle in the block transfer. GO always reads as a 0. When set, this bit clears READY (Bit-07).

Receive Data Buffer Register (RXDBR)—1724368
The RXDBR serves as a temporary storage register in the DR11-B to hold the work being transferred under program control. There should be no need to access this register in the IMP11-A.

**INDICATORS**
Figure 3-11 shows the 12 indicators that are mounted on the IMP11-A front Indicator Panel.
The indicators, TX DATA, TX TYB, and TX RFNB represent the current state of the Data, Ready-for-Next-Bit and There’s-your-Bit signals respectively between the host and IMP.

The indicators IMP NOT READY and HOST NOT READY reflect the state of the Ready signals in both the IMP and host. The normal condition for these lights is that both should be OFF. If either of these lights is ON, it indicates an abnormal condition in either the host or the IMP.

The two READY indicators reflect the state of the DR11-B READY signals. These lights will be OFF during DMA transfers and will be ON when the respective DR11-B is idle.

**PROGRAMMING EXAMPLE**

The following example shows the programming steps necessary to transmit a block of 500 words. The IMP11-A should be initialized on START UP by toggling the two CLEAR STATUS bits.

**TRNSMT:**
MOV #TXBUF, TXBAR; Set up Bus Address
MOV #500., TXWCR; Set up word count
MOV #4, TXCSR; Set Enable Last Bit
BIS #101, TXCSR; Set TX GO and INT Enable.

**TXBUF:** (500 words of data)

114: Transmit Interrupt Service Address
116: and Processor Status Word

The following example shows the programming steps necessary to receive a 500 word (or less) message:
IMP11-A

MOV #RXBUF, RXBAR; Set RX Bus Address
MOV #500., RXWCR; Set RX Word Count
MOV #14, RXCSR; Set host ready, write enable
BIS #101, RXCSR; Set RX GO and Interrupt Enable

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RX Interrupt Service routine address and Processor Status Word
126

The above program for receiving will cause an interrupt whenever 500 words of data have been received and/or the Last Bit signal is received.

NOTE
Using a BIS instruction to set any bit in the DR11-B Status register after the IMP11-A is running can inadvertently clear the CYCLE bit and cause a malfunction. Therefore, if it is necessary to reference the Status register after the IMP11-A is running, use a byte instruction. This restriction applies only when the IMP11-A has started performing data transfers (READY bit clear).

CABLES
Various system cables are described in the following paragraphs.

UNIBUS Cables
Connection between the IMP11-A and the PDP-11 UNIBUS is by means of standard PDP-11 UNIBUS Cables (BC11A). An M920 Jumper card is provided for the UNIBUS connection between the two DR11-B’s within the IMP11-A. The input bus cable (processor side) connects to slots AB01 in the DR11-B in the front of the mounting box and the output bus cable connects to slots AB04 in the second DR11-B.

NOTE
It was not intended for any other devices to be housed in the BA11-ES Mounting Box with the IMP11-A, therefore UNIBUS connections were not provided in the other two System Units. If it is essential to mount another UNIBUS device in this box, a short length of bus cable must be used to connect it to the DR11-B’s located in the front of the box.

Signal Cable
A signal cable is not provided with the IMP11-A, the user must provide this cable which connects the IMP11-A to the IMP. The end of this cable which attaches to the IMP11-A should be connected to the M908 cable connector which is provided and is organized as follows:

3-19
<table>
<thead>
<tr>
<th>SIGNAL NAME*</th>
<th>SIGNAL PIN</th>
<th>SIGNAL GROUND PIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ready-for-next-host-bit</td>
<td>N1</td>
<td>N2</td>
</tr>
<tr>
<td>(TX RFNB)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>There’s-your-host-bit</td>
<td>P1</td>
<td>P2</td>
</tr>
<tr>
<td>(TX TYB)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data: Host to IMP</td>
<td>S1</td>
<td>S2</td>
</tr>
<tr>
<td>(TX Data)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Last Host bit</td>
<td>R1</td>
<td>R2</td>
</tr>
<tr>
<td>(TX LB)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ready-for-next-IMP-bit</td>
<td>H1</td>
<td>H2</td>
</tr>
<tr>
<td>(RX RFNB)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>There’s-your-IMP-bit</td>
<td>D1</td>
<td>D2</td>
</tr>
<tr>
<td>(RX TYB)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data: IMP to host</td>
<td>F1</td>
<td>F2</td>
</tr>
<tr>
<td>(RX Data)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Last IMP bit</td>
<td>E1</td>
<td>E2</td>
</tr>
<tr>
<td>(RX LB)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IMP master ready</td>
<td>L1</td>
<td></td>
</tr>
<tr>
<td>IMP Ready test</td>
<td>L2</td>
<td></td>
</tr>
<tr>
<td>Host Master Ready</td>
<td>J1</td>
<td></td>
</tr>
<tr>
<td>Host Ready Test</td>
<td>J2</td>
<td></td>
</tr>
<tr>
<td>Shield Ground</td>
<td>C2</td>
<td></td>
</tr>
</tbody>
</table>

*The signal names shown correspond to the names used in BB + N Report #1822. Shown in parenthesis are the corresponding signal names in the IMP11-A.

The signal cable connects to slot F04 of the interface logic for local host operation and slot E04 for distant host operation. The two slots are pin compatible and no change in the signal cable should be required to convert from local host to distant host operation. Figure 3-12 shows a simplified schematic of a typical signal to illustrate the relationship of the two connector slots.

NOTE

The distant and local transmit (host to IMP) signals do not interfere but the distant and local receive signals will interfere in Local Host Mode unless the Differential Receiver Module is removed.

Further specifications for construction of the interface cable can be found in Bolt, Beranek, and Newman report #1822, “Specifications for the Interconnection of a Host and an IMP.”

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Internal Cabling
A short length of ribbon cable is used to connect the LED indicators on the front panel to the Indicator cable (slot D04) in the IMP11-A logic.

A short UNIBUS Cable is used to connect the first DR11-B to the IMP11-A transmit logic. Another short UNIBUS cable is used to connect the second DR11-B to the IMP11-A receive logic. These cables are supplied with the IMP11-A.

GROUNDING
The IMP11-A should be grounded to the processor system ground with the ground strap provided. In Local Host Mode, the IMP and the PDP-11 processor should contain a high quality connection between each other.

SYSTEM CONSIDERATIONS
The maximum transfer rate of the IMP11-A is controlled by the frequency of the M401 Variable Clock in slot F01. IMP11’s are shipped from the factory with the clock set for 5 MHz which results in a transfer rate of
IMP11-A

approximately 500,000 bits/second or 31,250 words/second. The transfer rate can be slowed down by adjusting the clock if necessary.

Since the IMP11-A is completely asynchronous, it can be placed in any position on the UNIBUS without incurring latency problems.

SPECIFICATIONS

Mechanical:
Mounting Box One, type BA11-ES
Dimensions 10\(\frac{1}{2}\) in. h, x 19 in. w, x 24 in. d (26.7 cm. x 48.3 cm. x 61 cm)
Weight 130 lbs (58.9kg)
Prerequisites None

Electrical:
Input Power 120 Vac +/− 10%, 47-63 Hz
Power Supply One, type H720-E
Logic M-series modules, TTL levels

Operational:
Capacity One IMP host interface
Transfer Full duplex, NPR
Unibus Loads Two
Data Rate Nominal 500,000 bits/sec., full duplex
Interrupt Receive Section:
1) Receipt of LAST BIT from IMP
2) Receive word count overflow
Transmit Section:
1) Word count overflow

Output Levels Local host—single ended 0 Vdc to 5 Vdc
Distant host—differential +/− 1.0 Vdc

Signalling Bit asynchronous with request/acknowledge handshake per bit

Indicators 12 front panel Light Emitting Diodes displaying major IMP11-A functions

Cabling Connector only supplied for terminating customer supplied IMP-HOST cable