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peripherals

handbook

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CHAPTER 1

INTRODUCTION

DIGITAL's family of PDP-11 processor peripherals is continually growing to provide you with the PDP-11 hardware that most precisely meets your needs. Cost effectiveness, capacity, ease of use and reliability are constantly being improved and upgraded. At the same time, older peripherals receive the same care and respect due to DIGITAL's family product tradition of longevity and stability. Peripherals development occurs along the full range of customer needs. For example, this handbook edition includes descriptions of four new or upgraded card readers, as well as of ten new disks.

Because of the growing selection of DIGITAL peripherals, the traditional Peripherals Handbook has been divided into two books. The **Terminals and Communications Handbook** describes DIGITAL's terminals and communications equipment. This **Peripherals Handbook** describes the bootstrap, disks, line printers, magnetic tapes, paper tapes and sensor I/O devices. A final chapter, Systems Options, describes other PDP-11 devices, such as expander boxes and UNIBUS switches.

These devices are discussed by chapter, with the specific peripherals described within the chapter in alphabetical and alphanumeric order. For example, Chapter 6 is Magnetic Tapes; within the chapter the tapes are described in the following order:

- **TE10**—7- or 9-track, 45 inches per second, 800 bits per inch tape
- **TE16**—9-track, 45 inches per second, 800 or 1600 bits per inch tape
- **TS03**—9-track, 12½ inches per second, 800 bits per inch tape
- **TU45**—9-track, 45 inches per second, 800 or 1600 bits per inch tape
- **TU58**—cartridge tape with 114 megatype storage per cartridge
- **TU60**—reel to reel cassette tape

The description of each peripheral device includes: a section listing the outstanding features, a paragraph or two presenting general information about the device and its uses, a section containing register and bit information, and a section on device specifications. The specification information is subject to change, and
INTRODUCTION

should be considered as a guide only. For specific site or interfacing information, consult your local DIGITAL sales office.

Appendix A lists the UNIBUS addresses and vectors of DIGITAL's peripherals. Appendix B lists the specifications for supported peripherals.

When you purchase a peripheral device, you will receive detailed user and maintenance documentation. DIGITAL also publishes excellent tutorial guides to DIGITAL software languages and operating systems. The Education Services group at DIGITAL has developed a wide variety of hardware and software courses specifically designed to answer customer's needs.

The PDP-11 Processor Handbook describes the UNIBUS members of the PDP-11 family. It explains the PDP-11 instruction set, the UNIBUS, and describes programming techniques with examples.

The PDP-11 Software Handbook describes the 11 family of operating systems and languages.

The VAX Software, Architecture and Processor Handbooks fully describe DIGITAL's VAX system and software.

As an addition to DIGITAL's standard products, the Computer Special Systems group provides unique hardware and software solutions to meet specific customer's needs. Products of this group are identified in this handbook by a CSS designation under the specification section.
CHAPTER 2
BOOTSTRAP

M9312

The M9312 is DIGITAL's new UNIBUS bootstrap module, designed to support the extended contemporary family of UNIBUS peripherals.

FEATURES

- supports all devices previously booted from the M9312 as well as the newer devices
- capable of providing bootstrap support for new peripherals as they are introduced
- configuration flexibility

DESCRIPTION

The M9312 Bootstrap/Terminator module contains a complete set of UNIBUS termination resistors along with 512 words of read-only memory that can be used for diagnostic routines, the console emulator routine, and for bootstrap programs.

Five sockets on the M9312 allow you to interchange ROMs, enabling you to use the module with any UNIBUS PDP-11 system and to boot any peripheral device simply by adding or changing ROMs. One socket is used solely for a diagnostic ROM (PDP-11/60 and 11/70 systems), or for a ROM that contains the console emulator routine and diagnostics for all other PDP-11 systems. The other four sockets accept ROMs that contain bootstrap programs. One or two bootstrap programs may be contained in a particular ROM; however, some devices may require two or more ROMs to contain their particular bootstrap programs.

Diagnostics, bootstrap programs, and the console emulator routine are all selectable through the address offset switch bank on the M9312.

The following table lists the devices supported by the various models of the M9301 bootstrap and by the M9312 bootstrap.
### Supported by: M9301—M9312

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### Specifications

**Physical**
- Double height extended 21.6 × 14 cm (8 1/2 in. × 5 1/2 in.)

**Electrical**
- +5VDC ± 5%
- 1.5A typical (3A maximum)
CHAPTER 3
CARD READERS

CD11

DESCRIPTION
The CD11 is a high-speed card reader that can process punched cards at up to 1200 cards/minute. There are two versions: a tabletop unit with an input hopper capacity of 1000 cards that operates at a rate of 1000 cards/minute and a free-standing floor model with a large 2250-card hopper that has a processing speed of 1200 cards/minute. The Control Unit is a set of modules mounted in a System Unit (SU) assembly.

The CD11 Card Readers access the PDP-11 UNIBUS from the interrupt and non-processor request (NPR) modes of operation. Control and status information is relayed in the interrupt mode. Data is transferred through direct memory access (NPR).

The Card Reader design helps prevent card jams and keeps card wear to a minimum. Readers have a high tolerance to cards that have been nicked, warped, bent or subjected to high humidity.

To keep cards from sticking together, the readers use a special "riffle air" feature, the bottom half inch of cards in the input hopper is subject to a stream of air which separates the cards and air cushions them from the deck and from each other.

Cards entering the reader are selected through a vacuum picker. The picker and its associated throat block prevent the unit from
accepting cards that have been stapled or taped together (unless such taping is on the leading edge). Because the card track is very short, only one card is in motion at a time. This minimizes the chances of cards jamming; stoppages are also reduced since the reader automatically makes six attempts to process a card before rejecting it.

The read station uses infrared light-emitting diodes (LEDs) as its light source and phototransistors as its sensors. No adjustments are required during the ten-year life expectancy of the diodes.

Because card reader operation is flexible, cards can be loaded and unloaded while the reader is operating. A switch may be set to provide system blower shutdown or continual running after the last card has been read. Automatic shutdown reduces computer room noise level and indicates that the card hopper is empty.

A control unit is included with the card reader.

DATA FORMATS
The reader is designed to sequentially look for data in 80 columns, starting with column number 1. Each column has 12 zones, or rows. A hole or mark is interpreted as a binary one, and the absence of a hole or mark as a binary zero. Data is read from the card one column at a time.

There are two data formats for input to the computer:

Non-Compressed Mode: A separate bit in the data register is used to record the state of each card zone. The 12-zone bits correspond to bits 00 through 11 of the PDP-11 word. Bits 12 thru 16 of the PDP-11 word are used for special error and data packing information.

Compressed Mode: The 12-zone bits are encoded into 8 bits, to fit in a PDP-11 byte (8 bits). More efficient data storage is achieved in this mode. All present Hollerith Codes (the standard used for 12-zone card data), and their proposed expansion, can be accommodated with the compressed format.

The CD11 has 4 registers: Status, Column Count, Bus Address, and Data. A bit within the Status Register is set or cleared under program control to cause the Data Register to hold either the non-compressed or compressed format.
REGISTERS
Status and Control Register (CDST) 777 160

Effect of the Initialize (INIT) signal: clear bits 15 to 13, 11 to 9, 6 to 3, 1, and 0.
Read only: bits 15 through 9, 7, 3, and 2
Write only: bits 8 and 0

Bit: 15  Name: Error (ERR)
Function: Set to indicate an error condition that is the inclusive OR of all error conditions (bits 14-9 in this register).
If the error condition is due to bit 11, 10, or 9, the Error bit does not set until the Busy signal from the Card Reader is cleared. This permits the entire card to pass through the read station before an interrupt occurs.

Bit: 14  Name: Reader Check
Function: Set when an abnormal condition exists in the card reader. Any one of the following four conditions sets this bit:
Hopper Check: input hopper is empty or the output stacker is full. This error indication occurs after column 80 of the last card has been read.
Pick Check: feed mechanism failed to deliver a card to the read station when demanded. This error condition occurs if a card is not delivered within 400 ms after a Read command is initiated.
Stack Check: previous card was not properly seated in the output stacker and may be badly damaged.
Read Check: read station electronics do not agree with the usual light and dark areas of the card. This could
be caused by torn cards or cards with illegal punches (holes in the 0 or 81st column positions).

Error-causing condition should be corrected before clearing this bit.

**Bit: 13**  
**Name:** End of File (EOF)  
**Function:** Used with CD11-E only. Associated with the END OF FILE pushbutton on that reader.

The END OF FILE pushbutton is used as a programming aid to allow the user to insert an END OF FILE flag at the appropriate place in the program.

When the last group of cards in a specific file has been loaded into the hopper, the user can then depress the END OF FILE switch. When the switch is depressed, the card reader functions in a normal manner until the input hopper is empty and the last card is read. At this time, the card reader HOPPER CHECK indicator light comes on and the controller END OF FILE bit (bit 13) is set. Because a hopper-empty condition is considered an error, the status register Reader Check, Hopper Check, and Error bits are also set.

When a CD11-A is used, bit 13 is always clear.

**Bit: 12**  
**Name:** Off-Line  
**Function:** Set when the reader is off-line. When clear, the reader is on-line, under program control and ready to accept a Read command.

Depressing the card reader RESET switch brings the reader on-line, provided no error conditions exist and the reader MODE switch is in the REMOTE position.

The card reader goes off-line (setting bit 12) whenever an error condition is sensed (STOP light on reader is lit), the reader STOP pushbutton is depressed, or the MODE switch is set to the LOCAL position.

**Bit: 11**  
**Name:** Data Error  
**Function:** When the controller is in the packing mode of operation (bit 1 set), the normal 12-bit code is compressed into an 8-bit code that allows a column to be transferred as a single byte. When this compressed code is used, card zones 1-7 are represented by an octal code. Therefore, no more than one zone should be at 1 at any given time. Bit 11 is set in the packing mode whenever more than one of zones 1-7 are a 1.
When set this bit does not inhibit further transfer of data into memory.

**Bit: 10  Name: Data Late**

**Function:** Set when NPR request is not granted during the time that data is guaranteed valid from the Card Reader. This bit prevents further NPR requests from occurring, thereby preventing clocking of the column-count register (CDCC) and current address register (CDBA).

**Bit: 9  Name: Non-Existent Memory**

**Function:** If the controller is engaged in a NPR data transfer and attempts to access a memory address that does not exist, bit 9 sets to provide an NXM error indication. This NXM error occurs if the controller does not receive SSYN within a specified amount of time after it has issued MSYN.

When set, this bit inhibits further NPR requests.

**Bit: 8  Name: Power Clear (PWR CLR)**

**Function:** Set to clear the column-count register (CDCC), the current address register (CDBA), and all bits in the status register (CDST) with the exception of bits 12, 7 and 2.

**Bit: 7  Name: Ready (RDY)**

**Function:** Set when the CD11 is ready to receive a new command. This bit is set by one of the following conditions:
- Error bit set: an error condition exists and the program should branch to an error-handling routine.
- Power Clear bit set: all controller logic has been cleared and the controller can engage in a data transfer.
- INIT signal occurs: same as POWER CLEAR.
- Busy clear and CDCC overflow: the present number of data transfers has been performed and the controller is now ready for a new Read command.

**Bit: 6  Name: Interrupt Enable (INT ENB)**

**Function:** Set to allow either Ready or Reader transition to On Line = 1 to cause an interrupt.

**Bit: 5-4  Name: Extended Bus Address (XBA17, XBA16)**

**Function:** Used to specify bus address lines (17 and 16) in direct memory transfers. Increment with the current address register (CDBA).

Bit 5 corresponds to XBA17; bit 4 to XBA16.
**Bit: 3**  
**Name:** Reader Transition to On Line (ON LINE TRANS)  
**Function:** Set when the card reader has gone on-line and is under program control. Depressing the card reader RE-SET switch brings the reader on-line, provided no error conditions exist and the reader MODE switch is in REMOTE.

The card reader goes off-line whenever an error condition is sensed or when the STOP switch is depressed.

**NOTE**  
The READER TRANSITION TO ON-LINE bit does not clear when the reader goes off-line.

**Bit: 2**  
**Name:** Hopper Empty  
**Function:** Set to indicate that either the input hopper is empty or the output stacker is full. The bit will set Reader Check (bit 14) and is cleared by correcting the condition that caused the error. Because the bit is controlled by the HOPPER CHECK signal from the card reader, it will not be cleared by Power Clear.

**Function:**  
**Name:** Data Packing

**Bit: 1**  
Determines whether the data is to be loaded as a 12-bit word or as a 8-bit byte. 0 = 12-bit word, 1 = 8-bit byte.

**NOTE**  
This bit has no effect on data read from the processor.

**Bit: 0**  
**Name:** Read  
**Function:** Set to cause the card reader feed mechanism to deliver one card to the read station for reading.

When set, this bit clears bits 15, 14, 11, 10, 9, 7, and 3 in the status register.

The bit also clears Error (bit 15) provided Hopper Check (bit 2) is clear.

If the Read bit is set when the Card Reader is busy, it will reset bits 15 and 2. Error is set to indicate that a Read command was issued when the card reader was not available for use.

**Column Count Register (CDCC) 777 162**

**Bit: 15-0**  
**Name:** Column Count
Function: Contains the 2s complement of the number of columns to be transferred to memory when cards are being read.

The column-count register is loaded prior to the initiation of the read function. The register is incremented by 1 after each transfer. When the contents of the register equal all 0s, further transfers are inhibited until another READ command occurs.

If an entire 80-column card is read and the column-count register has still not advanced to 0, then the next card is automatically fed to the read station.

All bits may be loaded or read by the program, and cleared by POWER CLEAR (bit 8 in the status register set) or INIT.

NOTE
The column-count register should not be modified by using byte instructions. Use only word instructions when loading this register. The register is wired in such a manner that the entire word is loaded even if a byte instruction is used. Therefore, if the programmer attempts to load only the low-order byte, the data on the high-order lines is also loaded. This latter data may be useless and/or unknown to the programmer.

Whenever the column-count register reaches 0, an interrupt is initiated if INT ENB is set to inform the processor that the desired number of columns has been transferred.

Current Address Register (CDBA) 777 164

Bit: 15-0  Name: Address
Function: These bits specify the bus or memory address into which the next column or data is to be stored.

The current address register is initially set to the memory location of the first column to be read. It then increments by 1 for transfers in the packing mode (byte transfers) and increments by 2 for transfers in the non-packing mode (word transfers). Incrementation occurs immediately after each data transfer.

The bits in this register are used in conjunction with
extended address bits A17 and A16 (bits 5 and 4, respectively, in the status register so that 18-bit memory addresses may be used.

Note that the extended address bits participate in the incrementation; they are a logical extension of this register.

The current address register is loaded prior to issuing a READ command. This register may be loaded or read by the program.

Cleared by POWER CLEAR (bit 8 in the status register set) or by INIT.

**NOTE**
The current address register should not be modified by using byte instructions. Use only word instructions when loading this register.

Data Buffer and Second Status Register CDDB 777 166
(Non-Packing Mode)

**Bit: 15**  **Name:** DATA ERROR

**Function:** A DATA ERROR from 1 occurs (bit 15 sets) whenever more than one of zones 1-7 are a 1.

When bit 15 sets it does not inhibit further transfers of data into memory; it also does not set bit 15 of CDST (ERROR BIT).

Read-only during DMA (NPR) transfer periods.

**Bit: 14-12**  **Name:** PACKED BITS (Zones 1-7)

**Function:** Bits 14 through 12 represent an octal code that defines the card zones as shown below. In the case of multiple zones, these bits are the inclusive OR of the octal codes of the zones.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Card Zone</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>13</td>
<td>12</td>
<td>zero, ZONES 1-7</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ZONE 1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>ZONE 2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>ZONE 3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ZONE 4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>ZONE 5</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>ZONE 6</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>ZONE 7</td>
</tr>
</tbody>
</table>

All bits are read-only DMA (NPR) transfer periods.
**CARD READERS**

**CD11**

**Bit: 11-0  Name: Zone**

**Function:** These bits represent the output of a 12-bit data buffer register. When the register is in a non-packing mode (bit 1 in the status register is clear), data from a card is loaded into this buffer one column at a time on a word basis. After each column is loaded, the contents of the buffer is placed on the UNIBUS for transfer to the processor, memory or other bus device.

The contents of the buffer is coupled to the 12 least-significant bus data lines as shown below:

<table>
<thead>
<tr>
<th>Bit</th>
<th>ZONES 0-9, respectively</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>ZONE 11</td>
</tr>
<tr>
<td>10</td>
<td><strong>Corresponding Card Image</strong></td>
</tr>
<tr>
<td>9-0</td>
<td>ZONE 12</td>
</tr>
</tbody>
</table>

Bits 11-0 are read as is whenever a card is not being read; bits 15-12 are always read as 0s.

**Data Buffer and Second Status Register CDDB 777 166**

**(Packing Mode)**

**Bit: 7-0  Name: Zone**

**Function:** These bits also represent the output of the data buffer register. During a read operation, data from a card is loaded into this buffer one column at a time. After each column is loaded, the contents of the 12-bit buffer are compressed into an 8-bit character by an encoding network and are then gated onto the UNIBUS as a low-order byte. This data compression is made available so that the card reader controller is fully compatible with the proposed expansion of the Hollerith code.

Bits 7 through 3 are encoded as follows:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Corresponding Card Image</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ZONE 12</td>
</tr>
<tr>
<td>6</td>
<td>ZONE 11</td>
</tr>
<tr>
<td>5</td>
<td>ZONE 0</td>
</tr>
<tr>
<td>4</td>
<td>ZONE 9</td>
</tr>
<tr>
<td>3</td>
<td>ZONE 8</td>
</tr>
</tbody>
</table>
CARD READERS

CD11

Bits 2 through 0 represent an octal code that defines the card zone as shown below. In the case of multiple zone, these bits are the inclusive OR of the octal codes of the zones.

<table>
<thead>
<tr>
<th>Bit 02</th>
<th>Bit 01</th>
<th>Bit 00</th>
<th>Card Zone</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>zero, ZONES 1-7</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>ZONE 1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>ZONE 2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>ZONE 3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ZONE 4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>ZONE 5</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>ZONE 6</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>ZONE 7</td>
</tr>
</tbody>
</table>

All bits are read-only bits with the same conditions as described previously.

Data Buffer and Second Status Register When Used as Second Status Register CDDB 777 166

During non-data transfer periods (READY bit in the CDST set) the CDDB is used as a Second Status register containing additional status information from the reader. The bits are defined as follows:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>DATA ERROR from 1. Should always be set.</td>
</tr>
<tr>
<td>14</td>
<td>READ CHECK—read station electronics do not agree with the usual light and dark areas of the card. This could be caused by torn cards or cards with illegal punches (holes in the 0 or 81st column positions).</td>
</tr>
<tr>
<td>13</td>
<td>PICK CHECK—feed mechanism failed to deliver a card to the read station when demanded. This error condition occurs if a card is not delivered within 400 ms after a Read command is indicated.</td>
</tr>
<tr>
<td>12</td>
<td>STACK CHECK—previous card was not properly seated in the output stacker and may be badly damaged.</td>
</tr>
<tr>
<td>11-0</td>
<td>If READER is on-line (off-line bit in CDST CLEAR), these bits represent data lines 11-0 outputs from the READER. They should always be set. If any are not set, then that data line from the READER is defective.</td>
</tr>
</tbody>
</table>
NOTE
A few early model CD11 Controllers with wire lists prior to rev J do not have the Second Status register and do not use bits 15-12 of the Data Buffer register. These controllers are ones purchased before January 1, 1976. For these controllers, bits 15-12 are always read as zero and bits 11-00 are always read as data bits from the card reader whenever the Data Buffer register is selected.

SPECIFICATIONS FOR CD11-A, CD11-E AND CD11-F
(Specifications for all three are the same except where noted)

Main Specifications
Input medium: 80-column punched cards, 12 zones (or rows)
Speed:
   CD11-A 1000 cards/minute
   CD11-E 1200 cards/minute
   CD11-F 285 cards/minute
Hopper capacity:
   CD11-A 1000 cards
   CD11-E 2250 cards
   CD11-R 550 cards

Register Addresses
Status and Control: CDST 777 160
Column Count: CDCC 777 162
Current Address: CDBA 777 164
Data: CDBB 777 166

UNIBUS Interface
Interrupt vector address: 230
Priority level: BR4
Data transfer: NPR
Bus loading: 1 bus load

Mechanical
Mounting:
   CD11-A 1 table top unit + 1 system unit
   CD11-E 1 free-standing unit + 1 system unit
   CD11-F 1 table top unit + 1 system unit
CARD READERS

CD11

Size:
CD11-A 14” H x 24” W x 18” D
CD11-E 38” H x 24” W x 38” D
CD11-F 11” H x 19” W x 14” D

Weight:
CD11-A 85 lbs.
CD11-E 200 lbs.
CD11-F 60 lbs.

Power

Running current:
CD11-A 6A at 115 VAC
CD11-E 10A
CD11-F 5A

Starting current:
CD11-A 15A at 115 VAC
CD11-E 22A
CD11-F 4A

Current for control: 2.5A at +5V

Heat dissipation:
CD11-A 600 W
CD11-E 1150 W
CD11-F 570 W

Environment

Operating temperature: 15° C to 32° C
Relative humidity: 20% to 80%

Models

CD11-A: Card reader and control, 1000 cards/min, 115 VAC, 60 Hz
CD11-B: Card reader and control, 1000 cards/min, 230 VAC, 50 Hz
CD11-EA: Card reader and control, 1200 cards/min, 115 VAC, 60 Hz
CD11-EB: Card reader and control, 1200 cards/min, 230 VAC, 50 Hz
CD11-FA: Card reader and control, 285 cards/min, 115 VAC, 60 Hz
CD11-FB: Card reader and control, 285 cards/min, 230 VAC, 50 Hz
CARD READERS

CMS11-J, CMS11-H

The CMS11-J and CMS11-H Card Reader systems read 80-column Hollerith data cards at rates of up to 300 cards per minute (CMS11-H) and of up to 600 cards per minute (CMS11-J).

FEATURES

• programmed in the same manner as the CR-11 (software compatible)
• low cost
• reliable

DESCRIPTION

The CMS11-J and CMS11-H Card Reader systems are identical, except for their operating speeds. Each is equipped with a twin read head and will read both punch and mark-sense (with or without timing marks) cards.

The controller that interfaces the card reader to the UNIBUS is a single quad module that occupies one of the four slots in the PDP-11 processor system unit.

The CMS11-J and CMS11-H systems operate in one of four modes: punch, punch with timing marks, mark-sense, and mark-sense without timing marks. After the operating mode has been selected, the system operates in the same manner as the CR11.

SPECIFICATIONS

Controller

Mechanical:
Logic Mounting
Dimensions
Mounting Prerequisite

One quad height board (M8291)
8 1/2 in. h, 12 in. w, 5/8 in. d
One available SPC slot or equivalent

Electrical:
Logic Power
Module Type
Logic Levels

1.5 A @ +5V (derived from the power supply in the mounting box where the controller is installed)
M-Series
TTL
CARD READERS

CMS11-J, CMS11-H

Operational:

Registers
- Status Register (CRS)
- Data Buffer Register (CRB1)
- Data Buffer Register Encoded
- Output (CRB2)
- Maintenance Register (CRM)

Register Addresses
May be changed by "A" jumpers.
- CRS 777160
- CRB1 777162
- CRB2 777164
- CRM 777166

Data Outputs
- CRB1 = 12-bit character (Hollerith code)
- CRB2 = 8-bit character (compressed Hollerith code)

Interrupts
- Priority = BR6 (may be changed by jumper plug)
- Vector = location 230 (may be changed by "V" jumpers)
- Types = error, transition to on-line, column read, and card done

Commands
Read, elect, and interrupt enable

Status Indications
- Error conditions = error, card supply error, card reader check, timing error
- Operational conditions = reader ready, reader transition to on-line, busy, column ready, card done

CSS
The CMS11-K Card Reader system is a low card handling system designed to interface with the PDP-11 family of processors and peripherals.

**FEATURES**
- 250 cards per minute
- software-compatible with standard CM11 card reader
- low cost
- extremely reliable

**DESCRIPTION**
The CMS11-K system consists of two components, a card reader and a PDP-11 UNIBUS interface unit. The card reader is a motorized card handling device. Information is read from EIA standard (Hollerith code), 12 row 80 column punched or marked cards (or 40 column marked cards) at a nominal rate of 250 cards per minute.

The CMS11-K controller which interfaces the card reader to the UNIBUS consists of a single quad module that mounts in a small
peripheral controller (SPC) slot, and connects to the card reader by a single cable. Command and monitoring functions are provided by the controller. The controller also handles data transfers from the card reader to the UNIBUS. A 12-bit output character (one byte) is used when compressed Hollerith code is desired.

**REGISTERS**

**Status Register 777160**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>ERROR</td>
</tr>
<tr>
<td>14</td>
<td>CARD DONE</td>
</tr>
<tr>
<td>13</td>
<td>HOPPER CHECK</td>
</tr>
<tr>
<td>12</td>
<td>MOTION CHECK</td>
</tr>
<tr>
<td>11</td>
<td>TIMING ERROR</td>
</tr>
<tr>
<td>10</td>
<td>ON LINE TRANSFER</td>
</tr>
<tr>
<td>9</td>
<td>BUSY</td>
</tr>
<tr>
<td>8</td>
<td>READY</td>
</tr>
<tr>
<td>7</td>
<td>COLUMN READY</td>
</tr>
<tr>
<td>6</td>
<td>INTERRUPT ENABLE</td>
</tr>
<tr>
<td>5</td>
<td>EJECT</td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>NOT USED</td>
</tr>
</tbody>
</table>

**Bit: 15  Name: ERROR**

**Function:** Used to indicate that an error condition is present. This bit is set whenever one of the following conditions occurs:

- the card reader goes off-line from an on-line condition. During normal operation, this occurs when a card reader check or supply error is sensed.
- a TIMING ERROR is present when the reader completes reading of the card (CARD DONE).
- an attempt is made to read a card while the ERROR bit is set and the error-causing conditions have not been corrected. The bit remains set and subsequent READ commands are ignored.

This bit is connected to the interrupt logic so that the program can branch to an error-handling routine.

This is a read-only bit, cleared by INIT.

With the error removed, bits 15, 14, 11, and 10 are automatically cleared when the status is loaded. However, if using a DATOB for loading, the low order byte must be used because the high order byte has no effect on the status register.
Bit: 14  Name: CARD DONE
Function: When set, indicates that one card has passed through the read station and the next card may be requested from the input hopper. This bit is connected to the interrupt logic.

This is a read-only bit, cleared by INIT or by loading the status register.

Bit: 13  Name: HOPPER CHECK
Function: When set, this bit indicates that either the input hopper is empty or the output stacker is full. In either case, the condition must be corrected before further operation can take place.

This is a read-only bit, cleared by correcting the error condition.

Bit: 12  Name: MOTION CHECK
Function: When set, this indicates the presence of an abnormal condition in the card reader. Any one of the following three conditions set this bit:

- FEED ERROR—indicates the card reader feed mechanisms failed to deliver a card to the read station when demanded.
- MOTION ERROR—indicates a card jam in the reader.
- STACK FAIL—indicates that card has not been delivered to the output stacker.

This is a read-only bit, cleared by correcting the error condition.

Bit: 11  Name: TIMING ERROR
Function: When set, this indicates that a new column of data has been loaded into the data buffer before a previously loaded column was read by the program. Clears COLUMN READY bit at this time and TIMING ERROR causes the ERROR bit to be indicated at CARD DONE time.

Once the TIMING ERROR bit is set, the column ready flip-flop clocking is inhibited and no data transfers can take place until TIMING ERROR is cleared.

When the EJECT bit is set prior to issuing a READ command, it prevents TIMING ERROR from setting because timing error is not relevant if the card is ejected.
This is a read-only bit, cleared by INIT or by loading that status register.

Bit: 10  Name: READER TRANSITION TO ON-LINE
Function: When set, this bit indicates that the card reader has gone on-line and now is under program control. Depressing the card reader RESET switch brings the reader on-line, providing no error conditions exist.

The card reader goes off-line whenever an error condition is sensed or the RESET switch is depressed. When the reader goes from on-line to off-line, the ERROR bit is set.

This bit is connected to the interrupt logic so that the program can identify card reader availability.

This is a read-only bit, cleared by INIT or by loading the status register.

Bit: 9  Name: BUSY
Function: When set, indicates that a card is in the process of being read.

This is a read-only bit, cleared when the card is not in the read station or when the READ command is removed.

Bit: 8  Name: READER READY STATUS
Function: When set, this bit indicates that the reader is off-line. When clear, indicates the reader is on-line and ready to accept READ commands.

This is a read-only bit.

Bit: 7  Name: COMMAND READY
Function: When set, indicates that one column of data has been loaded into the data buffer and is ready for transfer to the bus.

When this bit is set and a card is ejected, a TIMING ERROR can still occur if the bit remains set when the new data arrives at the data buffer.

Once a card is ejected, COLUMN READY is inhibited from setting.

COLUMN READY is cleared when the data buffer is addressed (either CRB1 or CRB2). This operation does not affect the contents of the data buffer but does clear the COLUMN READY bit.
This bit is also connected to the interrupt logic so that a data transfer can take place once the data has been assembled in the buffer.

This is a read-only bit, cleared by INIT or by addressing the data buffer.

**Bit: 6**  **Name:** INTERRUPT-ENABLE  **Function:** When set, allows an interrupt to occur providing one of the following bits is also set: OFF-LINE (NOT READY), CARD DONE, TRANSITION TO ON-LINE, or COLUMN READY. TIMING ERROR causes an interrupt only when CARD DONE is set. This is a read/write bit, cleared in INIT.

**Bit: 5-2**  **Name:** UNUSED  **Function:**

**Bit: 1**  **Name:** EJECT  **Function:** When set, this bit prevents the COLUMN READY flag from being set. However, data transfers from the card reader to the data buffer still take place. Although the remaining card columns are actually read by the card reader, absence of COLUMN READY flags make it seem to the controller that the card has been ejected from the read station.

When EJECT is set prior to issuing a READ command, it also prevents the TIMING ERROR bit from being set because a timing error is not relevant if the card is ejected.

Setting EJECT alone does not eject a card. The READ bit must also be set to fetch the card.

This is a read/write bit, cleared by INIT.

**Bit: 0**  **Name:** READ  **Function:** When set, this bit causes the card reader feed mechanism to deliver one card to the read station. This bit is always read as a 0.

Cleared by INIT or by loading with a 0. This bit can be loaded by the program, but is always read as a 0 whether set or cleared.

**Data Buffer Register 777162**  **Bit: 15-12**  **Name:** UNUSED  **Function:**
CARD READERS

CMS11-K

Bit: 11-0  Name: ZONES 12-1
Function: These bits represent the output of a 12-bit data buffer register. During a read operation, data from a card is loaded into the buffer one column at a time. After each column is loaded, the contents of the buffer is placed on the UNIBUS for transfer to the processor or other bus device on demand.

Data Buffer Register 777164
Bit: 15-8  Name: UNUSED.
Function:
Bit: 7-0  Name: ZONES 12-1 COMPRESSED
Function: These bits represent the compressed output of a 12-bit data buffer register. During a read operation, data from a card is loaded into this buffer one column at a time. After each column is loaded, the contents of the 12-bit buffer are compressed into an 8-bit character by an encoding network and are then gated onto the UNIBUS as a low-order byte. This data compression is made available so that the card reader controller is fully compatible with the proposed expansion of the Hollerith code.

Maintenance Register 777166
Bit: 15  Name: MAINT
Function: When set, this bit allows the processor to check out card reader operation without a card reader being present. Any reference to this register must keep the MAINT bit set or all maintenance functions are disabled.

Bit: 14  Name: MBUSY
Function: When set, this bit along with MAINT being set, allows the processor to control the assertion and negation of the BUSY bit on the controller logic.

Bit: 13  Name: MRDY
Function: When set, this bit along with MAINT being set, allows the processor to control the assertion and negation of the READ bit in the controller logic.

Bit: 12  Name: MOT/HOP
Function: When set, this bit along with MAINT being set, allows the processor to jointly control the assertion and ne-
CMS11-K

gation of the MOTION and HOPPER CHECK bits in the controller logic.

Bit: 11-0  Name:  ZONE DATA
Function: When MAINT is set, bits 0-11 simulate data from the card reader. The same bit position assignments used here appear in the CRB1 register.

SPECIFICATIONS

Mechanical:
Cabinet: Table Top
Dimensions: 10.75 in. high, 19.25 in. wide, 11.75 deep
Weight: 32 lb

Electrical:
Operating Voltage and Line Frequency:
104-127 Vac at 48-63 Hz
190-264 Vac at 48-52 Hz
single phase

Operational:
Card Type: Standard 40 and 80 column cards
Card Rate:
250 cards/minute (60 Hz)
200 cards/minute (50 Hz)

Hopper Capacity:
Input: 250 cards
Output: 250 cards

Models:
CMS11-KA: 115 Vac, 60 Hz
CMS11-KB: 230 Vac, 50 Hz

Environmental:
Dry Bulb Temperature (operating):
(1000 ft. below sea level to 30,000 ft. above sea level)
54° to 100°F

Dry Bulb Temperature (nonoperating):
−30° to 150°F

Relative Humidity: 30 to 90% (noncondensing)

CONTROLLER SPECIFICATIONS

Mechanical:
Logic Housing: One quad board
CARD READERS

CMS11-K

Dimensions 10 1/2 in. high, 8 1/2 in. deep
Mounting Small Peripheral Controller
Prerequisite Slot
Interconnecting Cable 25 ft

**Electrical:**

<table>
<thead>
<tr>
<th>Description</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Power</td>
<td>+5 V @ 1.5 A</td>
</tr>
<tr>
<td>Logic Voltages</td>
<td>TTL Levels (+3 V, 0 V)</td>
</tr>
<tr>
<td>Module Type</td>
<td>M-Series</td>
</tr>
<tr>
<td>CSS</td>
<td></td>
</tr>
</tbody>
</table>
DESCRIPTION

The CR11-B Card Reader system provides PDP-11 users with a high performance card handling capability. Mounted in an attractive table-top cabinet configuration, the CR11-B may be used with any of DIGITAL's PDP-11 family of processors and peripherals.

Two distinct components comprise the CR11-B Card Reader—a card reader and a UNIBUS interface unit.

The card reader is a motorized, continuous running, card handling device. Information is read from EIA standard (Hollerith code). 12 row, 80-column punched cards at a nominal rate of 600 cards-per-minute.

The CR11-B Controller, which interfaces the card reader to the PDP-11 UNIBUS consists of a single quad module that mounts in a small peripheral controller slot and connects to the card reader by a single cable.

The CR11-B Controller provides the command and monitoring functions for the card reader, and in addition, handles data transfers from the card reader to the UNIBUS. A 12-bit output character is used for standard data transfers and an 8-bit output character (one-byte) is used when compressed Hollerith code is desired.
SOFTWARE
The CR11-B Card Reader is compatible with the standard CR11 card reader software. Within the control unit are two registers, one for card reader status, the other to hold one column of data from a card (Hollerith Code). The same register addresses and bit definitions are used.

CARD READER SPECIFICATIONS
Mechanical:
- Cabinet: One
- Dimensions: 19-9/16 in. h, 23-1/16 in. w, 18 in. d
- Weight: 75 lb

Electrical:
- Operating Voltage: 115/230 Vac ± 10%, single phase
- Line Frequency: 47-63 Hz
- Power Consumption: 450 W

Operational:
- Card Type: Standard 80-column card
- Card Rate: 600 card/minute (nominal)
- Hopper/Stacker: 1000
- Card Capacity: Silicon photocells, 12-bits simultaneously
CARD READERS

COMPARTMENT SPECIFICATIONS

Mechanical:

Logic Housing
Dimensions
Mounting Prerequisite
Interconnecting Cable

One quad board (M8290)
10\(\frac{1}{2}\) in. h, 8\(\frac{1}{2}\) in. d
Small Peripheral Controller Slot
25 ft

Electrical:

Logic Power
Logic Voltages
Module Type

+5 V @ 1.5 A
TTL Levels (+3 V, 0 V)
M-Series

Operational:

Commands
Status Indications
Interrupts

Read, Eject, and Interrupt Enable
Error, card reader check, card reader done
Vectored

Environmental (Operating):

Dry Bulb Temperature
Relative Humidity
Wet Bulb Temperature

50° to 100°F
30 to 90\% (non-condensing)
80°F

Environmental (Non-Operating):

Dry Bulb Temperature
Relative Humidity

−25° to 135°F
5 to 95\% (non-condensing)

Modules:

CR11-BA
CR11-BB

115 Vac, 60 Hz
230 Vac, 50 Hz

CSS
CHAPTER 4

DISKS

FEATURES

• economical storage for large volume
• random-access data storage
• easy-to-program controller

DESCRIPTION

The RK05 cartridge disk drive and RK11 controller are a complete mass storage system, offering an economical solution for large-volume, random-access data storage. The system includes a modular mass storage device utilizing removable disk cartridges and a complete easy-to-program control.

A disk cartridge holds over 1.2 million words. It is an ideal solution—for the case in which a large volume of programs and data are developed and maintained for one or more users. The system is expandable up to 9.6 million words per control (8 disks).

The removable disk cartridge offers the flexibility of virtually unlimited off-line capacity with rapid transfers of files between on-line and off-line without copying operations.

Average total access time on each drive is 70 milliseconds. On expanded systems, operations are overlapped for efficiency; one drive may read or write while one or more additional drives are seeking new head positions for the next transfer. All data transfers utilize the Non-Processor Request facility during transfers.

Each disk is permanently mounted inside a protective case that
automatically opens when inserted in the disk drive. While on-line, dust contamination is prevented by a highly efficient continuous absolute air filtration system.

The RK05 provides accurate data storage and transfers by means of a write check function, correct cylinder verification by hardware, hardware checksum, and hardware maintenance features. There are no mechanical detents, thus a major source of wear and critical adjustment is eliminated.

REGISTERS
Drive Status Register (RKDS) 777 400

Contains the current selected drive status and correct sector address.

Read only: all bits

Bit: 15-13  Name: Identification of Drive (ID)
Function: If an interrupt is caused as a result of a SEARCH COMPLETE (bit 13 RKCS) or a SEEK INCOMPLETE (bit 9 RKDS), these bits will contain the binary representation of the logical drive number that caused the interrupt.

Bit: 12  Name: Drive Power Low (DPL)
Function: Set when an attempt is made to initiate a new function or if a function was actively in progress when the control sensed a loss of power to one of the disk drives. This bit can be accompanied by bit 15 RKER (DRE) and is reset by a BUS INIT or a CONTROL RESET function.

Bit: 11  Name: RK05
Function: Set to identify the selected disk drive as an RK05.

Bit: 10  Name: Drive Unsafe (DRU)
Function: Set to indicate that an unusual condition has occurred
in the drive and it is unable to properly perform any operations. Putting the RUN/LOAD switch in the LOAD position will reset the condition. If, when setting the RUN/LOAD switch back to the RUN position, the condition recurs and the drive or associated power supply is inoperative, corrective maintenance procedures should begin. This bit can be accompanied by bit 15 RKER.

Bit: 9  
**Name:** Seek Incomplete (SIN)  
**Function:** Set to indicate that due to some unusual condition a SEEK function was not completed within 180ms of initiation. A DRIVE RESET function clears this condition. This bit can be accompanied by bit 15 RKER.

Bit: 8  
**Name:** Sector Counter OK (SOK)  
**Function:** Indicates that the selected drive sector counter (bits 0-3 RKDS) is not in the process of changing and is ready for examination.

Bit: 7  
**Name:** Drive Ready (DRY)  
**Function:** Set to indicate that the selected disk drive complies with the following conditions:
- properly supplied with power
- loaded with a disk cartridge
- door is closed
- LOAD/RUN switch is in the RUN condition
- the disk is spinning
- the heads are properly loaded
- the disk is not in a DRU condition (bit 10 RKDS)

Bit: 6  
**Name:** Read/Write/Seek Ready  
**Function:** Set when the selected drive head mechanism is not in motion and the drive is ready to accept a new function.

Bit: 5  
**Name:** Write Protect Status (WPS)  
**Function:** Set when the selected disk is in WRITE PROTECTED mode.

Bit: 4  
**Name:** SC = SA  
**Function:** Set when the disk heads are currently positioned over the disk addresses currently held in bits 0-3 RKDA.

Bit: 3-0  
**Name:** Sector Counter (SC)  
**Function:** Indicates the current sector address of the selected
drive. This is the look ahead. Sector address 00 is defined as the sector which follows the sector that contains the index pulse.

Error Register (RKER) 777 402

/read only: all bits.

**Bit: 15** Name: Drive Error (DRE)

Function: Set when an attempt is made to initiate a function when a function is actively in progress or when the selected drive is not ready or in some error condition; or if any of the drives in the system sense a loss of either ac or dc power. If this bit is found set, the RKDS should immediately be referenced to discover the cause of the condition.

**Bit: 14** Name: Overrun (OVR)

Function: Set if during a READ, WRITE, RD/CHK or WT/CHK operation on sector 138 surface 1 of cylinder address 3128 was finished and the RKWC had not yet overflowed. This essentially is an attempt to overflow out of a disk drive.

**Bit: 13** Name: Write Lock Out Violation (WLO)

Function: Set if an attempt is made to write on a disk which is currently being write-protected.

**Bit: 12** Name: Seek Error (SKE)

Function: Set if the disk head mechanism is not properly positioned while executing a normal READ, WRITE, RD/CHK or WT/CHK function.

**Bit: 11** Name: Programming Error (PGE)

Function: Set if the FMT bit (bit 10 RKCS) is set while initiating some function other than a READ or WRITE.
Bit: 10  Name: Non-Existent Memory (NXM)
Function: Set if memory does not respond within 20μs of the
time when the RK11 becomes Bus Master during a
DATI or DATO NPR sequence. Because of the speed
of the disk drive, it is possible that if a NXM does occur
it will be accompanied by a DLT (bit 7 RKER).

Bit: 9  Name: Data Late (DLT)
Function: Set when an NPR sequence is required before the pre-
vious one was completed.

Bit: 8  Name: Timing Error (TE)
Function: Set if a loss of timing pulses for 5μsec has been de-
tected.

Bit: 7  Name: Non-Existent Disk (NXD)
Function: Set if an attempt was made to initiate a function on a
nonexistent drive.

Bit: 6  Name: Non-Existent Cylinder (NXC)
Function: Set if an attempt was made to initiate a function on a
cylinder larger than 312(sub)8.

Bit: 5  Name: Non-Existent Sector (NXS)
Function: Set if an attempt was made to initiate a transfer on a
sector larger than 13(sub)8.

Bit: 1  Name: Checksum Error (CSE)
Function: Set while performing a RD/CHK or READ function as a
result of faulty recalculation of the checksum. Cleared
at the initiation of any new function. This is a soft error.

Bit: 0  Name: Write Check Error (WCE)
Function: Set if an error was encountered during a WT/CHK
function as a result of faulty bit comparison between
disk data and memory data. Clears at the initiation of
a new function. This is a soft error.

NOTE
When bits 5 through 15 are set, hard errors
are indicated. They are cleared only by a
BUS INIT or a CONTROL CLEAR function.

Control Status Register (RKCS) 777 404
Bit: 15  Name: Error
Function: Set when any bit in the RKER is set. Processor reac-
tion is dictated by bits 6 and 8 RKCS. This READ ONLY
bit clears if all the bits in RKER are cleared and if bit 14 RKCS is cleared.

**Bit: 14  Name:** Hard Error (H.E.)

**Function:** Set when any of bits 5-15 RKER are set by the control. Stops all controller action and processor reaction as dictated by bit 6 RKCS. This READ ONLY bit, along with bits 5-12 RKER, is cleared only by a BUS INIT or a CONTROL RESET function.

**Bit: 13  Name:** Search Complete (SCP)

**Function:** Signifies that the previous interrupt was caused as a result of some previous SEEK or DRIVE RESET function. READ ONLY bit. Clears at the initiation of any new function.

**Bit: 11  Name:** Inhibit Increment (INH BA)

**Function:** Setting this bit inhibits incrementing the RKBA during a data transfer. This allows a data to be transferred to or from any one bus address for the entire operation.

**Bit: 10  Name:** Format (FMT)

**Function:** FORMAT mode must be used only in conjunction with the normal READ and normal WRITE function. This mode is used to format a new disk pack or to reformat any sector that may have been erased or damaged due to control or drive failure.

In the FORMAT mode, the normal WRITE operation is altered so that the servo positioner is not checked for proper position before the write operation. During a WRITE, the header is rewritten each time the associated sector is written. In this mode, the normal READ operation is altered so that only one word is transferred to memory per sector; the header word. Therefore, a 3-word READ function in the FORMAT mode will
transfer 3 contiguous header words to 3 consecutive memory locations for software checking. For a 200-word transfer, 200 contiguous header words from 200 consecutive sectors will be read, and so on.

Bit: 8  Name: Stop on Soft Error (SSE)
Function: If a soft error is encountered while this bit is set:
• and bit 6 RKCS (IDE) is reset; all controller action will stop at the end of the current sector.
• and bit 6 RKCS (IDE) is set, all controller action will stop and a Bus Request will occur at the end of the current sector.

Bit: 7  Name: Control Ready (RDY)
Function: Signifies that the controller is no longer engaged in actively executing a function and is ready to accept a command.

Bit: 6  Name: Interrupt on Done Enable (IDE)
Function: The controller will issue a Bus Request and interrupt to vector address 220 if:
• a function has completed its activity;
• a hard error is encountered;
• a soft error is encountered and bit 8 RKCS is set.

Bit: 5-4  Name: Memory Extension (MEX)
Function: Reserved for extended bus addresses, and used in conjunction with the RKBA. These bits make up a two-bit counter that increments each time the RKBA overflows. A bus DATO to these bits overrides any overflow from the RKBA.

Bit: 3-1  Name: Function
Function: The bits indicate the binary representation of the function to be performed. The functions are:
CONTROL RESET (000)
WRITE (001)
READ (010)
WRITE CHECK (011)
SEEK (100)
READ CHECK (101)
DRIVE RESET (110)
WRITE LOCK (111)

Bit: 0  Name: Go
**Function:** Initiates the function encoded in bits 1 through 3 of RKCS. WRITE ONLY bit.

**Word Count Register (RKWC) 777 406**
Contains the twos complement of the total number of words to be affected by a given function. It increments by one after each word transfer.

**Current Bus Address Register (RKBA) 777 410**
Contains the Bus Address to or from which data will be transferred. The register is incremented by two at the end of each transfer.

**Disk Address Register (RKDA) 777 412**

**NOTE**
All RKDA bits are loaded from the bus data lines only in RK11 READY state, and cleared by BUS INIT and Control Reset. The RKDA is incremented automatically at the end of each disk sector.

**Bit: 15-13** **Name:** Drive Select (DR SEL)
**Function:** These bits contain the binary representation of the logical drive number currently being selected.

**Bit: 12-5** **Name:** Cylinder Address (CYL ADD)
**Function:** Binary representation of the cylinder address currently being selected. The largest valid address or number for the cylinder address is 312(sub)8.

**Bit: 4** **Name:** Surface (SUR)
**Function:** When set, the lower disk head is enabled and operation is performed on the lower surface. When clear, the upper disk head is enabled.

**Bit: 3-0** **Name:** Sector Address (SC)
**Function:** Binary representation of the disk sector to be addressed for the next function.

**Data Buffer Register (RKDB) 777 416**
**Bit: 15-0** **Name:** Data
**Function:** This register is a general data handler. It is loaded from the bus only while the RK11 is bus master during an NPR sequence. The RKDB is constructed of a 6-word register file capable of sustaining a UNIBUS NPR latency of 55μsec every 85μsec.
Cross Cylinder Operation
Surface 0 is defined as the upper surface and is active when RKDA 04 is reset. If a transfer is initiated that requires an overflow from surface 0, the control will automatically change to sector 0 of surface 1 with no time loss. If a transfer is initiated that requires an overflow from surface 1, the control will automatically move the heads to the next cylinder, check for proper head positioning, and continue the transfer on sector 0 and surface 0 of the new cylinder. An attempt to overflow out of the last sector of the last cylinder will result in an error condition.

At the end of each sector of data transfer, the RKDA is automatically incremented.

Hardware Poll
The controller is capable of having any or all of the drives perform a SEEK or DRIVE RESET operation at any one time. A HARDWARE POLL feature will identify the logical drive number in bits 13, 14, and 15 of the RKDS of any drive that has completed a SEEK or DRIVE RESET operation. It will cause an interrupt if bit 6 RKCS is set (IDE), if the controller is in the READY state (bit 7 RKCS is set), and if the controller was not attempting to cause an interrupt as a result of some other operation. This will occur even if bit 6 RKCS (IDE) was not set when first initiating the SEEK or DRIVE RESET function. If two or more drives complete the function simultaneously, the control will interrupt once for each drive and identify each one in turn in the RKDS. Care should be taken in this situation to raise the processor interrupt status to a level equal to or greater than that currently held by the RK11, or else a second interrupt will occur immediately after the first and the interrupt service routine will be interrupted. This situation will occur also if an attempt is made to initiate a SEEK to an address where the drive has already arrived. In this case one interrupt will occur as a result of the SEEK function having been successfully initiated and another to report that the heads have reached their destination.

Interrupts
Because of the format structure of the RK11, any interruption of a write sequence cannot be tolerated until the end of the sector, because this would result in an unformatted disk. Therefore, any outside intervention of this operation is delayed until the end of the current sector, including the CONTROL RESET function and the PROCESSOR or BUS INITIALIZE signals. All those functions, such as CONTROL RESET, SEEK, and WRITE LOCK, which normally take only a few microseconds to initiate, can actually take
DISKS

up to 3.3ms if initiated while writing. For this reason the SEEK and WRITE LOCK functions will cause an interrupt (if bit 6 RKCS is set) as soon as the function has been successfully initiated. The CONTROL RESET, which cannot cause an interrupt under any circumstances, can therefore take up to 3.3ms to complete.

SPECIFICATIONS FOR RK11-D

Main Specifications
Storage medium: disk cartridge
Capacity/cartridge: 1,228,800 words
Data transfer speed: 11.1μsec/word
Time for ½ revolution: 20msec
Disk rotation speed: 1500 RPM
Drives/control, max: 8

Track Positioning Time
One track move: 10msec
Average: 50msec
Maximum: 85msec

Data Organization
Surfaces/drive: 2
Tracks/surface: 200 + 3 spare
Sectors/track: 12
Words/sector: 256
Recording method: double frequency
Recording density: 2040 bits/inch, max
Access with single R/W: 1 to 65,536 words

Register Addresses
Drive Status: (RKDS) 777 400
Error: (RKER) 777 402
Control Status: (RKCS) 777 404
Word Count: (RKWC) 777 406
Current Bus Address: (RKBA) 777 410
Disk Address: (RKDA) 777 412
Data Buffer: (RKDB) 777 416

UNIBUS Interface
Interrupt vector address: 220
Priority level: BR5
Data transfer: NPR
Bus loading: 1 bus load

**Mechanical**
Mounting: A standard cabinet is supplied for the drive
Disk drive: Panel-mounted, 10 1/2” high
Disk control: 1 System Unit (SU)

**Power**
Starting current: 10A at 115 Vac for 2 seconds
Running current for drive: 2A at 115 Vac
Current for control: 7.5A at +5V
Heat dissipation: 160 W

**Environmental**
Operating temperature: 10°C to 40°C
Relative humidity: 10% to 90%

**SPECIFICATIONS FOR RK05**

**Mechanical**
Mounting: mounts in a standard PDP-11 cabinet
Size: 10 1/2” front panel height
Weight: 110 lb

**Power**
Starting current: 10A at 115 Vac for 2 seconds
Running current: 2A at 115 Vac
Heat dissipation: 160 W

**Prerequisite**
RK11
DESCRIPTION
The RK05-HC unit select switch option provides a reliable and convenient method of electronically (rather than manually) interchanging RK05s. It is a thumbwheel switch that is mounted on the front panel of an RK05 disk drive.

FEATURES
- simplicity, enhances system performances by allowing an easy method of interchanging disk drives
- versatility, easily reconfigured
- diagnostic software support, utilizes all standard RK05 software
- reliability, uses a thumbwheel switch designed for long life and efficient, reliable performance

DESCRIPTION
The RK05-HC Unit Select Switch option is a high quality eight-position thumbwheel switch mounted on the control panel of the RK05 disk drive. The Unit Select Switch option provides a reliable and convenient method of electronically interchanging RK05s. This technique enhances system performance and eliminates the need for field service or software support when disk drives must be reassigned.
**SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Logic Panels</th>
<th>One RK05 mounting panel including index/sector module and hardware to install and verify operation.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimensions</td>
<td>19 in. wide × 10 1/2 in. high</td>
</tr>
<tr>
<td>Prerequisite</td>
<td>RK05 disk drive</td>
</tr>
<tr>
<td>CSS</td>
<td></td>
</tr>
</tbody>
</table>
The RK06/RK07 disk drives are high-performance medium capacity storage drives that provide the reliability and features of a high capacity drive in a medium capacity, inexpensive subsystem.

FEATURES

• capacity
  RK06: 14 million 8-bit bytes per drive (formatted)
  112 million 8-bit bytes per subsystem (maximum)
  RK07: 28 million 8-bit bytes per drive (formatted)
  224 million 8-bit bytes per subsystem (maximum)

• performance
  RK06: 38 milliseconds average seek time
  RK07: 36.5 milliseconds average seek time
  538,000 bytes per second peak transfer rate

• reliability
  Track-following servo system for data reliability, error detection of connection and head offset positioning.
  —parity checking on all control transfers between drive and controller and controller and drive.
  —brush cycle
  —home lock prevents accidental head loading
DISKS

RK06, RK07

DESCRIPTION
The RK06/RK611 disk drive subsystem and the RK07/RK611 disk drive subsystem each consist of an RK611 drive controller and of up to eight RK06 and/or RK07 disk drives. Each RK06 or RK07 disk drive is a free-standing, high-performance moving head device that is connected to the RK611 controller via a daisy-chain bus arrangement. The RK611 controller, located in the associated cabinetry, provides an interface between the subsystem and a PDP-11 system via the UNIBUS. Both RK06 and RK07 drives can be used in one subsystem.

Dual access operation is a hardware option available to the RK06 and RK07 drives enabling either drive to be accessed through two different controllers. Figure 4-1 shows the system configuration for dual access operation. The eight RK06s or RK07s are daisy-chained; the two controllers can be attached to two different CPUs or the same one.

Media
The storage medium for the RK06 disk drive is a top-loading, dual-platter, RK06K disk cartridge which can be freely interchanged between any of the available RK06 drives. It has a maximum formatted storage capacity of 6.3 million 18-bit words or 6.9 million 16-bit words. The RK07 disk drive uses a similar cartridge, the RK07K disk cartridge, as the storage medium. It also can be interchanged between any of the available RK07 drives. It has a maximum formatted capacity of 12.5 million 18-bit words or 13.8 million 16-bit words. Note that an RK06K cartridge cannot be used on an RK07 drive, nor an RK07K cartridge on an RK06 drive.

Each dual-platter pack provides three recording surfaces that are serviced by three read/write heads and a servo surface that is monitored by a single read head. The recording surfaces provide three data tracks per cylinder with a maximum of 411 cylinders per RK06 disk pack or 815 cylinders per RK07 disk pack. Each track can accommodate either 20 (18-bit word) or 22 (16-bit word) sectors, while each sector contains 256 data words. The servo surface provides positioning signals for the heads and timing signals for data transfer synchronization.

The high-density recording capability (required to achieve maximum storage capacities) is provided by the use of the modified frequency modulation (MFM) encoding technique. In addition, each RK06 and RK07 disk drive and the controller contain phase-locked oscillator (PLO) circuitry which maintains a constant bit density if a disk is subjected to minor speed variations.
Figure 4-1 RK06/RK611-RK07/RK611 Dual Access System Configuration
DISKS

RK06, RK07

For head positioning, the maximum seek time in the RK06 disk drive (411 cylinders) is 75 ms, while the minimum (track-to-track for one cylinder) is 8 ms, with an average access time of 38 ms. The maximum seek time in the RK07 drive (815 cylinders) is 71 ms, and the minimum seek time is 6.5 ms. The average access time is 36.5 ms.

A data transfer rate of 4.3us per 16-bit word between the controller and the UNIBUS provides an average transfer rate of 232,500 words per second.

Diagnostic and Error Detection/Correction Capabilities
Diagnostic capabilities are enhanced by an extensive status/error reporting network, consisting of nine UNIBUS-addressable registers which monitor subsystem activities and are visible to the software.

For extended maintenance and serviceability, the RK06/RK611 and RK07/RK611 subsystems provide a software controlled diagnostic mode (DMD) of operation. When diagnostic mode is initiated, the drive interface lines are effectively disconnected from the controller while the UNIBUS interface remains intact. With this arrangement, Read or Write commands can be initiated using simulated data and control techniques, while actual transmissions between the drives and the controller are disabled. In this manner, closed loop data transfers to and from main storage can verify controller operation in relation to data control.

The RK611 controller provides data error detection and correction logic that utilizes an error correction code (ECC) technique to detect and identify (for software correction) data error bursts up to 11 bits in length and to detect (but not identify) error bursts longer than 11 bits. In addition and in conjunction with ECC operation, each RK06 or RK07 disk drive has a head offset capability which allows the recovery of data from a cartridge that may have been written by a drive with slightly misaligned heads.

The data recovery features, operating in conjunction with the PLO clock system and the MFM recording technique, provide increased reading and recording reliability. However, if a disk pack sector proves defective, and hardware and software attempts to recover its data are unsuccessful, the operating system can mark the sector "bad" so that future attempts to use it will be prevented.

Maintenance Features
The following standard features enhance the reliability, availability, and serviceability of the RK06/RK611 and RK07/RK611 subsystems.
The RK06 and RK07 drive interface is designed to allow a specific drive to be electrically isolated from the controller for maintenance purposes. This allows an off-line tester to be utilized without taking a drive off-line or cycling the system down. With this feature, software can reconfigure the system for continued operation while maintenance is performed.

Service access to an RK06 or RK07 disk drive is from the top, front, or rear of the drive and not from the sides. Therefore, maintenance for a given drive in a multidevice system can be performed without disturbing interdrive cabling.

The logic and power board cages can be extended, following removal of the rear panel of an RK06 or RK07 disk drive, to facilitate emergency maintenance.

Mean-time-to-repair (MTTR) for emergency maintenance is improved by the inclusion of light emitting diodes (LEDs) on the front edge of certain logic boards. The LEDs provide a service engineer with an indication of the functionality of certain key logic areas.

For the implementation of cartridge alignment procedures, a protection switch is available to the service engineer to provide write protection for the cartridge and control of head velocity to ensure alignment integrity.

If an RK06 or RK07 drive loses ac power, neither the drive nor cartridge will be harmed; no data will be lost, and the format will remain intact.

When dual-access RK06 or RK07 disk drives are installed, the logic allows dual-access functionality to be tested utilizing only one of the two available controllers. This feature provides enhanced availability for multiprocessor systems by freeing one controller for normal dual-access operations.

**RK06 DISK DRIVE PERFORMANCE SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Medium</td>
<td>Dual-platter magnetic cartridge, DEC RK06K-DC</td>
</tr>
<tr>
<td>Disk diameter</td>
<td>355mm (14 in.) nominal</td>
</tr>
<tr>
<td>Magnetic heads</td>
<td>3 read/write: 1 servo</td>
</tr>
</tbody>
</table>
### DISKS

#### RK06, RK07

<table>
<thead>
<tr>
<th>Recording capacity (formatted)</th>
<th>18-bit word</th>
<th>16-bit word</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cylinders/cartridge</td>
<td>411</td>
<td>411</td>
</tr>
<tr>
<td>Tracks/cylinder</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Tracks/cartridge</td>
<td>1233</td>
<td>1233</td>
</tr>
<tr>
<td>Sectors/track</td>
<td>22</td>
<td>20</td>
</tr>
<tr>
<td>Words/sector</td>
<td>256</td>
<td>256</td>
</tr>
<tr>
<td>Bits/word</td>
<td>18</td>
<td>16</td>
</tr>
<tr>
<td>Bits/sector</td>
<td>4608</td>
<td>4096</td>
</tr>
<tr>
<td>Bits/track</td>
<td>92,160</td>
<td>90,112</td>
</tr>
<tr>
<td>Bits/surface</td>
<td>37.88M</td>
<td>37.04M</td>
</tr>
<tr>
<td>Bits/pack</td>
<td>113.63M</td>
<td>111.11M</td>
</tr>
<tr>
<td>Bits/inch (inner track)</td>
<td>4040</td>
<td>4040</td>
</tr>
<tr>
<td>Tracks/inch</td>
<td>192.3</td>
<td>192.3</td>
</tr>
</tbody>
</table>

#### Electrical

- **Voltage**
  - See model designations in Section 1.5.
- **Input Power**
  - Single access drives: 500 W maximum at 60 Hz, 450 W nominal at 60 Hz, 550 W maximum at 50 Hz, 500 W nominal at 50 Hz
  - Dual access drives: 550 W maximum at 60 Hz, 500 W nominal at 60 Hz, 600 W maximum at 50 Hz, 550 W nominal at 50 Hz

#### Start current

- **Single access drives**
  - 10.5 A rms at 115V/60 Hz, 5.3 A rms at 230V/60 Hz, 11.0 A rms at 115V/50 Hz, 5.5 A rms at 230V/50 Hz
- **Dual access drives**
  - 11.3 A rms at 115V/60 Hz, 6.1 A rms at 230V/60 Hz, 11.8 A rms at 115V/50 Hz, 6.3 A rms at 230V/50 Hz

- **Power factor**
  - 0.80 minimum

- **AC-low detection**
  - Less than 90V (rms) for one cycle or more

#### Power cord

- **Length**
  - 2.7m (9 ft)
**DISKS**

**RK06, RK07**

Plug type
- NEMA 5-15P for 120Vac (nominal) models
- NEMA 6-15P for 240Vac (nominal) models

**Operating environment**
- Ambient temperature: 10°C to 40°C (50°F to 104°F)
- Maximum temperature rate of change: 20°C/hour (36°F/hour)
- Relative humidity of 28°C: 10% to 90% for a maximum wet bulb temperature of 28°C
- Maximum altitude: 2440 m (8000 ft)
- Bit transfer rate (unbuffered nominal): 4.30 M/S
- Bit cell width: 232.5 ns

**Latency**
- Rotational frequency: 2400 rpm ± 2.5%
- Average: 12.5 ms (1/2 rotation)
- Maximum: 25.0 ms

**Seek Times**
- Average: 38 ms
- Maximum: 71 ms
- Start/Stop times: 60 seconds maximum, 30 seconds nominal

**Model Designations**
- RK06-EA: 90-128Vac @ 60 ± 0.5 Hz
- RK06-EB: 180-256Vac @ 60 ± 0.5 Hz
- RK06-EC: 90-128Vac @ 50 ± 0.5 Hz
- RK06-ED: 180-256Vac @ 50 ± 0.5 Hz

**NOTE**
Models RK06-FA through FD are the dual-access models corresponding to models EA through ED respectively.

**RK06K-DC Cartridge**
- Temperature stabilization: If the cartridge and drive are at approximately the same temperature, 30 min.; if there is some difference, up to
DISKS

RK06, RK07

two hours, depending on the difference.
40°F to 120°F

Operating temperature range
Allowable relative humidity (for operation)
Storage temperature range (for recorded disks)
Allowable relative humidity (for storage)

8% to 90% for a maximum wet bulb reading of 28°C (82°F)
−40°C to 65°C (−40°F to 150°F)
8% to 80% for a maximum wet bulb reading of 28°C (82°F)

RK07 DISK DRIVE PERFORMANCE SPECIFICATIONS

Characteristics
Storage Type
Medium
Dual-platter magnetic cartridge, DEC RK07K-DC

Magnetic heads
355 mm (14 in.) nominal
3 read/write, 1 servo

Recording capacity (formatted)

18-bit word
16-bit word

815
815

3
3

2445
2445

20
22

256
256

18
16

4608
4096

73.43M
75.11M

220.32M
225.33M

4040
4040

384.6
384.6

Bits/inch (inner track)

Tracks/inch

Electrical
Voltage
See model designations in Section 1.5.

Input Power
500 W maximum at 60 Hz
450 W nominal at 60 Hz

Single access drives
### DISKS

**RK06, RK07**

- **550 W maximum at 50 Hz**
- **500 W nominal at 50 Hz**

<table>
<thead>
<tr>
<th>Component</th>
<th>Dual access drives</th>
<th>Start current</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>550 W maximum at 60 Hz</td>
<td>10.5 A rms at 115V/60 Hz</td>
</tr>
<tr>
<td></td>
<td>500 W nominal at 60 Hz</td>
<td>5.3 A rms at 230V/60 Hz</td>
</tr>
<tr>
<td></td>
<td>600 W maximum at 50 Hz</td>
<td>11.0 A rms at 115/50 Hz</td>
</tr>
<tr>
<td></td>
<td>550 W nominal at 50 Hz</td>
<td>5.5 A rms at 230V/50 Hz</td>
</tr>
</tbody>
</table>

- **Power factor** 0.80 minimum
- **AC-low detection** Less than 90 V (rms) for one cycle or more

### Power cord

- **Length** 2.7m (9 ft)
- **Plug type** NEMA 5-15P for 120Vac (nominal) models, NEMA 6-15P for 240Vac (nominal) models

### Operating environment

- **Ambient temperature** 10°C to 40°C (50°F to 104°F)
- **Maximum temperature rate of change** 20°C/hour (36°F/hour)
- **Relative humidity** 10% to 90% for a maximum wet bulb temperature of 28°C (82°F)
- **Maximum altitude** 2440 m (8000 ft)
- **Bit transfer rate (unbuffered nominal)** 4.30 M/S
- **Bit cell width** 232.5 ns

### Latency

- **Rotational frequency** 2400 rpm ± 2.5%
DISKS

RK06, RK07

Average 12.5 ms (1/2 rotation)
Maximum 25.0 ms

Seek Times
Average 36.5 ms
Maximum 71.0 ms
Start/stop times 60 seconds maximum, 30 seconds nominal

Model Designations
RK07-EA 90-128Vac @ 60 ± 0.5 Hz
RK07-EB 180-256Vac @ 60 ± 0.5 Hz
RK07-EC 90-128Vac @ 50 ± 0.5 Hz
RK07-ED 180-256Vac @ 50 ± 0.5 Hz

NOTE
Models RK07-FA through FD are the dual-access models corresponding to models EA through ED respectively.

RK07K-DC Cartridge
Temperature stabilization time
If the cartridge and drive are at approximately the same temperature, 30 min.; if there is some difference, up to two hours, depending on the difference.

Operating temperature range
40° to 120°

Allowable relative humidity (for operation) 80% to 90% for a maximum wet bulb reading of 28°C (82°F)

Storage temperature range (for recorded disks) −140°C to 65°C (−40°F to 150°F)

Allowable relative humidity (for storage) 8% to 80% for a maximum wet bulb reading of 28°C (82°F)

RK611 Disk Drive Controller
The RK611 disk controller presents a complete control and data interface to the PDP-11 UNIBUS (which serves both the central processor and main memory) and to the KR06 or RK07 disk drives.

Command Control
The RK611 control interface contains all the logic required to receive, store, and decode the 13 separate disk commands (e.g.,
RK06, RK07

Start Spindle, Seek Write, etc.) that can be executed by the controller. In addition, the control interface contains all the logic required to receive and store the status information (i.e., modes, conditions, faults, and errors) delivered from a selected drive. To accommodate the exchange of information (commands/status) between the control interface and a selected drive, information is both sent (commands) and received (status) via a pair of bidirectional serial message lines.

Data Control
The RK611 data interface contains all the logic required to transfer data (16- or 18-bit words) between main memory and a selected drive. Since UNIBUS transfers require parallel data flow, while transfers to and from a disk require serial data flow, the data interface also contains parallel-to-serial (memory-to-disk) and serial-to-parallel (disk-to-memory) conversion logic. In addition, a bidirectional read/write data line is used to accommodate the exchange of serial data between the RK611 data interface and a selected drive.

Finally, the data interface logic contains a 66-word data buffer (Silo), that is used to compensate for the timing differences that exist between the average UNIBUS data transfer rate (4.3 $\mu$s/word) and the burst transfer rate of the disk (3.7 $\mu$s/word).

Controller Registers
The controller contains 15 UNIBUS-addressable registers. Nine of the 15 registers provide temporary storage for the manipulation of status and/or error information. This information, coupled with the diagnostic capabilities of the controller, allows a programmer to create diagnostics that can be extremely effective as fault isolation aids.

Basic RK06 or RK07 Disk Subsystem

RK611 CONTROLER PERFORMANCE SPECIFICATIONS

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required mounting space</td>
<td>Occupies one double system unit in an expansion box</td>
</tr>
<tr>
<td>Power requirements</td>
<td>+5Vdc $\pm$ 5% @ 15A</td>
</tr>
<tr>
<td></td>
<td>+15Vdc $\pm$ 5% @ 175mA</td>
</tr>
<tr>
<td></td>
<td>$-15$Vdc $\pm$ 5% @ 400mA</td>
</tr>
<tr>
<td>Number of drives/controllers</td>
<td>8(max)</td>
</tr>
<tr>
<td>Number of UNIBUS-addressable registers</td>
<td>15</td>
</tr>
</tbody>
</table>
DISKS

RK06, RK07

Figure 4-2

Device base address 777440 (octal) switch-selectable
Device interrupt vector 000210 (octal) switch-selectable

NOTE

The RK611 device base address overlaps the Look-Ahead Register in the RC11 disk subsystem, and the RK611 Device Interrupt Vector overlaps the same vector in the RC11 subsystem.

Interrupt priority Level 5 (plug-selectable)
Small peripheral controller options Up to three slots, one of which must be quad height. The other two can be quad or hex height.
Data transfer rates 22 sector (16-bit data words)
20 sector (18-bit data words)
UNIBUS to controller (average word rate) 4.3 µs/word
4.6 µs/word
Drive to controller (burst rate) 3.7 µs/word
4.2 µs/word

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DISKS

RK06, RK07

Time to update drive status 15 $\mu$s
Time to update drive attention 7.4 $\mu$s
Error detection/correction 32-bit ECC word/sector
Time for correction Less than one revolution
Maintainability Diagnostic mode places all controller timing and data paths under software control.
Number of sectors/track Software-programmable for 20 or 22 sector format.

RK611 DEVICE REGISTERS
There are 15 usable, 16-bit device registers contained in the RK611 that are used to interface the controller with the RK06 or RK07 drives and with the PDP-11 UNIBUS. The 15 registers are loaded and/or read under program control to initiate selected disk commands and monitor subsystem status and error conditions. Device register bits are generally cleared by a UNIBUS Initialize (INIT), Controller Clear (CCLR), or Subsystem Clear (SCLR) operation. In the following description (unless otherwise specified), it should be understood that the clearing of a bit by any one of these three methods is implied.

NOTE
The RK611 does not recognize DATOB (MOVB, BICB, etc.) bus cycles. All registers must be written as words.

RK611 UNIBUS-Addressable Registers

<table>
<thead>
<tr>
<th>Address (octal)</th>
<th>Type</th>
<th>Register</th>
<th>Basic Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>777 440</td>
<td>R/W</td>
<td>Control/Status Register 1 (RKCS1)</td>
<td>Decode commands/ controller status</td>
</tr>
<tr>
<td>777 442</td>
<td>R/W</td>
<td>Word Count Register (RKWC)</td>
<td>Number of data words for transmission</td>
</tr>
<tr>
<td>777 444</td>
<td>R/W</td>
<td>Bus Address Register (RKBA)</td>
<td>Main memory location for word</td>
</tr>
<tr>
<td>777 446</td>
<td>R/W</td>
<td>Disk Address Register (RKDA)</td>
<td>Desired track/sector address</td>
</tr>
<tr>
<td>777 450</td>
<td>R/W</td>
<td>Control/Status Register 2 (RKCS2)</td>
<td>Additional control information</td>
</tr>
</tbody>
</table>

56
<table>
<thead>
<tr>
<th>Address</th>
<th>Type</th>
<th>Register</th>
<th>Basic Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>777 452</td>
<td>R</td>
<td>Drive Status Register (RKDS)</td>
<td>Drive status reports</td>
</tr>
<tr>
<td>777 454</td>
<td>R</td>
<td>Error Register (RKER)</td>
<td>Additional drive status</td>
</tr>
<tr>
<td>777 456</td>
<td>R/W</td>
<td>Attention Summary/Offset Register (RKAS/OF)</td>
<td>Drive status change state/head offset value</td>
</tr>
<tr>
<td>777 460</td>
<td>R/W</td>
<td>Desired Cylinder Register (RKDC)</td>
<td>Cylinder address</td>
</tr>
<tr>
<td>777 462*</td>
<td></td>
<td></td>
<td>Unused</td>
</tr>
<tr>
<td>777 464</td>
<td>R/W</td>
<td>Data Buffer Register (RKDB)</td>
<td>Data word to/from Silo</td>
</tr>
<tr>
<td>777 466</td>
<td>R/W</td>
<td>Maintenance Register 1 (RKMR1)</td>
<td>Drive message select/control</td>
</tr>
<tr>
<td>777 470</td>
<td>R</td>
<td>ECC Position Register (RKECPS)</td>
<td>Error position information following correction sequence.</td>
</tr>
<tr>
<td>777 472</td>
<td>R</td>
<td>ECC Pattern Register (RKECPT)</td>
<td>Error correction pattern following correction sequence.</td>
</tr>
<tr>
<td>777 474</td>
<td>R</td>
<td>Maintenance Register 2 (RKMR2)</td>
<td>Shift register A for serial Message A.</td>
</tr>
<tr>
<td>777 476</td>
<td>R</td>
<td>Maintenance Register 2 (RKMR3)</td>
<td>Shift register B for serial Message B.</td>
</tr>
</tbody>
</table>

**NOTE**

R/W = read/write (selected bits) in relation to UNIBUS. R = read only in relation to UNIBUS.

* The RK611 responds to this address with SSYN. However, if the bus cycle is a DATI, D (00:15) is undefined.

**Control and Status Register (RKCS1) 777 440**

This register can be read or written via program control. It is used to store the current disk command function code and operational status of the controller. In addition, the register can initiate command execution and can enable a controller clear operation.
Bit: 15  Name: Combined Error/Controller Clear (CERR/CCLR)

Function: As a combined error (CERR) indicator, bit 15 can be set by the controller, or any one of the drives, to indicate that a subsystem error has occurred (Table 7-1). However, when the bit is set via program control, a controller initialize (CCLR) operation is enabled which clears the controller and results in the clearing of bit 15 itself. Thus, if the bit is internally set (CERR) by an error that is followed by an external set (CCLR) to initialize the controller, bit 15 will be cleared. However, since only controller errors will be initialized by CCLR, any error originating in a drive will remain set in the drive.

CAUTION: When using a BIC instruction on the RKCS1 register, ensure that a 1 is set in bit 15 of the mask. If this is not done and CERR is set, a CCLR will occur, and the RK611 will be cleared. For example, to clear the Interrupt Enable (IE) bit (bit 6 in RKCS1), the following instruction format is recommended:

BIC #100100, @ RKCS1

Bit: 14  Name: Drive Interrupt (DI)

Function: In relation to program control, Drive Interrupt (DI) is a read-only bit. When set, the bit differentiates between a drive-initiated interrupt and a controller-initiated interrupt.

The DI bit is set when any drive sets an associated Attention (ATNO-ATN7) bit (8-15 in RKAS-OF). Thus, if the Interrupt Enable (IE) bit is set, the setting of the DI bit with the set condition of Controller Ready (RDY),
RK06, RK07

bit 7 in RKCS1, indicates a drive-initiated interrupt. The DI bit is reset by UNIBUS Initialize (INIT), Subsystem Clear (SCLR), or by the execution of Drive Clear commands to all drives asserting Attention.

Bit: 13  Name: Drive-to-Controller Parity Error (DTC PAR)
Function: The DTC Parity Error is a read-only bit that is internally set to indicate that a parity error has been detected in a serial message received from the selected drive.

Bit: 12  Name: Controller Format (CFMT)
Function: The Controller Format bit specifies the number of sectors for each track in the selective drive. When bit 12 is set, a 20-sector format (18-bit data words) is defined for the sector counter located in the drive, and when the bit is reset, a 22-sector format (16-bit data words) is defined.

Bit: 11  Name: Controller Time-Out (CTO)
Function: Controller Time-Out is a read-only error bit that is set to indicate that GO, bit 0 in RKS1, has been set for approximately 800 ms. Since this interval exceeds the time required to execute the longest possible drive operation (i.e., a Seek from cylinder 410 to cylinder 0 followed by a 65K work data transfer), the set condition of this bit indicates that the last command has not been completed due to a malfunction.

Bit: 10  Name: Controller Drive Type (CDT)
Function: This bit specifies the type of drive that will be selected by the controller. To specify RK06 disk drives, the bit must be 0. For an RK07 drive, the bit must be 1.

Bit: 8-9 Name: Extended Bus Address (BA16, BA17)
Function: The Extended Bus Address bits reflect UNIBUS upper address bits 16 and 17 and as such are an extension of the 16-bit RKBA register which contains the memory address required for the current data transfer.

Bit: 7  Name: Controller Ready (RDY)
Function: Controller Ready (RDY) is effectively a read-only bit. However, the bit can be externally set via conventional initialization (INIT, CCLR, SCLR) or internally set upon completion of a command. The RDY bit is reset when GO, bit 0 in RKCS1, is set.

Bit: 6  Name: Interrupt Enable (IE)
**Function:** When the Interrupt Enable (IE) bit is set, the controller will be allowed to interrupt the processor under any of the following conditions:

When Controller Ready (RDY), bit 7 in RKCS1, is set upon completion of a command.

When any drive sets an associated Attention (ATNO-ATN7) bit (8-15) in RKAS/OF, with the set condition of Controller Ready (RDY).

When any drive or the controller indicates the presence of an error by the setting of Controller Error (CERR), bit 15 in RKCS1.

In addition, via program control, an interrupt can be forced by the simultaneous setting of the Interrupt Enable/IE) and Controller Ready (RDY) bits in RKCS1. Finally, Interrupt Enable, bit 6, can be reset via program control as well as by conventional initialization (INIT, CCLR, SCLR).

**Bit:** 1-4  **Name:** Function Code (F1-F4)

**Function:** The configuration of the Function Code bits (F1-F4), with the setting of the GO bit, allows the selected drive to respond to the following command control configuration.

<table>
<thead>
<tr>
<th>Command</th>
<th>F4</th>
<th>F3</th>
<th>F2</th>
<th>F1</th>
<th>GO</th>
<th>Octal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Select Drive</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>01</td>
</tr>
<tr>
<td>Pack acknowledge</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>03</td>
</tr>
<tr>
<td>Drive Clear</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>05</td>
</tr>
<tr>
<td>Unload</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>07</td>
</tr>
<tr>
<td>Start Spindle</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>11</td>
</tr>
<tr>
<td>Recalibrate</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>13</td>
</tr>
<tr>
<td>Offset</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>15</td>
</tr>
<tr>
<td>Seek</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>17</td>
</tr>
<tr>
<td>Read Data</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>21</td>
</tr>
<tr>
<td>Write Data</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>23</td>
</tr>
<tr>
<td>Read Header</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>25</td>
</tr>
<tr>
<td>Write Header</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>27</td>
</tr>
<tr>
<td>Write Check</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>31</td>
</tr>
</tbody>
</table>

**Bit:** 0  **Name:** Go (GO)

**Function:** When the GO bit is set, the disk command function code (F1-F4) is executed. With the GO bit set, only
other device register bits can be set (diagnostic mode excepted), as follows:

Controller Clear (CCLR), bit 15 in RKCS1, may be set via program control to initialize (general clear and preset) certain device registers within the controller. However, any status and error conditions set in the drives are not affected.

Subsystem Clear (SCLR), bit 5 in RKCS2, may be set via program control to initialize both controller and all of the drives.

When command execution is completed, the GO bit is reset and the controller is ready to accept a command. However, the GO bit cannot be set if the Combined Error (CERR) bit is set. When CERR is set, the execution of a command can only occur following the initiation of a CCLR.

Spare Bit—Spare bit 5 can be written and read back.

Word Count Register (RKWC) 777 442
The RKWC Register is loaded with the twos complement of the number of data words to be transferred to or from main memory. The register is incremented by 1 after each bus cycle, and accommodates a maximum transfer of 65,536 words. The RKWC Register can only be cleared by writing all zeros via program control.

Bus Address Register (RKBA) 777 444
The RKBA Register is initially loaded with the low-order 16 bits of the UNIBUS address that will reflect the main memory start location for a data transfer. With the low-order bit (0) always forced to 0, the RKBA Register content is combined with high-order bits 8 and 9 of the RKCS1 Register (BA16), (BA17) to form a complete even-number word address. Following each data transfer bus cycle, the register is incremented by two to select the next even-numbered location.

Disk Address Register (RKDA) 777 446

<table>
<thead>
<tr>
<th>15</th>
<th>11</th>
<th>10</th>
<th>8</th>
<th>7</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPARE BITS</td>
<td>TRACK ADDRESS</td>
<td>SPARE BITS</td>
<td>SECTOR ADDRESS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

For Read, Write, and Write Check commands, the RKDA Register is initially loaded to define the desired sector (1 of 20 or 22) and track (1 of 3 read/write heads) on the selected drive, from or to which the first block of a data transfer will be initiated. If the
word count value indicates that a block of more than 56 data words is to be transferred, the Sector Address bits of the RKDA Register will be incremented to select the next consecutive sector and the next track, if necessary, until a word count overflow indicates that data transfers are completed or an error occurs. In either case, completion of the command is indicated by the setting of the Controller Ready (RDY) bit in RKCS1 and an increment of the RKDA Register to the next sector location.

Bit: 15-11 Name: Spares
Function: Spare bits 15-11 are 0.
Bit: 10-8 Name: Track Address (TA0-TA2)
Function: The Track Address bits are configured (0-2) to select the appropriate read/write head associated with the desired track. The Track Address bits are incremented after the last sector (23(sub)8 or 25(sub)8) on the track has been transferred and the Sector Address has been reset to zero. Similarly, if transfers continue beyond the last sector of the last track (2) of a given cylinder, the Track Address is reset to zero and the Cylinder Address (in RKDC) is incremented by one. In this manner, subsequent sectors, tracks, and cylinders can be consecutively transferred until the word count equals zero. However, if the word count does not equal zero after the transfer of the last sector (19 or 20(sub)10) on the last track (2) of the last cylinder (410(sub)10) for an RK06 (or 814(sub)10 for an RK07), a Cylinder Overflow Error (COE) will occur.

Bit: 7-5 Name: Spares
Function: Spare bits 5-7 are 0.
Bit: 4-0 Name: Sector Address (SAO-SA4)
Function: Sector Address bits 0-4 are configured (00-23) to select a value (00-19(sub)10) for a 20-sector format (18-bit data words) or configured (00-25) to select a value (00-21(sub)10) for a 22-sector format (16-bit data words). The Sector Address is incremented by one when the sector has been transferred.

Control/Status Register 2 (RKCS2) 777 450
The RKCS2 Register can be read or written via program control and is used to store the current drive select code, subsystem operational status, and Silo control information. In addition, the register can initiate a Subsystem Clear (SCLR) operation.
**Bit: 15**  
**Name:** Data Late Error (DLT)  
**Function:** Data Late Error is a read-only error bit that is set to indicate the following conditions:  
During the execution of a Write command, the Silo was empty when the risk required a data word.  
During the execution of a Read or a Write Check command, the Silo was full when the disk provided the next data word.  

This error bit can be forced set under the following conditions:  
- by loading the Data Buffer Register (RKDB) when Input Ready (IR) (bit 6) is reset.  
- by reading the Data Buffer Register (RKDB) when Output Ready (OR) (bit 7) is reset.  

**NOTE**  
When RKCS2 is loaded under program control, the controller Sector/Index pulse separator logic is initialized. This action causes the controller to ignore the next sector or index pulse from the selected drive. Therefore, unnecessary loading of RKCS2 can increase latency time by an amount equivalent to 1.5 sectors.

**Bit: 14**  
**Name:** Write Check Error (WCE)  
**Function:** Write Check Error is a read-only error bit that is set to indicate that a data word read from the disk during the execution of a Write Check command did not compare with the corresponding data word contained in main memory. If a write check error is detected
and the BAI bit is not set, the RKBA Register will contain the memory address of the next data word location (mismatched word address plus two).

**Bit: 13**  
**Name:** UNIBUS Parity Error (UPE)  
**Function:** UNIBUS Parity Error is a read-only error bit that is set to indicate that a parity error has been detected in a 16-bit data word format from main memory, during the performance of a Write or Write Check command. During 18-bit data word transfers, a UNIBUS parity error cannot be detected.

**Bit: 12**  
**Name:** Nonexistent Drive (NED)  
**Function:** Nonexistent Drive is a read-only error bit that is set to indicate the following:  
- A Select Acknowledge (SACK) signal from a selected drive has not been asserted on the interface in response to a message (other than a Release) sent to the drive.
- A complete status message (A0-A3, B0-B3) was not received from a selected drive within 20μs of a message request from the controller.

**Bit: 11**  
**Name:** Nonexistent Memory (NEM)  
**Function:** Nonexistent Memory is a read-only error bit that is set when the controller attempts to execute a bus cycle and SSYN is not returned within 10μs of the assertion of MSYN.

**Bit: 10**  
**Name:** Programming Error (PGE)  
**Function:** Programming Error is a read-only bit that is set if any controller register is written (bits for CCLR and SCLR excepted) while the GO bit in RKCS1 is set. The error is disabled in diagnostic mode.

**Bit: 9**  
**Name:** Multiple Drive Select (MDS)  
**Function:** Multiple Drive Select is a read-only error bit that is set by the assertion of the MDS signal line, via the selected drive, when a determination is made that at least one other drive has been simultaneously selected. This bit can only be cleared by a UNIBUS Initialize (INIT) or a Subsystem Clear (SCLR).

**Bit: 8**  
**Name:** Unit Field Error (UFE)  
**Function:** Unit Field Error is a read-only error bit that is set to indicate the following:
The Drive Select code bits (T0-T2) in the current status message (A0-A3) received by the controller did not compare with the Drive Select (DS0-DS2) code transmitted on the Message A line. The setting of this error bit is disabled by diagnostic mode operation.

A Deselect bit (T3) was transmitted to a Drive on the Message A line and the Select Acknowledge (SACK) signal was not negated.

Bit: 7 Name: Output Ready (OR)
Function: Output Ready is a read-only bit that is set to indicate that a word is in the Silo output buffer. The bit is cleared by conventional initialization (INIT, CCLR, SCLR) or by the setting of the GO bit (0 in RKCS1).

Bit: 6 Name: Input Ready (IR)
Function: Input Ready is a read-only bit that is set to indicate that the Silo input buffer is ready to accept a word. Conversely, the bit is reset to indicate that the Silo is full and cannot accept a word. The IR bit is also set by conventional initialization (INIT, CCLR, SCLR) or by the setting of the GO bit (0 in RKCS1).

Bit: 5 Name: Subsystem Clear (SCLR)
Function: When the SCLR bit is set via program control, the controller is cleared and the Initialize line is asserted on the drive interface to clear all of the drives available to the system.

Bit: 4 Name: Bus Address Increment Inhibit (BAI)
Function: When the BAI bit is set via program control, the RKBA Register is prevented from incrementing during data transfers. This is primarily a diagnostic aid.

Bit: 3 Name: Release (RLS)
Function: When the RLS bit is set and a command is initiated, the drive specified by DS0-2 will be released. The bit is used in dual-access configurations to effect the release of a drive from one controller and make it available to the other controller. This is necessary because once a drive is accessed by a specific controller, it is not available to the other unless one second has elapsed since the first controller accessed the drive.

Bit: 2-0 Name: Drive Select (DS0-DS2)
Function: The Drive Select bits are configured (0-7(sub)8) with the unit number of the drive to be currently selected.
Drive Status Register (RKDS) 777 452
The RKDS Register is a read-only register that is used to store the operational status of the selected drive. However, information obtained from the drive is not immediately available to program control until the information is validated (SVAL) by the setting of bit 15, which indicates that a complete status message has been received providing a valid update.

Status information bits set in the RKDS Register can be cleared by conventional initialization (INIT, CCLR, SCLR). However, a Controller Clear (CCLR) operation does not affect status or error condition bits that are currently set in the drives. In addition, a UNIBUS Initialize (INIT) or Subsystem Clear (SCLR) operation can only reset status or error bits in a drive if the associated status or error condition no longer exists.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>Status Valid (SVAL)</td>
<td>Status Valid is a read-only bit that is set to indicate that the bits in both the Drive Status (RKDS) and Error (RDER) registers have been updated for the selected drive with receipt of a complete status message. The bit is cleared by conventional initialization (INIT, CCLR, SCLR): initiating a new command (writing into RKCS1), selecting a new drive (writing into RKCS2), or whenever an Attention signal is asserted by the selected drive status change.</td>
</tr>
<tr>
<td>14</td>
<td>Current Drive Attention (CDA)</td>
<td>Current Drive Attention is a read-only bit that is the logical equivalent of the Drive Status-Change (DSC) bit</td>
</tr>
</tbody>
</table>
in the drive defined by the Drive Select (DS0-DS2) bits in RKCS2. The assertion of the Attention line indicates any one of the following conditions:
Seek operation is completed.
Offset operation is completed.
Heads are unloading (Message A1:T14).
A FAULT condition (Message B0:T7) has been set in the drive which enables the setting of CERR (bit 15 in RKCS1) to indicate one or more of the following:
1. AC low error (Message B0:T6).
2. Nonexecutable function (Message B0:T8).
3. Controller-to-drive message parity error (Message B0:T9).
4. Seek incomplete (Message B0:T10).
   Invalid address (Message B0:T5).
   Seek and no motion (Message B1:T12).
   Limit detected on seek (Message B1:T13).*
   Servo unsafe (Message B1:T14).*
5. Write lock error (Message B0:T11).
6. Speed loss error (Message B0:T12).*
7. Drive off track (Message B0:T13).
8. Read/write unsafe (Message B0:T14).
9. Sector error (Message B1:T4).*
10. Write current/no write gate (Message B1:T5).*
11. Write gate/no transitions (Message B1:T6).*
12. Head fault (Message B1:T7).*
13. Multiple head select (Message B1:T8).*
14. Index error (Message B1:T9).*
15. Tribit error (Message B1:T10).*
16. Servo signal error (Message B1:T11).*

NOTE
A Drive Status-Change (DSC) is also indicated by the setting (Message A0:T14) of bit 14 in RKMR2.

* In addition to setting the CSA bit and asserting Attention, these drive fault conditions will cause the heads to be unloaded.

**Bit: 13  Name:** Positioning in Progress (PIP)
**Function:** Positioning in Progress is a read-only bit that is set (Message A0:T13) to indicate that the heads are in motion.
Bit: 12  Name: Spare
Function: Spare bit 12 is 0.

Bit: 11  Name: Write Lock (WRL)
Function: Write Lock is a read-only bit that is set (Message A0:T11) if the selected drive is write protected.

Bit: 9-10  Name: Spare
Function: Spare bit 9 and 10 are 0.

Bit: 8  Name: Disk Drive Type (DDT)
Function: Disk Drive Type is a read-only bit that is internally conditioned (Message A0:T8) to indicate the type of drive selected. For an RK06 drive, the bit is 0, and for an RK07 drive, the bit is 1. However, before any commands can be executed, the bit must compare with the condition of Controller Drive Type, bit 10 in RKCS1.

Bit: 7  Name: Drive Ready (DRDY)
Function: Drive Ready is a read-only bit that is set (Message A0:T7) to indicate that the selected drive is up to speed and the heads are properly positioned over a valid cylinder. Under these conditions, the drive is prepared to receive a command.

Bit: 6  Name: Volume Valid (VV)
Function: Volume Valid is a read-only bit that is set (Message A0:T6) to indicate that the Volume Valid flip-flop has been set in the selected drive by a Pack Acknowledge command. The set condition of the bit ensures the program that the cartridge and the unit number plug have not been changed since the last command was issued to the drive, and power has not been removed. The bit is reset when the cartridge, the unit number plug, or ac power is removed.

Bit: 5  Name: Drive Off Track (DROT)
Function: Drive Off Track is a read-only bit that is set (Message B0:T13) to indicate that the Write Gate signal has been asserted while the heads are not properly positioned over the track center line.

Bit: 4  Name: Speed Loss (SPLS)
Function: Speed Loss is a read-only bit that is set (Message B0:T12) to indicate that spindle speed is unacceptably low for an unexplained reason.

Bit: 3  Name: Drive AC Low (ACLO)
Function: Drive AC Low is a read-only bit that is set (Message B0:T6) to indicate that ac power in the selected drive is low or has been interrupted. Following detection of an ac low condition, the heads will unload when the next Sector pulse occurs. This action allows the transfer of the current sector to be complete before the heads are unloaded.

Bit: 2  Name: Offset (OFST)
Function: Offset is a read-only bit that is set (Message A0:T10) to indicate that the selected drive is in Offset mode.

Bit: 1  Name: Spare
Function: Spare bit 1 is 0.

Bit: 0  Name: Drive Available (DRA)
Function: Drive Available is a read-only bit that is conditioned (Message A0:T5) to dual-access operation as follows:

• When set by a selected drive, DRA indicates that the drive is available to accept commands from the controller.

• If an attempt is made to select a dual-access drive that is currently accessed by the other controller, the DRA bit will not be set. This is considered an error condition by the controller, resulting in the setting of controller Combined Error (CERR) bit in RKCS1 and the generation of a program interrupt (if enabled).

Drive Error Register (RKER) 777 454
The RKER Register is a read-only register that is used to store the error status of a selected drive. However, error information obtained from the drive is not immediately available to program control until the information is validated (SVAL) by the setting of bit 15 in the RKDS Register, which indicates that a complete status message frame has been received.

Error bits set in the RKER Register can be cleared by conventional initialization (INIT, CCLR, SCLR). However, a Controller Clear (CCLR) operation does not affect error bits that are currently set in the drive. In addition, a UNIBUS Initialize (INIT) or Subsystem Clear (SCLR) operation can only reset error bits in a drive if the associated error condition no longer exists.
Bit: 15  Name: Data Check (DCK)
Function: Data Check is a read-only bit that is set to indicate that a data error was detected when the current sector was read.

Bit: 14  Name: Drive Unsafe (UNS)
Function: Drive Unsafe is a read-only bit that is set (Message B0:T14) to indicate that any one of the following read/write unsafe conditions, each of which causes the heads to be unloaded, has been detected.

1. Sector Error (Message B1:T5) indicates that Write Gate was asserted in the drive in coincidence with the trailing edge of a sector pulse.
2. Write Current/No Write Gate (Message B1:T5) indicates that write current has been detected in the drive without the assertion of Write Gate.
3. Write Gate/No Transitions (Message B1:T6) indicates that the drive received the assertion of Write Gate while no encoded write data has been received.
4. Head Fault (Message B1:T7) indicates that an electrical imbalance exists in the write signals that have been fed to the head, which could cause erroneous data to be recorded.
5. Multiple Head Select (Message B1:T8) indicates that more than one read/write head has been selected simultaneously.
6. Index Error (Message B1:T9) indicates that the once-per-revolution index pulse is either mispositioned or is missing.
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7. Tribit Error (Message B1:T10) indicates that three successive tribits were missing from the servo track.
8. Servo Signal Error (Message B1:T11) indicates that no signals have been detected from the servo head.

In addition to the setting of the UNS bit in the RKER Register, the occurrence of any one of these fault conditions allows the CDA bit to be set in the RKDS Register, the Attention signal to be asserted for the RKAS/OF Register, the DSC bit (Message A0:T14) to be set in RKMR2, and the Fault bit (Message B0:T7) to be set in RKMR3.

Bit: 13  Name: Operation Incomplete (OPI)
Function: Operation Incomplete is a read-only bit that is set to indicate that following the positioning of the heads to a desired cylinder and the reading of 32 headers, the desired header could not be found. This error can result from any one of the following:
1. Head mispositioning
2. Incorrect head selection
3. Read channel failure
4. Improper pack formatting

Bit: 12  Name: Drive Timing Error (DTE)
Function: Drive Timing Error is a read-only bit that is set to indicate the following:
1. The loss of write clock by the controller during a write.
2. The loss of encoded read data by the controller during a read.

Bit: 11  Name: Write Lock Error (WLE)
Function: Write Lock Error is a read-only bit that is set (Message B0:T11) to indicate that the drive received the assertion of the Write Gate signal when it was in Write Protect mode. The occurrence of this fault allows the CDA bit to be set in RKDS, the Attention signal to be asserted for RKAS/OF, the DSC bit to be set in RKMR2, and the Fault bit to be set in RKMR3.

Bit: 10  Name: Invalid Disk Address Error (IDAE)
Function: Invalid Disk Address Error is a read-only bit that can be set via an Invalid Address bit (Message B0:T5) from the drive, or by the controller, to indicate the following:
1. An Invalid Address (Message: B0:T5) bit has been set in the selected drive, indicating that an invalid
cylinder address (411(sub)10 through 511(sub)10 for the RK06 or 815(sub)10 through 1023(sub)10 for the RK07) and/or invalid rack address (3(sub)10) has been detected with the receipt of a seek command.

In addition to setting the IDAE bit, either of these faults will set the SKI bit in the RKER Register; the CDA bit in the RKDS Register (while asserting an Attention signal for RKAS/OF), the DSC bit in RKMR2, and the Fault bit in RKMR3.

2. The controller detected an illegal desired cylinder (DC0-DC9) value (512(sub)10 through 1023(sub)10) in the RKDC Register during the initiation of a command, if the drive (as defined by bit 10 of RKCS1) is an RK06. These cylinder values are allowed only on the RK07.

3. The controller detected an illegal track address (TA0-TA2) value (3(sub)10 through 7(sub)10) in the RKDA Register during the initiation of a command.

**Bit: 9**  **Name:** Cylinder Overflow Error (COE)

**Function:** Cylinder Overflow Error is a read-only bit that is set to indicate that the RKWC Register is not equal to zero following a data transfer from cylinder 410(sub)10 (for RK06) or 815(sub)10 (for RK07), track 2(sub)10, and sector 19(sub)10 or 21(sub)10 (last logical sector).

**Bit: 8**  **Name:** Header Vertical Redundancy Check Error (HRVC)

**Function:** Header VRC Error is a read-only bit that is set to indicate that a VRC error has been detected on a sector header during a data transfer. If the Operation Incomplete (OPI) bit (bit 13) is also set, the sector in which the error occurred cannot be determined. However, if the OPI bit is reset, the VRC error was detected in the sector currently defined by the RKDA Register (SA0-SA4).

**Bit: 7**  **Name:** Bad Sector Error (BSE)

**Function:** Bad Sector Error is a read-only bit that is set to indicate that a data transfer has been attempted to or from a sector that has at least one of the two Good Sector Flag bits (Header Word 2, bits 14 and 15) reset, indicating a bad sector.

**Bit: 6**  **Name:** Error Correction Hard (ECH)
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Function: Error Correction Hard is a read-only bit that is set to indicate that a data error detected by the Error Correction Code (ECC) logic in the controller cannot be corrected using ECC.

Bit: 5 Name: Drive-Type Error (DTYE)

Function: Drive-Type Error is a read-only bit that is set when the drive-type status bit (Message A0:T8) returned from the selected drive does not compare with the CDT bit (bit 10) in RKCS1 (reset for RK06 or set for RK07).

Bit: 4 Name: Format Error (FMTE)

Function: Format Error is a read-only bit that is set when the format status bit (Message A0:T9) returned from the selected drive does not compare with the CFMT bit (bit 12) in RKCS1.

Bit: 3 Name: Control-to-Drive Parity Error (DRPAR)

Function: Control-to-Drive Parity Error is a read-only bit that is set (Message B0:T9) to indicate that the drive detected a parity error on a controller-to-drive message transmission. The occurrence of this fault allows the CDA bit (bit 14) to be set in RKDS, the attention signal to be asserted for RKAS/OF, the DSC bit to be set in RKMR2, and the Fault bit to be set in RKMR3.

Bit: 2 Name: Nonexecutable Function (NXF)

Function: Nonexecutable Function is a read-only bit that is set (Message A0:T8) to indicate that a Seek command or a Write Gate signal has been received by the selected drive while Volume Valid was reset. The occurrence of this fault allows the CDA bit (bit 14) to be set in RKDS, the Attention signal to be asserted for RKAS/OF, the DSC bit to be set in RKMR2, and the fault bit to be set in RKMR3.

Bit: 1 Name: Seek Incomplete (SKI)

Function: Seek Incomplete is a read-only bit that is set (Message B0:T10) to indicate that a seek operation has not been completed for one of the following conditions:

An Invalid Address (Message B0:T5) bit has been set in the drive, indicating that the drive has received an invalid head or cylinder address.

A Seek and No Motion (Message B1:T12) bit has been set in the drive, indicating that a Seek command was
received by the drive but no track crossing pulses were detected with 10ms.

A Limit Detected on Seek (Message B1:T13) bit has been set in the drive, indicating that an inner limit or an outer limit was detected during a Seek operation. If this fault occurs, the heads are unloaded.

A Servo Unsafe (Message B1:T14) bit has been set in the drive, indicating a servo runaway condition. If this fault occurs, the servo actuator is disconnected from the servo drive and connected to a battery that provides the necessary power to drive the heads to the home position.

**Bit: 0  Name:** Illegal Function (ILF)

**Function:** Illegal Function is a read-only bit that is set to indicate that an illegal command (33(sub)8, 35(sub)8, 37(sub)8) has been loaded into RKCS1.

* In addition to setting the CSA bit and asserting Attention, these drive fault conditions will cause the heads to be unloaded.

**Attention Summary/Offset Register (RKAS/OF) 777 456**

The RKAS/OF Register can be read or written via program control and as such is used to store the head offset value required by an Offset command and by the current condition of the Attention signal line that is monitored for each drive.

**Bit: 15-8  Name:** Attention (ATN7-ATN0)

**Function:** The Attention indicators are read-only bits that reflect the unit number of each drive available to the system and the condition of an associated Drive Status Change flip-flop. All of the ATN bits are continuously monitored and updated (polled) every 7.4 μs. Under these conditions and during the update time allotted to a drive, an ATN bit will be set by the assertion of an Attention Line signal if the Drive Status-Change flip-flop is set. Thus, the clearing of the flip-flop within the drive will clear the associated ATN bit. The condition of the Drive Status-Change flip-flop is also noted in the controller by the conditioning (Message A0:T14) of the DSC bit (bit 14) in the RKMR2 Register.

**Bit: 7-0  Name:** Offset (OF0-OF7)

**Function:** The Offset field (OF0-OF7) defines both the magnitude (OF0-OF5) and direction (OF7) of head movement in
relation to the center line of a track. As shown below, each binary increment of the offset value (excluding OF6) produces a move of 25 microinches (for an RK06) or 12.5 microinches (for an RK07) in a positive (+) or negative (−) direction. A positive offset (OF7 = 0) provides head motion toward the spindle, while a negative offset (OF7 = 1) provides head motion away from the spindle. Therefore, an offset value of all zeroes would leave the heads positioned on the center line of a desired cylinder.

**Desired Cylinder Register (RKDC) 777 460**
The RKDC Register can be read or written via program control and is used to store the address of the desired cylinder. Following an initial load, the value in the RKDC Register will be incremented by one whenever the track address (TA0-TA2) value in the RKDA Register overflows during a data transfer. When the RKDC Register is incremented and the RKWC Register is not equal to zero, a single-cylinder seek is initiated by the controller.

**Bit: 15-10**  **Name: Spares**
**Function:** Spare bits 15-10 are zero.

**Bit: 9-0**  **Name: Desired Cylinder (DC0-DC9)**
**Function:** For an RK06 drive, valid cylinder addresses range from the outer edge of the disk (0) to the center (410(sub)10), requiring nine (DC-DC8) address bits to define the range (000-632(sub)8). For an RK07 drive, valid cylinder addresses range from the outer edge of the disk (0) to the center (815(sub)10), requiring ten (DC0-DC9) address bits to define the range (000-1456(sub)8).

**Data Buffer Register (RKDB) 777 464**
The RKDB Register can be read or written via program control. Reading from the register empties the Silo, while writing into the register fills the Silo. Both RKDB Register and the Silo are cleared by conventional initialization (INIT, CCLR, SCLR).

**Maintenance Register (RKMR1) 777 466**
The RKMR1 Register can be read or written via program control and is primarily used to provide an operational analysis of the sub-system (i.e., RK611 controller and the selected drive). This includes drive message analysis and parity testing and the initiation of a Diagnostic mode (DMD) of operation in which the controller can be isolated and exercised.
Bit: 15  Name: Write Gate (WRT GT)
Function: Write Gate is a read-only bit that is set to indicate that Write Gate has been asserted by the controller.

Bit: 14  Name: Read Gate (RD GT)
Function: Read Gate is a read-only bit that is set to indicate that Read Gate has been asserted by the controller.

Bit: 13  Name: ECC Word (ECCW)
Function: ECC Word is a read-only bit that is normally set in the controller. A reset condition of the bit indicates that the timing logic is reflecting the ECC field within the sector.

Bit: 12  Name: Precompensation Delay (PCD)
Function: Precompensation Delay is a read-only bit that is set to indicate that write precompensation logic within the controller has determined that the pulse required to record the current data bit must be delayed in time to ensure the reliability of the bit during subsequent reads.

Bit: 11  Name: Precompensation Advance (PCA)
Function: Precompensation Advance is a read-only bit that is set to indicate that write precompensation logic within the controller has determined that the pulse required to record the current data bit must be advanced in time to ensure the reliability of the bit during subsequent reads.

Bit: 10  Name: Maintenance-Encoded Write Data (MEWD)
Function: The MEWD bit is a read-only bit that is normally unconditionally set by the controller. A reset condition of the bit, when read in conjunction with the setting of DMD, indicates that the encoding logic has functioned properly during the simulated execution of a Write command.
Bit: 9  Name: Maintenance-Encoded Read Data (MERD)
Function: When DMD is set, MERD is used to simulate encoded serial data.

Bit: 8  Name: Maintenance Clock (MCLK)
Function: When DMD is set, MCLK replaces the internal controller clock derived from the data separator. The toggling (set, reset, etc.) of MSLK provides the clock pulses required to step through a controller command, including the simulated reading or writing of data.

Bit: 7  Name: Maintenance Index (MIND)
Function: When MIND is set in conjunction with the setting of the DMD bit, the receipt of an index pulse from a drive is simulated.

Bit: 6  Name: Maintenance Sector Pulse (MSP)
Function: When MSP is set in conjunction with the setting of the DMD bit, the receipt of a sector pulse from a drive is simulated.

Bit: 5  Name: Diagnostic Mode (DMD)
Function: When the Diagnostic mode bit is set, the controller is effectively disconnected from all of the drives and placed under the control of specific bits in the RKM01 Register (i.e., MSP, MIND, MCLK, MERD).

Bit: 4  Name: Parity Test (PAT)
Function: When the Parity Test bit is set, the controller is forced to generate even parity for the messages sent to the drive on the Message A and Message B lines. Similarly, the controller makes an even parity check on the status messages return from the drive.

Bit: 3-0 Name: Message Select (MS0-MS3)
Function: The RK06 or RK07 Message Select (MS0 and MS1) bits define one of the four pairs of 16-bit status messages (A0-A3 and B0-B3) that can be simultaneously delivered to the controller on the Message A and Message B lines. When both messages are defined by the equivalent value, Message A is sent to the RKM02 Register as Message B is simultaneously sent to the RKM03 Register. The select bits are cleared by conventional initialization or by loading a command (other than Select Drive) into RKCS1.
ECC Position Register (RKECPS) 777 470
The Error Correction Code (ECC) Position Register is a read-only register that is used to store the error position value, which results from the successful execution of an ECC correction sequence. When an ECC correction sequence is not in progress, the RKECPS Register contains one of two possible values (004066(sub)8 or 005066(sub)8). If the CFMT bit (bit 12) in RKCS1 is reset reflecting a 22-sectort format (16-bit data words), the lesser value is contained in the register. However, if the CFMT bit is set, reflecting a 20-sector format (18-bit data words), the greater value is contained in the register.

Bit: 15-13 Name: Spares
Function: Spare bits are zero

Bit: 12-0 Name: Error Position (EP00-EP12)
Function: The Error Position bits are read-only bits that define the start bit location of an error burst (containing from 1 to 11 error bits) within a 256-word data field, following the completion of an ECC correction sequence. The position is valid if the error is ECC-correctable. If the detected error is not correctable using ECC, the register contains a constant (010040(sub)8).

ECC Pattern Register (RKECPT) 777 472
The Error Correction Code (ECC) Pattern Register is a read-only register that contains an 11-bit error correction pattern from the ECC polynomial generator. The pattern is valid if the error is ECC-correctable.

Bit: 15-11 Name: Spares
Function: Spare bits are zero.

Bit: 10-0 Name: Error Pattern (EPA10-EPA0)
Function: The Error Pattern bits are read-only bits that provide an 11-bit correction pattern for an error burst that does not exceed 11 bits in length and is, therefore, ECC-correctable.

Maintenance Register 2 (RKMR2) 777 474
RKMR2 is a read-only register that is used for Message A controller-to-drive transmission (commands), as well as Message A0-A3 drive-to-controller transmission (status).

Controller-to-Drive (Message A)—For controller-to-drive transmission, the 16-bit Message A shift register assembles disk commands, along with an appropriate odd parity bit, from various de-
vice registers and command logic within the controller. As the bits are assembled in the register, they are serially transmitted to the drives in coincidence with the transmission of Message B, with each bit position (0-15) directly related to an equivalent transmission time (T0-T15).

**Drive-to-Controller (Message A0-A3)**—For drive-to-controller transmissions, the 16-bit Message A shift register assembles status information, along with an appropriate odd parity bit, from various status and error registers within the drive. As the bits are serially transmitted from the drive in coincidence with Message B status bits, they are assembled in the register with each bit position relating directly to an equivalent transmission time.

**Maintenance Register 3 (RKMR3) 777 476**
RKMR3 is a read-only register that is used for Message B drive-to-controller transmissions (additional command parameters), as well as Message B0-B3 drive-to-controller transmissions (status).

**Controller-to-Drive (Message B)**—For controller-to-drive transmissions, the 16-bit Message B shift register assembles additional disk command information (including the status message request numeric of 0, 1, 2, or 3), along with an appropriate odd parity bit, from various device registers and command logic within the controller. As the bits are assembled in the register, they are serially transmitted to the drives in coincidence with the transmission of Message A, with each bit position (0-15) directly related to an equivalent transmission time (T0-T15). For additional information, refer to Paragraph 2.5.1.

**Drive-to-Controller (Message B0-B3)**—For drive-to-controller transmissions, the 16-bit Message B shift register assembles status information, along with an appropriate odd parity bit, from various status and error registers within the drive. As the bits are serially transmitted from the drive in coincidence with the Message A status bits, they are assembled in the register with each bit position relating directly to an equivalent transmission time.

Since only one of four status messages can be stored in the Message B shift register at a time, a desired message (B1-B3), other than B0, must be previously defined by the execution of a Select Drive command.

**NOTE**
Maintenance Registers 2 (RKMH2) and 3 (RKMR3) only contain valid status messages following the execution of a Select command.
DIGITAL's low cost, small capacity cartridge disk subsystem combines current technology with reliability and maintenance features specifically designed to offer a low price feature.

FEATURES

- **Capacity:**
  5.2 million bytes per drive (formatted)
  20.8 million bytes per subsystem
  41.6 million bytes per CPU

- **Performance:**
  55 milliseconds average seek time
  512 bytes per second transfer rate
  3.9 microseconds per word peak transfer rate
  Direct Memory Access

- **Reliability:**
  Track following embedded servo system
  CRC checking on all data transfers between drive and controller
  Simplified modular construction
  Easy access to subassemblies and heads

DESCRIPTION

The RL01 is a top-loading, rack-mounted, cartridge disk drive. Each drive can store up to 5.2 million bytes; an RL01 subsystem
can include up to four drives. Average access time, including head positioning and rotational latency, is less than 68 milliseconds. Cartridge interchangeability is assured by the data integrity design features. An embedded closed-loop servo positioning system provides the RL01 with improved data integrity and reliability since the servo information is continuously sampled by the same head that reads and writes the data. Reliable read and recording techniques are assured by a phase locked-loop clock system and modified frequency modulation (MFM) recording. Cyclical Redundancy Checking (CRC) is performed on all data transferred to and from the disk.

The pack is formatted at the factory with servo and header data that cannot be modified or rewritten in the field. The subsystem protects against accidental writing in the servo and header areas, insuring pack integrity.

From its inception, the RL01 disk drive was designed to be especially reliable and easy to service. These design prerequisites have resulted in a drive that has few failures and requires less time for repairs. This means a significant reduction in total cost of ownership.

The design of the drive subsystem itself is extremely simple. There are only five printed circuit boards in the drive itself, and only eleven major subassemblies. Since all mechanical adjustments are set at the factory, there are only two adjustments that may ever have to be made to the drive during use. Circuits are designed to tolerate wide voltage fluctuations. Low component density and its own powerful high volume recirculating forced air cooling and filter system for the drive and cartridge mean fewer electronic failures. These features also allow the RL01 to function within a wide range of temperature and humidity variations.

To increase maintenance ease, the drive is mounted on tracks that slide out, making all subassemblies and heads accessible from the top of the unit.

RL01 subsystems feature a universal power supply. Using a different line cord plug and inverting a connector on the rear of the unit converts the drive from 115 volts/50-60 Hz to 230 volts/50-60 Hz. The drives are UL listed, CSA certified, and meet IEC 435 requirements.

Disk Cartridge
The storage medium of the RL01 is a 5440 type disk cartridge. It has one platter with two recording surfaces, each containing 256
tracks. The disk is formatted in forty sectors per track. Each sector contains the servo information, a header field, and a 256 byte data field. The prerecorded servo information is interspersed with the data and thus is read with the same head that reads and writes data. This way no cartridge surface is reserved for only servo information, both surfaces of the cartridge are used for data recording.

The disk cartridge is designed for both convenience and reliability. When stored, the impact-resistant plastic cartridge completely encloses and seals the recording surfaces against dirt and contamination. Lightweight and easy to carry, the disk cartridge may be stacked three high for storage convenience. Since the cartridge is top loading and magnetically secured and aligned to the drive, it can be mounted easily and securely.

Subsystem Configuration
The typical RL01/RL11 mass storage subsystem consists of up to four RL01 disk drives connected in a daisy-chain configuration and a disk controller. Additional drives, if required, necessitate a second controller.

Basic functions of the disk drive are as follows:
• store and retrieve data in accordance with controller commands
• generate control and timing signals for transferring data between controller and drive
• generate a status message describing drive operational conditions

Basic functions of the controller are:
• to interpret and execute drive commands
• to control the flow of data between the UNIBUS and the drives
• to route status information from the drives to the UNIBUS
• to provide error flags and fault indications related to overall subsystem operation
• to perform parallel/serial data conversion, error detection, and all the other control and timing functions related to high-speed random access data storage and retrieval.

The RL01 disk controller is a single hex module that can be installed in any small peripheral controller (SPC) slot.

The controller has a repertoire of eight commands. These are all the commands necessary for reading and writing data, and for performing other operational functions.
**Name of Command** | **Basic Function**
--- | ---
No Operation | Diagnostic tool for exercising controller sequence logic.
Write Check | Reads a block of data and compares it with a block of data in memory.
Get Status | Obtains status word from device.
Seek | Causes drive to seek to desired track and/or select a new head.
Read Header | Reads first header encountered on selected disk track.
Write Data | Writes serial data on selected disk track.
Read Data | Reads serial from selected disk track.
Read Data Without Header Check | Reads serial data from selected disk track without performing header comparison. (This enables data recovery in case a header is not found.)

The controller contains four UNIBUS word-addressable registers.
The address, read/write capability, and function of each register are summarized in Table X-X.

The contents of the disk address (DA) and multipurpose (MP) registers have different meanings, depending on the command being executed.

Bit configurations and functions are detailed in Chapter 4 of this manual.

### RL11 Addressable Registers

<table>
<thead>
<tr>
<th>Address (Octal)</th>
<th>Type (read/write)</th>
<th>Register Name/Mnemonic</th>
<th>Basic Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>774 400</td>
<td>R/W</td>
<td>Control Status (CS)</td>
<td>Indicates drive ready condition; decodes drive commands and provides overall control functions and error indications.</td>
</tr>
<tr>
<td>774 402</td>
<td>R/W</td>
<td>Bus Address (BA)</td>
<td>Indicates memory location involved in data transfer during a normal read or write operation.</td>
</tr>
<tr>
<td>774 404</td>
<td>R/W</td>
<td>Disk Address (DA)</td>
<td>Stores information for: (1) seeking to desired track; or (2) selecting sectors to be transferred during read/write operations. Also used when requesting a drive status message.</td>
</tr>
<tr>
<td>Address (Octal)</td>
<td>Type (read/write)</td>
<td>Register Name/Mnemonic</td>
<td>Basic Function</td>
</tr>
<tr>
<td>----------------</td>
<td>------------------</td>
<td>------------------------</td>
<td>----------------</td>
</tr>
<tr>
<td>774 406</td>
<td>R/W</td>
<td>Multipurpose (MP)</td>
<td>Functions as word counter when transferring read/write data between UNIBUS and drives. Acts as storage buffer when reading drive status or header information from controller silo.</td>
</tr>
</tbody>
</table>

In addition to the four addressable registers and standard UNIBUS handshaking logic, there is: a first-in first-out silo to compensate for the different data transfer rates between the UNIBUS and the drive(s); a write percompensation circuit for offsetting the effects of peak shifting normally associated with modified frequency modulation (MFM) encoded recording; a phase lock loop circuit to compensate for variations in disk speed; a data separation circuit for decoding separate clock and nonreturn to zero (NRZ) data signals from the drive MFM encoded serial data; a header compare circuit for locating headers on the recording surfaces; and a cyclic redundancy check (CRC) circuit for detecting header and data recording errors. In addition, there are two control circuits, labeled function control and format control. Each of these controls has a binary counter that addresses two read only memories (ROMs) and thus provides the necessary ROM output control signals in the proper sequence for command execution. The function control is operative during execution of all eight commands. The format control is only operative during execution of those commands associated with the actual transfer of header information or read/write data. In a typical read/write application, the function control starts to count, sets up various control conditions, reaches a predetermined state, and stops. The format control then takes over, establishes the necessary word boundaries, controls the actual transfer of header information and data, and then causes operation to revert back to the function control for command completion.
REGISTERS
Control Status Register 774 400
In the Control Status Register, bits 1 through 9 can be read or written, the other bits can only be read.

Bit: 0     Name: Drive Ready (DRDY)
Function: When set, this bit indicates that the selected drive is ready to receive a command. The bit is cleared when a seek operation is initiated and set when the seek operation is completed.

Bit: 1-3   Name: Function Code
Function: These bits are set by software to indicate the command to the executed.

<table>
<thead>
<tr>
<th>F2</th>
<th>F1</th>
<th>F0</th>
<th>Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>No Op</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Write Check</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Get Status</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>Seek</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>0</td>
<td>Read Header</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>Write Data</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td>Read Data</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
<td>Read Data Without Header Check</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Command execution requires that bit 7 of the same word be cleared by software. In a sense, then, bit 7 can be considered as a negative Go bit.

**Bit: 4-5**  
**Name:** Bus Address Extension Bits  
**(BA16, BA17)**  
**Function:** Two upper-order bus address bits. Read and written as data bits 4 and 5 of the CS register but considered as address bits 16 and 17 of the BA register.

**Bit: 6**  
**Name:** Interrupt Enable (IE)  
**Function:** When this bit is set by software, the controller is allowed to interrupt the processor at the normal command or error termination.

**Bit: 7**  
**Name:** Controller Ready (CRDY)  
**Function:** When cleared by software, this bit indicates that the command in bits 1-3 is to be executed. When set, this bit indicates the controller is ready to accept another command.

**Bit: 8-9**  
**Name:** Drive Select (DS0, DS1)  
**Function:** These bits determine which drive will communicate with the controller via the drive bus.

**Bit: 10**  
**Name:** Operation Incomplete (OPI)  
**Function:** When set, this bit indicates that the current command was not completed within 200 ms.

**Bit: 11**  
**Name:** Data CRC (DCRC) or Header CRC (HCRC)  
**Function:** If OPI (bit 10) is cleared and bit 11 is set, the CRC error occurred on the data (DCRC). If OPI (bit 10) is set and bit 11 is also set, the CRC error occurred on the header (HCRC).

If OPI (bit 10) is cleared and bit 11 is set and the function command is write check, the CRC error denotes a write check error.

Cyclic redundancy checking is performed on the first and second header words, even though the second header word is always zero.

**Bit: 12**  
**Name:** Data Late (DLT) or Header Not Found (HNF Error)  
**Function:** When OPI (bit 10) is cleared and bit 12 is set, it indicates that, on a write operation, the silo was empty and, therefore, a word was not available for writing; or, on a read operation, that the silo was full and unable to store another word from the drive.
Bit: 13  Name: Non-Existent Memory (NXM)
Function: When set, this bit indicates that, during a direct memory access (DMA) data transfer, BSYNCL was not received within 10 to 20 μsec.

Bit: 14  Name: Drive Error (DE).
Function: This bit is tied directly to the DE interface line. When set, it indicates that the selected drive has flagged an error, the source of which can be determined by executing a Get Status command.
One way to clear the DE is to reset the drive error register (e.g., by setting bit 3 of the Get Status command word).

Bit: 15  Name: Composite Error
Function: When set, this bit indicates that one or more of the error bits (bits 10-14) is set. If the IE bit (bit 6 of CS) is set and an error occurs, the current operation will terminate and the interrupt routine will be initiated.

Bus Address Register 774 402
In this, bits 1 through 15 can be read or written, bit 0 is always zero.
The Bus Address register indicates the memory location involved in the data transfer during a normal read or write operation. The contents of the register are automatically incremented by two when each word is transferred between the UNIBUS and the drive. The register overflows into Control Status register bits 4 and 5. A BUS INIT or loading the register with zeros clears the Bus Address register.

Disk Address Register 774 404
The contents of the Disk Address Register vary in meaning depending on which operation: seek, read/write or get status is being performed.

Disk Address Register During a Seek Command

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYLINDER ADDRESS DIFFERENCE</td>
<td>RESERVED</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Bit: 0**  Name: —
- **Function:** Must be a 1.
Bit: 2  Name: Direction (DIR)
Function: This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 7-14).

Bit: 3  Name: —
Function: Must be a 0.

Bit: 4  Name: Head Start (HS)
Function: Indicates which head (disk surface) is to be selected. Set = lower, clear = upper.

Bit: 5-6  Name: —
Function: Reserved

Bit: 7-14  Name: Cylinder Address Difference [DF(07:00)]
Function: Indicates the number of cylinders the heads are to move on a seek.

Bit: 15  Name: —
Function: Must be a 0.

Disk Address Register During a Read or Write Data Command
For a read or write operation, the Disk Address register is loaded with the address of the first sector to be transferred. After that, when each adjoining sector is transferred, the Disk Address register is automatically incremented by one.

![Diagram of Cylinder Address and Sector Address](image)

Bit: 0-5  Name: Sector Address
[SA (5:0)]
Function: Address of one of the 40 sectors on a track.

Bit: 6  Name: Head Select (HS)
Function: Indicates which head (disk surface) is to be selected. Set = lower; clear = upper.

Bit: 7-14  Name: Cylinder Address
[CA(7:0)]
Function: Address of one of the 256 cylinders. (Octal range is 0 to 377.)

Bit: 15 Name: —
Function: Must be a 0.

Disk Address Register During Get Status Command

Bit: 0 Name: —
Function: Must be a 1.

Bit: 1 Name: Get Status (GS)
Function: Must be a 1, indicating to the drive that its status word is being requested. At the completion of the Get Status command, the drive status word is read into the controller Multipurpose register (output stage of silo). With this bit set, bits 8-15 are ignored by the drive.

Bit: 2 Name: —
Function: Must be a 0.

Bit: 3 Name: Reset (RST)
Function: When this bit is set, the drive clears its error register before sending a status word to the controller.

Bit: 4-7 Name: —
Function: Must be a 0.

Bit: 8-15 Name: —
Function: Not used.

Multipurpose Register
The contents of the Multipurpose Register vary depending on which function is being performed: get status, read header, or read/write data.
Multipurpose Register During Get Status Command

Bit: 0-2  Name: State (C:A)  
[ST(C:A)]

Function: These bits define the state of the drive.

<table>
<thead>
<tr>
<th>C</th>
<th>B</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Bit: 3  Name: Brush Home (BH)

Function: Asserted when the brushes are not over the disk.

Bit: 4  Name: Heads Out (HO)

Function: Asserted when the heads are over the disk.

Bit: 5  Name: Cover Open (CO)

Function: Asserted when the cover is open or when the dust cover is not in place.
Bit: 6  Name: Head Select (HS)
Function: Indicates the currently selected head. Clear = upper head; set = lower head.

Bit: 7  Name: Reserved
Function: Will be 0.

Bit: 8  Name: Drive Select Error (DSE)
Function: Indicates multiple drive selection is detected.

Bit: 9  Name: Volume Check (VC)
Function: Indicates the transition from a head load state to a head on track state.

Bit: 10 Name: Write Gate Error (WGE)
Function: Indicates the drive sensed. Write Gate is asserted when Sector Pulse is asserted.

Bit: 11 Name: Spin Error (SPE)
Function: Indicates the spindle is not reaching speed in the required time.

Bit: 12 Name: Seek Time Out (SKTO)
Function: Indicates the heads did not come on track in the required time during a seek command.

Bit: 13 Name: Write Lock (WL)
Function: Indicates Write Lock status of selected drive.

Bit: 14 Name: Current Head Error (CHE)
Function: Indicates write current was detected in the heads when Write Gate was not asserted.

Bit: 15 Name: Write Data Error (WDE)
Function: Indicates Write Gate was asserted but no transitions were detected on the Write Data line.

**Multipurpose Register During a Read Header Command**—When a Read Header command is executed, three words will be stored in the MP register (silo). The first header word will contain sector address, head select, and cylinder address information. The second word will contain all zeros. The third word will contain the header CRC information. All three words are readable by the program.

**Multipurpose Register During Read/Write Data Command for Word Count**—When reading or writing data, the word count is loaded with the 2's complement of the number of words to be
DISKS

RL01

transferred, and is then incremented by 1 as each word is transferred. The reading or writing operation generally is terminated where word counter overflows. The word counter can keep track of from 1 data word to the full 40-sector count of 5120 data words (decimal).

The RL01 disk drive will not do spiral read/writes. The program must break up a data transfer so that the required data from each track is read. In between each data transfer, a seek to the next track or surface must be made. Thus, the maximum data transfer that can be made is 5120 words but, in most cases, it will be less. Also, data cannot be transferred beyond sector 40 without breaking up the transfer into two operations (e.g., sectors 19-40 and 0-10).

Bit: 0-12  Name: Word Count (WC)
Function: 2's complement of total number of words to be transferred.

Bit: 13-15  Name: Word Count (WC)
Function: Must be a 1 for word count in correct range.

SPECIFICATIONS

RL01 Disk Drive Physical and Environmental Specifications

Width
Compatible with 48.26 cm (19 in) RETMA rack

Depth  
63.5 cm (25 in) behind bezel

Height  
26.52 cm (10.44 in)

Weight  
34.02 kg (75 lb)

Mounting  
The drive mounts on chassis slides.

Power Source  
90-127 Vac (47-63 Hz)
180-254 Vac (47-63 Hz)
(Manually selectable)

Input Power  
160 W max at 115 Vac, 60 Hz

Power Factor  
Greater than 0.85

Starting Current  
3.5 A rms max @ 90 Vac/47-63 Hz
5.0 A rms max @ 127 Vac/47-63 Hz
1.75 A rms max @ Vac/47-63 Hz
2.5 A rms max @ 254 Vac/47-63 Hz

Heat Dissipation  
600 Btu/hr max

Power Cord and Connector  
A molded line cord compatible with the drive operating voltage and the 861 power
control for 120 Vac is attached to the drive. The Power cord is 2.74 m (9 ft) long and the plug is NEMA 5-15P.

Safety
The RL01 disk drive is UL listed and CSA certified.

Interlocks
Interlocks are used where potential exists for damage to drive, media, operators, or service personnel.

Temperature/Humidity

Operating
Temperature: $10^\circ \text{C} (50^\circ \text{F})$ to $40^\circ \text{C} (104^\circ \text{F})$
Relative Humidity: 10 to 90 percent with maximum wet bulb temperature $28^\circ \text{C} (82^\circ \text{F})$ and minimum dew point $2^\circ \text{C} (36^\circ \text{F})$

Non-Operating
Temperature: $-40^\circ \text{C} (-40^\circ \text{F})$ to $66^\circ \text{C} (151^\circ \text{F})$
Relative Humidity: 10 to 95 percent, non-condensing

Altitude

Operating:
Altitude: 2440 m (8,000 ft) max

Non-Operating:
Altitude: 9.1 km (30,000 ft) max

Shock

Operating:
Half sine shock pulse of gravity peak and $10 \pm 3$ ms duration applied once in either direction of three orthogonal axes (3 pulses total).

Non-Operating:
Half sine shock pulses of 40 gravity peak and $30 \pm 10$ ms duration perpendicular to each of six package surfaces.

Vibration

Operating:
Sinusoidal vibration (sweep rate 1 octave/min)
5-50 Hz, 0.002 in displacement amplitude
50-500 Hz, 0.25 gravity peak
500-50 Hz, 0.25 gravity peak
50-5 Hz, 0.002 in displacement amplitude

Non-Operating:
Vertical Axis Excitation—1.40 gravity rms
DISKS

RL01

overall from 10 to 300 Hz. Power spectral density of 0.029 g**2/Hz from 10 to 50 Hz, with 8 dB/octave rolloff from 50 to 300 Hz.

Longitudinal and Lateral Axis Excitation—0.68 gravity rms overall from 10 to 200 Hz. Power spectral density of 0.007 g**2/Hz from 10 to 50 Hz, with 8 dB/octave rolloff from 50 to 200 Hz.

EMI
To be supplied.

Dust
To be supplied.

Attitude
Maximum pitch: ±5 degrees
Maximum roll: ±5 degrees

General
Linear bit density: 3725 bits/in at track 255 (decimal)
16 bit words per sector: 128
Number of sectors per surface: 40
Track density: 125/in
Number of tracks per surface: 256
Number of surfaces: 2
Formatted capacity (megabytes): 5.2
Encoding method: MFM

Transfer Rate (Unbuffered Values)
Bit rate: 4.1 megabits/second ±1 percent
Bit cell width: 244 ns ±1 percent
Words (16 bit): 256 kilowords/second ±1 percent

Latency
Rotational frequency: 2400 rpm
Average latency: 12.5 ms
Maximum latency: 25.0 ms

Seek Time
Average seek time (85 tracks): 55 ms max
One track seek time: 15 ms max
Maximum seek time (256 tracks): 100 ms max
Head switching time: 8 ms max

Start/Stop Time
Start time: 40 seconds
Stop time: 30 seconds

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DISKS

Operating Environment
The operating temperature of the air surrounding the cartridge lies within the 40°C to 48°C (40°F to 120°F) range at relative humidity of 8 to 80 percent. The wet bulb reading shall not exceed 25°C (78°F). Before a cartridge is placed in operation, it should be conditioned within its cover for a minimum of 2 hours in the same environment as that in which the disk drive is operating. The above specified range does not necessarily apply to the disk drive.

Storage Environment
The storage temperature lies within the −40°C to 65°C (−40°F to 150°F) range, the wet bulb reading not exceeding 29°C (85°F). For wet bulb temperatures between 0.56°C and 29°C (33°F and 85°F) the disk cartridge shall be able to withstand relative humidity of 8 to 80 percent. The stray magnetic field intensity shall not exceed 50 Oe.

Dimensions (Cartridge)

External Diameter
The external diameter of the top cover is 38.35 cm (15.1 in).

The external diameter of the protection cover is 37.03 cm (14.5 in).

The external height of the cartridge when resting on its bottom surface is 6.19 cm (2.44 in).

Maximum Speed
The rotating parts of the disk cartridge are capable of withstanding the effect of stress at the speed of 2,500 rev/min.

Track Geometry
Number of Tracks—There are 256 discrete concentric tracks per data surface.

Identification of Data Tracks
Data Track Identification—Data track identification is a three digit decimal number (000-255) that numbers data tracks consecutively starting at the outermost data track of each data surface.

Data Surface Identification—The data surfaces are numbered 0 and 1 starting
with the uppermost surface and corresponding with the head numbers.

Cylinder Address—A cylinder is defined as the data tracks on the data surface with a common data track identification.

Data Track Address—A 16-bit work, where bits 0-5 define a binary sector number, bit 6 defines surface, and bits 7-15 define a binary cylinder address. This information is in word 1 of each sector’s header.

### RL11 Controller Specifications

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required Mounting Space</td>
<td>One hex height module, which may be mounted in SPC slot.</td>
</tr>
<tr>
<td>Power Requirements</td>
<td></td>
</tr>
<tr>
<td>+5 Vdc ± 5% @ 5 A</td>
<td></td>
</tr>
<tr>
<td>+15 Vdc ± 1% @ 0.5 A</td>
<td></td>
</tr>
<tr>
<td>−15 Vdc ± 1% @ 0.5 A</td>
<td></td>
</tr>
<tr>
<td>No. Drives/Controller</td>
<td>Up to 4</td>
</tr>
<tr>
<td>No. UNIBUS Addressable Registers</td>
<td>4</td>
</tr>
<tr>
<td>Device Base Address</td>
<td>774 400 (octal), jumper selectable</td>
</tr>
<tr>
<td>Device Interrupt Vector</td>
<td>000 330 (octal), jumper selectable</td>
</tr>
<tr>
<td>Interrupt Priority</td>
<td>Level 5 (plug selectable)</td>
</tr>
<tr>
<td>Data Transfer Rates</td>
<td>40 sector (16-bit data words):</td>
</tr>
<tr>
<td></td>
<td>3.7 us/word (average)</td>
</tr>
<tr>
<td></td>
<td>3.9 us/word (peak)</td>
</tr>
<tr>
<td></td>
<td>Double cycle control</td>
</tr>
<tr>
<td>Error Detection Capability</td>
<td>Cyclic redundancy checking (CRC)</td>
</tr>
<tr>
<td>Maximum cable length between controller and last drive</td>
<td>30.48 m (100 ft)</td>
</tr>
</tbody>
</table>
The RM02 and RM03 disk drives offer the performance required for data base intensive applications. The RM03's transfer rate is efficiently utilized by the PDP-11/70 and larger systems. The RM02 is used on the PDP-11/43 through the PDP-11/60 systems. The capacity, features, and appearance of the RM02 and RM03 are otherwise identical.

FEATURES
- Capacity: 67 million bytes per disk pack
- Performance:
  RM02: 30 milliseconds average seek time
         12.5 milliseconds average latency
         806,000 bytes per second peak transfer rate.
  RM03: 30 milliseconds average seek time
         8.3 milliseconds average latency
         1,200,000 bytes per second peak transfer rate.
DISKS

RM02/RM03

• Reliability:
  subsystem parity checking
  header error detection
  data error detection and correction
  program controlled head offset positioning

DESCRIPTION
The RM02/03 disk subsystem has a formatted capacity of 67 megabytes. The drive resides in a free-standing cabinet, and is compatible with the following controllers: the RJM02, for the smaller 11s and RWM03 for the 11/70.

A common 14-inch diameter removable disk pack with five platters is used by both the RM02 and RM03 drives. The top and bottom platters are nonfunctional, protective covers for the three inner disks. The six surfaces of these three disks are divided into five data storage surfaces and one servo track surface.

Subsystem Features and Capabilities—Since the same pack with the same reading format is used by both drives, data can be easily interchanged between RM02 and RM03 disk subsystems. All RM02s and RM03s have error detection and error isolation operations performed on all information (data and header) read from the disk. This feature permits the software to correct detected errors and recover data that would otherwise be incorrect.

The drives also have the ability to accept offset commands that cause the heads to move off the track centerline in a program-controlled attempt to recover data that is not normally recoverable. The offset distance is a fixed 200 µin on either side of the track centerline.

Data is recorded on the disk in 32 sectors for 16 bit formats. Each sector contains unique cylinder, sector, and track information encoded in a header block. This block also has provisions for accepting manufacturer- or user-specified codes to indicate that the sector is unacceptable for data storage.

The RM02 and RM03 incorporate a unique integrated backplane that permits dual-port, matched-impedance, MASSBUS connections to be made directly onto the backplane. This eliminates the requirements for multiple internal cables for the interface. This integrated backplane also simplifies the interconnections of MASSBUS cables, as up to eight RM02s and RM03s can be daisy-chained from a controller.
Extensive diagnostic programs are available for maintenance procedures. An off-line tester is also available to isolate drive-associated faults.

Recording on the disk is by the Modified Frequency Modulation method, commonly referred to as the Miller-Encoded Recording Technique.

The RM02 or RM03 disk subsystem also offers a dual-port capability, enabling it to be accessed through two different controllers.

**Figure 4-4  Dual Port Subsystem Configuration**

**Subsystem Configuration**—Each RM02 or RM03 disk subsystem is composed of two hardware elements: the RM02/03 adapter and a storage module drive (SMD). Both of these subsystem elements are located within a single cabinet.

To operate this disk system, a high-speed controller is needed to interface to the computer memory bus. This provides a high-speed
path for direct memory transfers. Each controller can handle anywhere from one to eight RM02 or RM03 disk subsystems.

The smaller PDP-11s use the RH-11 controller.

The PDP-11/70 uses the RH70 controller.

**System Operation**—Whenever a data transfer occurs, the following decisions are made:
- which drive is to be used and at what position on that drive is the desired data location?
- what method is to be used to access this data location?
- what is the direction of transfer (read or write)?

The commands generated by the processor to accomplish the results of these decisions occur through the controller. Some of these commands are used to condition the controller circuits for the type of operation, and other commands are routed to the drive where they are used to position the heads over the correct location.

Up to eight RM03s can be connected to a single controller and up to eight RM02s can be connected to a single controller. Since all of these drives have the same address, the processor must designate to the controller which drive is to be used. Only the selected drive decodes the position commands (cylinder location, sector number, and track number) required to mechanically position the heads.

Prior to issuing the positioning commands to the drive, the processor establishes how these commands are to be executed.

The drive starts its mechanical positioning after receiving the cylinder, sector, and track values plus a command containing the GO bit. The drive notifies the processor through the controller when it locates the desired position or if it could not find it. No flag is given on an implied seek in a data transfer command. If no error condition exists, the processor now initiates the data transfer sequence.

Prior to transferring data, the processor configures the controller for the following:
- number of data words to be transferred
- format of these words (16 bit word or 18 bit word)
- if a write operation, the bus address of the starting memory location from which data is taken and placed on the disk
DISKS

RM02/RM03

- if a read operation, the bus address of the first memory location where the data taken from the disk is to be stored
- the method of notifying the processor the data transfer is complete

The processor now initiates a data transfer command that contains the GO bit and the data transfer begins. The data transfer command may or may not contain the same position information (cylinder, sector, and track values) just sent to the drive.

When the heads are at the correct location and the command is a read operation, serial data is read off the disk, converted to parallel in the drive, and applied onto the bus lines to the controller. This first word is routed through the controller to the computer bus, then to the memory location established by the processor. As successive words are read, the controller monitors the handling of each word and increments the memory address to the next location and decrements the word count for each word. The controller terminates the read operation in the drive when the word count is complete.

A write operation is very similar to a read operation. The major difference is the direction of data flow: from memory to the disk. Again, the correct disk position must be located, the number of words to be transferred must be supplied to the controller, the format must be established, and the memory location from which these words are to be taken must be determined. At the completion of a write operation the controller interrupts the processor to indicate that the data transfer is finished.

MASSBUS Protocol for Control Sequences—All control communications on the MASSBUS interface lines between the controller and the drive must conform to the MASSBUS protocol sequence. The following six groups of lines establish the control sequence between the controller and the drive.

1. Drive Select lines
2. Register Select lines
3. Control lines
4. Control to Drive line
5. Demand line
6. Transfer line

The control lines are used to write control and status information into appropriate drive registers prior to a data transfer operation.
DISKS

and are used to read status or error information from the drive registers.

System Registers
The processor must condition the controller and the drive with specific positioning and format information before any data can be transferred in the system. To do this, addressable registers are used. They are available to the processor and can be accessed by using the proper protocol procedures and the correct address for each register.

The registers in the controller are called local registers and the registers in the drive are called remote registers. The procedures required to read or write local registers are contained in the specific controller manual for each system.

Specific bit locations in these drive registers are designated as follows:
Read Only indicates that the program can read the status of these bits but cannot load them
Write Only indicates that the program can load them but will read back a 0
Read/Write indicates that the program may load them and also read them back.

Twenty-two registers are used by the drive and the controller to communicate control commands, status data, error conditions, and maintenance information. Sixteen registers are located in the drive, and the remaining six are located in the various controllers that are used as a MASSBUS interface.

Table 4-1 contains these 22 registers, their mnemonics, UNIBUS and MASSBUS addresses, whether they are read only or read/write, and their basic function.

Controller Registers—Six of the 22 registers for drive operation are located in the controllers. The RJM02 controller contains the following registers.

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMWC</td>
<td>Word Count</td>
</tr>
<tr>
<td>RMBA</td>
<td>Bus Address</td>
</tr>
<tr>
<td>RMCS2</td>
<td>Control and Status 2</td>
</tr>
<tr>
<td>RMDB</td>
<td>Data Buffer</td>
</tr>
</tbody>
</table>
### Table 4-1 Controller and Drive Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>UNIBUS Address</th>
<th>MASSBUS Address</th>
<th>Mode</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMCS1 Control</td>
<td>776 700</td>
<td>00*</td>
<td>Read/Write</td>
<td>Contains function code, Go bit.</td>
</tr>
<tr>
<td>RMWC Word Count</td>
<td>776 702</td>
<td>*</td>
<td>Read/Write</td>
<td>Contains 2’s complement of number of words to be transferred.</td>
</tr>
<tr>
<td>RMBA Bus Address</td>
<td>776 704</td>
<td>*</td>
<td>Read/Write</td>
<td>Contains memory address of location where data transfer is to begin.</td>
</tr>
<tr>
<td>RMDA Desired Sector/Track Address</td>
<td>776 706</td>
<td>05</td>
<td>Read/Write</td>
<td>Contains disk sector and track address where transfer is to occur.</td>
</tr>
<tr>
<td>RMCS2 Status</td>
<td>776 710</td>
<td>*</td>
<td>Read/Write</td>
<td>Contains controller status indication.</td>
</tr>
<tr>
<td>RMDS Drive Status</td>
<td>776 712</td>
<td>01</td>
<td>Read/Write</td>
<td>Contains all non-error status plus error summary bit.</td>
</tr>
<tr>
<td>Register Name</td>
<td>UNIBUS Address</td>
<td>MASSBUS Address</td>
<td>Mode</td>
<td>Function</td>
</tr>
<tr>
<td>-------------------------------------</td>
<td>----------------</td>
<td>-----------------</td>
<td>-----------</td>
<td>--------------------------------------------------------------------------</td>
</tr>
<tr>
<td>RMER1 Error No. 1</td>
<td>776 714</td>
<td>02</td>
<td>Read/Write</td>
<td>Contains individual error indication.</td>
</tr>
<tr>
<td>RMAS Attention Summary</td>
<td>776 716</td>
<td>04</td>
<td>Read/Write</td>
<td>Contains 1-bit per-drive attention summary status.</td>
</tr>
<tr>
<td>RMLA Look-Ahead</td>
<td>776 720</td>
<td>07</td>
<td>Read Only</td>
<td>Contains current sector address under heads.</td>
</tr>
<tr>
<td>RMDB Data Buffer</td>
<td>776 722</td>
<td>*</td>
<td>Read Only</td>
<td>Contains input and output connection to silo for maintenance.</td>
</tr>
<tr>
<td>RMMR1 Maintenance No. 1</td>
<td>776 724</td>
<td>03</td>
<td>Read/Write</td>
<td>Contains diagnostic test functions.</td>
</tr>
<tr>
<td>RMDT Drive Type</td>
<td>776 726</td>
<td>06</td>
<td>Read Only</td>
<td>Contains drive character indication.</td>
</tr>
<tr>
<td>RMSN Serial Number</td>
<td>776 730</td>
<td>10</td>
<td>Read Only</td>
<td>Contains lowest four digits of drive serial number.</td>
</tr>
</tbody>
</table>
**Table 4-1 Controller and Drive Registers (Cont.)**

<table>
<thead>
<tr>
<th>Register Name</th>
<th>UNIBUS Address</th>
<th>MASSBUS Address</th>
<th>Mode</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMOF Offset</td>
<td>776 732</td>
<td>11</td>
<td>Read/Write</td>
<td>Contains bit for control of offset of drive heads.</td>
</tr>
<tr>
<td>RMDC Desired Cylinder</td>
<td>776 734</td>
<td>12</td>
<td>Read/Write</td>
<td>Contains address of cylinder for seek operation.</td>
</tr>
<tr>
<td>RMHR Holding</td>
<td>776 736</td>
<td>13</td>
<td>Read/Write</td>
<td>Not used; contents always all zeros.</td>
</tr>
<tr>
<td>RMMR2 Mainten- nance No. 2</td>
<td>776 740</td>
<td>14</td>
<td>Read Only</td>
<td>Contains diagnostic test functions.</td>
</tr>
<tr>
<td>RMER2 Error No. 2</td>
<td>776 742</td>
<td>15</td>
<td>Read/Write</td>
<td>Contains drive error bits.</td>
</tr>
<tr>
<td>RMEC1 ECC Position</td>
<td>776 744</td>
<td>16</td>
<td>Read Only</td>
<td>Contains position of error burst.</td>
</tr>
<tr>
<td>RMEC2 ECC Pattern</td>
<td>776 746</td>
<td>17</td>
<td>Read Only</td>
<td>Contains the error burst.</td>
</tr>
<tr>
<td>RMBAE Bus Address</td>
<td>776 750</td>
<td>*</td>
<td>Read/Write</td>
<td>Contains the bus address extension bits.</td>
</tr>
<tr>
<td>RMCS Control and Status</td>
<td>776 752</td>
<td>*</td>
<td>Read/Write</td>
<td>Contains status and error indications.</td>
</tr>
</tbody>
</table>

* Controller registers (RMCS1 is shared by drive and controller).
The RH20 and RH70 controllers contain all of these registers plus the RMBAE (bus address extension) and RMCS3 (control and status 3) registers.

**Control Register (RMCS1)**—This read/write register is shared by both the RH controller and the drive. The bits assigned to the RH controller contain the operational status of overall system.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-5</td>
<td>Not used by RH controller</td>
<td>Used by drive</td>
</tr>
<tr>
<td>6</td>
<td>IE (Interrupt Enable)</td>
<td>A program-controlled interrupt may occur by writing into IE and RDY at the same time.</td>
</tr>
<tr>
<td></td>
<td>Read/write</td>
<td></td>
</tr>
<tr>
<td>07</td>
<td>RDY (Ready)</td>
<td>This bit is normally set except during data transfers when it is reset.</td>
</tr>
<tr>
<td></td>
<td>Read only</td>
<td></td>
</tr>
<tr>
<td>8, 9, A16, A17</td>
<td>UNIBUS Address Extension Bits</td>
<td>Upper extension bits of the RMBA register. Cleared by INIT, controller clear, or by writing 0s in these bit positions.</td>
</tr>
</tbody>
</table>

![Diagram of RMCS1 register](image-url)
<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>PSEL (Port Select)</td>
<td>A UNIBUS select control bit, this bit cannot be modified while the RH controller is performing a data transfer (RDY negated).</td>
</tr>
<tr>
<td>11</td>
<td>Not used by RH controller</td>
<td>Used by drive.</td>
</tr>
<tr>
<td>12</td>
<td>Not used by either controller or drive</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>MCPE (MASSBUS Control Bus Parity Error)</td>
<td>Parity errors that occur on the control bus while writing a drive register are detected by the drive and cause the PAR error (RMER1 register, bit 03) to set.</td>
</tr>
<tr>
<td>14</td>
<td>TRE (Transfer Error)</td>
<td>Set if any of the following conditions occur.</td>
</tr>
<tr>
<td></td>
<td>Read/Write</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1. Data late (RMCS2 bit 15 is set).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Write check error (RMCS2 bit 14 is set).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. UNIBUS parity error (RMCS2 bit 13 is set).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4. Nonexistent drive (RMCS2 bit 12 is set).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5. Nonexistent memory (RMCS2 bit 11 is set).</td>
</tr>
</tbody>
</table>
Bit | Name | Function
--- | --- | ---
15 | SC (Special Condition) | Read only

6. Program error (RMCS2 bit 10 is set).
7. Missed transfer bus parity error (RMCS2 bit 9 is set).
8. MASSBUS data bit 9 is set.
9. Drive error occurs during a data transfer.

Cleared by UNIBUS A INIT, controller clear, or by loading a data transfer command with GO bit set.

Set by TRE or ATTN or MASSBUS control parity error. Cleared by UNIBUS A INIT, controller clear, or by removing the ATTN condition.

Word Count Register (RMWC)—The word count register is located in the controller. This register is loaded by the program with the 2's complement of the number of words to be transferred. During a data transfer, it is incremented by 1 each time a word is transmitted to or from memory. A maximum of 65,535 words can be transferred at one time.

**Word Count Register (RMWC)**

00-15 WC (Word Count) Read/write

Incremented for each data transfer. Set by the program to specify the number of words to be transferred (2's complement form). This register is cleared only by writing 0's into it.

Address Register (R MBA)—This device register is used by the controller to address the memory location in which a transfer is to take place.
The RMBA register forms the lower 16 bits of address which combine with bit 09 and 08 of the control register RMCS1 to read the 18 bit memory address. This register is loaded by the program with the starting memory address. Each time a DMA transfer is made, the register is incremented by 2. If the BAI (bus address increment inhibit) bit (bit 03 of RMCS2) is set, the incrementing of the register is inhibited and all transfers take place to or from the starting memory address.

**Address Register (RMBA) Bit Assignments**

**Bit:** 0  **Name:** Not used

**Function:**

**Bit:** 1-15  **Name:** BA (Bus Address) Read/write

**Function:** The BA register is incremented by 2 by the controller after each transfer of a word to or from memory.

**Status Register (RMCS2)—**This read/write register indicates the status of the controller and contains the drive unit number. The unit number specified in bits 0 to 2 of this register indicates which of the possible eight drives is selected.

**Bit:** 0-2  **Name:** U (Unit Select) Read/Write

**Function:** The unit select bits can be changed by the program during data transfer operations without interfering with the transfer. The drive registers contain bits that come from the selected drive.

**Bit:** 3  **Name:** BAI (Unibus Address Increment Inhibit) Read/Write

**Function:** When set during a data transfer, all data words are read from or written into the same memory location.
Bit: 4  Name: PAT (Parity Test) Read/Write
Function: While PAT is set, the controller checks for even parity received on the data bus but not on the control bus.

Bit: 5  Name: CLR (Controller Clear) Write only
Function: UNIBUS A INIT also causes Controller Clear to occur.

Bit: 6  Name: IR (Input Ready) Read only
Function: Serves as a status indicator for diagnostic check of the silo buffer. An attempt to write the RMDB register before IR is asserted will cause a data late error (bit 15 of this register sets). Read only.

Bit: 7  Name: OR (Output Ready) Read only
Function: Serves as a status indicator for diagnostic check of the silo buffer. An attempt to read the RMDB register before OR is asserted will cause a data late error (bit 15 of this register sets).

Bit: 8  Name: MDPE (MASSBUS Data Bus Parity Error) Read only
Function: MDPE causes a transfer error (bit 14 of RMCS1 sets). Parity errors on the MASSBUS data bus during write operations are detected by the drive and cause the PAR error (RMER1 register, bit 3).

Bit: 9  Name: MXF (Missed Transfer) Read/write
Function: MXF causes a transfer error (bit 14 of RMCS1 sets). This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive that has ERR (bit 14 of RMDS set) or if the drive fails to initiate the command for any reason (such as a parity error).

Bit: 10 Name: PGE (Program Error)
Function: PGE causes a transfer error (bit 14 of RMCS1 sets). The data transfer command code is inhibited from being written.

Bit: 11 Name: NEM (Nonexistent Memory) Read only
Function: NEM causes a transfer error (bit 14 contains the address +2 of the memory location causing the error).

Bit: 12 Name: NED (Nonexistent Drive) Read only
Function: NED causes a transfer error (bit 14 of RMCS1 sets).

Bit: 13 Name: UPE (Unibus Parity Error) Read/Write
Function: UPE causes a transfer error (bit 14 of RMCS1 sets).
RM02/RM03

When the UNIBUS is selected to do 18 bit data transfers, the UPE error is disabled. When a UNIBUS parity error occurs, the RMBA register contains the address +2 of the memory word with the parity error [if BAI (bit 3 of this register) is not set]. This bit may be set by program control for diagnostic purposes.

**Bit: 14**  
**Name:** WCE (Write Check Error) Read only  
**Function:** WCE causes a transfer error (bit 14 of RMCS1 sets). If a mismatch is detected during a write check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RMBA (and extension) is the address of the word following the one that did not match (if BAI is not set). The mismatched data word from the disk is displayed in the data buffer (RMDB).

**Bit: 15**  
**Name:** DLT (Data Late) Read only  
**Function:** DLT causes a transfer error (bit 14 of RMCS1 sets). Buffering is 66 words deep in the controller. Can also be set by the program reading or writing the RMDB register.

**Data Buffer Register (RMDB)—**This read/write register is used to monitor the silo data buffer in the controller. If the program attempts to write into the data buffer while it is full or read the data buffer when it is empty, a data late (DLT) error occurs (bit 15 of RMCS2 is set). The RMCS2 register also provides status indicators showing whether the data buffer can be read or written. When RMCS2 bit 6 (IR) is set, the data buffer can be written. When RMCS2 bit 7 (OR) is set, the data buffer can be read.

The RMDB register can be read and written only as an entire word. Any attempt to write a byte will cause an entire word to be written. Reading the RMDB register is a "destructive" readout operation: The top data word in the silo buffer is removed by the action of reading the RMDB and a new data word (if present) replaces it a short time later. The action of writing the RMDB register causes one more data word to be inserted into the silo buffer (if it was not full).

**Bit: 0-15**  
**Name:** DB (Data Buffer)  
**Function:** Used by the program for diagnostic purposes. When the register is written into, IR is cleared until the data buffer is ready to accept a new word. When the register is read, it will cause OR to be cleared until a new word
is ready. During a write-check error condition, the data word read from the disk that did not compare with the corresponding word in memory is frozen in RMDB for examination by the program.

**Bus Address Extension Register (RMBAE)**—The RMBAE register contains the upper 6 bits of the memory address which combine with the lower 16 bits located in RMB register to form the complete 22 bit address. This register is loaded by the program in conjunction with the RMB register to specify the starting memory address of a data transfer operation. The 6-bit field is incremented (decremented for specific function codes) each time a carry (borrow) occurs from the RMBA register during memory transfers.

**Control and Status Register No. 3 (RMCS3)**—The RMCS3 register contains parity error information associated with the memory bus. Bit position 13 of the RMCS3 (DPE) indicates that a parity error occurred during the memory transfer. Bit positions 13 through 15 of RMCS3 further localize the error for diagnostic maintenance. In addition, bits 0 through 3 provide the diagnostic program the ability to invert the sense of parity check and thereby verify correct operation of the parity circuits.

An interrupt enable bit (IE) in the RMCS3 register allows the program to enable interrupts without writing into a drive register as previously described. This bit also appears in the RMCS1 register for program compatibility and can be set or cleared by writing into either register.

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOT USED</td>
<td>NOT USED</td>
<td>INVERTED PARITY CHECK</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Bit: 0-3
- **Name:** IPCK (Inverted Parity Check)
- **Function:** Parity control is provided for each byte in double word addresses, i.e.,
  - IPCK 0—Even word, even byte
  - IPCK 1—Even word, odd byte
IPCK 2—Odd word, even byte
IPCK 3—Odd word, odd byte
Read/write.

Bit: 4-5  Name: Not used
Function:

Bit: 6   Name: IE (Interrupt Enable)
Function: This bit can be set or cleared by writing into RMCS1 register. If written through RMCS3 register, write operation is not performed into a drive register simultaneously. Read/write.

Bit: 7-9 Name: Not used
Function:

Bit: 10  Name: (Double Word)
Function: Set if the last memory transfer was a double-word operation. Cleared by UNIBUS INIT, controller clear, or by loading a data transfer command with GO bit set. Read only.

Bit: 11  Name: WCE LO (Write Check Error-Even Word)
Function: Set when data fails to compare between memory and the drive. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO set.

When set, causes bit 14 (WCE) RMCS2 to set. Read only.

Bit: 12  Name: WCE HI (Write Check Error-Odd Word)
Function: Set when data fails to compare between memory and the drive. Cleared by UNIBUS INIT, controller clear, error clear, or by loading a data transfer command with GO set.

When set, causes bit 14 (WCE) of RMCS2 to set.

Bit: 13  Name: DPE LO (Data Parity Error-Even Word)
Function: Set if a parity error is detected on data from memory when the RH controller is performing a write or write check command. Cleared by UNIBUS INIT, controller clear, error clear, or by loading a data transfer command with GO bit set.

When set, causes bit 13 (UPE) of RMCS2 to set.

Bit: 14  Name: DOP HI (Data Parity Error-Odd Word) Read only
Function: When set, causes bit 13 (UPE) of RMCS2 to set.
Bit: 15  Name: APE (Address Parity Error) Read only
Function: When set, causes bit 13 (UPE) of RMCS2 to set.

MASSBUS Adaptor Registers

Control Register (RMCS1)—This register is utilized by both the drive and the controller to store the disk commands and operational status. The function (command) code designates a function for the drive selected in bits 0 through 2 of the RMCS2 register. Setting the GO bit causes the drive to recognize the function code in the control register. The actual execution of the command, however, does not begin until the Run line is asserted by a data transfer command.

Control Register (RMCS1) Bit Assignment Used by Drive

Bit: 0-5  Name: GO bit and F0-F4
Function: Execution of data command begins when MASSBUS Run line is asserted.

Bit: 6-10  Name: Not used by drive
Function: Used by controller.

Bit: 11  Name: DVA (Drive Available)
Function: This bit is used in dual-controller configurations. Read only.

Bit: 12-15  Name: Not used by drive
Function: Used by controller.

Drive Status Register (RMDS)—This read-only register contains the various status indicators for the selected drive. The status indicators displayed are those of the drive that is specified by the unit select bits (00:02) of the RMCS2 register. The register is a read-only register. Writing into this register will not cause an error, and will not modify any of the status bits.

Drive Status Register (RMDS)
Bit: 0  Name: OM (Offset Mode)
Function: When set and a read command is received, the offset is performed prior to the execution of the read. Read only.

Bit: 1-5  Name: SP (Spare) Read Only
Function: Spare bits for future expansions.

Bit: 6  Name: VV (Volume Valid)
Function: When reset, this bit indicates when the drive has been put off-line and on-line and a disk pack may have been changed. Therefore, the program should not assume anything about the identity of the pack. Read only.

Bit: 7  Name: DRY (Drive Ready)
Function: If this bit is reset, the controller cannot issue another command. When set, this bit indicates the readiness of the RM03 to accept a new command. Read only.

Bit: 8  Name: DPR (Drive Present)
Function: Always set for single-controller operation. In dual controller operation, this bit is set for the controller that has seized the drive and is reset for the other controller. Read only.

Bit: 9  Name: PGM (Programmable)
Function: In single-controller system configuration, this bit will always be reset. Dual-controller operation permits access from two controllers. Read only.

Bit: 10  Name: LBT (Last Block Transferred)
Function: Set by the drive on rising edge of EBL pulse when last addressable sector on the disk pack has been read or written. Cleared when a new track or sector address is received, also cleared during power-up cycles.

Bit: 11  Name: WRL (Write Lock)
Function: The drive is placed in write protect mode through a manual switch on the drive control panel. The status of the device is indicated by illumination of the light over the switch. When the indicator is on, any attempt by the operating system to issue a write command on a write-locked device will cause the write lock error. Read only.

Bit: 12  Name: MOL (Medium On-Line)
Function: After power-up cycle, heads are positioned over cylinder no. 0 and MOL bit is set. Whenever the MOL bit
changes state (set or reset), bit 15 (ATA) of this register is also set, except when the heads are unloaded. Read only.

Bit: 13  Name: PIP (Positioning in Progress)
Function: This bit helps to distinguish the case of a drive being in busy (DRY negated) while no data transfer is underway (RDY asserted in the controller). Read only.

Bit: 14  Name: ERR (Error)
Function: A composite error bit that is the logical OR of all drive error conditions. While ERR is set, only clearing commands are accepted by the drive in a programmable mode. Read only.

Bit: 15  Name: ATA (Attention Active)
Function: For dual-controller operation, the ATA bit is asserted on both ports each time the drive cycles up.

There are two ATA bits: ATA-A, which is accessible to controller A, and ATA-B, which is accessible to controller B. When the PORT switch is in controller A, the ATA-A bit is displayed in the ATA bit position (bit 15) of the register. Accesses from controller B will read all 0's except for the RMAS register. The reverse situation holds true when controller B is selected.

Error Register No. 1 (RMER1)—This register contains the error status indicators for the drive whose unit number appears in bits 0 through 2 of RMCS2. The logical OR of all the error bits in the RMER1 and RMER2 registers will be written into bit 14 of RMDS.

The RMER1 register is a read/write register and can be written as a word.

Errors can be classified into two categories: class A and class B.
• A class A error is handled at the completion of a non-data transfers command or, in the case of a data transfer command, at a sector boundary provided the Run line is inactive.
• A class B causes the command to terminate immediately or as soon as possible.

Error Register No. 1 (RMER1) Bit Assignments

Bit: 0  Name: ILF (Illegal Function)
Function: ILF is a class B error.
Bit: 1  Name: ILR (Illegal Register)
Function: When a read is attempted on an illegal register, the complement of the contents of the holding register is placed on the bus lines. ILR is a class A error.

Bit: 2  Name: RMR (Register Modification Refused)
Function: Set when a write is attempted into any register (except RMAS or RMMR1) while the GO bit is set. Cleared by drive clear, INIT, power-up cycle, or by writing 0's into this register.

The following registers can be written into before or after an operation.
- Control register
- Error registers
- Maintenance register no. 1
- Attention summary register
- Desired sector/track
- Address register
- Offset register
- Desired cylinder address register

The remaining drive registers are read-only registers.

Bit: 3  Name: PAR (Parity Error)
Function: Depending when PAR occurs, it is either a class A or B error.
- Class A during a register write
- Class B if DPE is set

Bit: 4  Name: FER (Format Error)
Function: Error usually indicates that pack and drive are incompatible in data word length (e.g., drive configured for 16 bit format and an 18 bit format pack installed).

Bit: 5 Name: WCF (Write Clock Fail)
Function: WCF is a class B error. Read/write.
Bit: 6 Name: ECH (ECC Hard Error)
Function: ECH is a class B error.
Bit: 7 Name: HCE (Header Compare Error)
Function: HCE is a class A error during a read header and data command and a class B error during all other commands.

Bit: 8 Name: HCRC (Header CRC Error)
Function: It is possible for the cylinder address and error sector/track address words of the header (first two words) to compare successfully but, because of an error in the first two header words of the CRC word, the HCE bit will be reset and the HCRC bit will be set.

Bit: 9 Name: AOE (Address Overflow Error)
Function: AOE is a class B error.

Bit: 10 Name: IAE (Invalid Address Error)
Function: IAE is a class B error which causes the command to terminate when the GO bit sets.

Bit: 11 Name: WLE (Write Lock Error)
Function: WLE is a class B error. The status of the WRITE LOCK switch is allowed to change only on a sector boundary during a write command.

Bit: 12 Name: DTE (Drive Timing Error)
Function: A failure in either the drive or the sequencing circuits of the RM03 no longer guarantees that the written or read data is in the proper sequence.

DTE is a class B error.

Bit: 13 Name: OPI (Operation Incomplete)
Function: OPI is a class B error.

Bit: 14 Name: UNS (Drive)
Function: Set when a condition exists that prevents proper operation (such as low ac power). Also set when bit 7 (DVC) of RMER2 is set.

Bit: 15 Name: DCK (Data Check Error)
Function: DCK is a class A error if bit 10 (HCI) of RMOF is set and a class B error if HCI is reset.

Maintenance Register No. 1—The RMMR1 register provides maintenance and diagnostic information useful during maintenance operations. This register has two distinct 16 bit sections: a read-only section and a write-only section. The read-only section permits monitoring of drive logic signals during the maintenance operations. The write-only section of this register provides a method to control the logic functions of the drive.

The write-only section can be written only after the drive is configured in the maintenance mode of operation (bit 00 set). The read-only section can be read in both normal and maintenance operational modes.

Maintenance Register No. 1 (RMMR1) Bit Assignments for Read-Only Bits

```
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Occupied
Run and Go
End of Block
Exception
Enable Search
Looking for Sync
Enable CRC Out
Data Area
Header Area
Continue
From Strobe
Enable ECC Out
Write Data
Last Sector
Last Sector Track
Diagnostic Mode
```

Bit: 0  Name: DMD (Diagnostic Mode)
Function: Set when the write-only section of this bit location is set by a diagnostic program. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.

Bit: 1  Name: LST (SECT TRK and Track)
Function: When set, used to enable the cylinder address counter and to cause a mid-transfer seek. Set at sector 31, track 4 for 16 bit format, or set at sector 29.

Bit: 2  Name: LS LST SECT (Last Sector)
Function: When set, used to enable the track address counter and to cause a new head to be selected during spiral data operations (either reading or writing).
Bit: 3  Name: WE WRITE DATA (Write Data)
Function: This bit represents the serial data being set to the drive during a write operation. Depending on the time this bit is read, it can be considered the output of the data register, ECC generator, or CRC generator. Cleared by drive clear, INIT, or power-up.

Bit: 4  Name: EECC EN ECC OUT (Enable ECC OUT)
Function: This bit is only set during write operations when the ECC pattern is being written.

Bit: 5  Name: WC PROM STROBE (PROM Strobe)
Function: One complete PROM cycle lasts 16 bit clocks when in 16 bit format or 18 bit clocks when in 18 bit format. These PROM strobes are used to generate the read or write data timing.

Bit: 6  Name: CONT CONTINUE (Continue)
Function: As long as Continue is set, the drive continues to perform data transfer.

Bit: 7  Name: PHA P HEADER AREA (Header Area)
Function: The header sync byte precedes the three header words.

Bit: 8  Name: PDA P DATA AREA (Data Area)
Function: The data sync byte precedes the 256 data words.

Bit: 9  Name: ECRC EN CRC OUT (Enable CRC Out)
Function: Set by the data sequencer during the time the CRC pattern is being written in a write operation. Cleared by drive clear, INIT, or power-up.

Bit: 10 Name: P LFS (Looking for Sync)
Function: Until Sync is located, the word clock to the data sequencer is inhibited.

Bit: 11 Name: ESRC ENABLE SEARCH (Enable Search)
Function: Setting the enable search enables the sector compare circuits which, in turn, activate the data sequencer once the correct rotational position is achieved.

Bit: 12 Name: REX REC EXC (Exception)
Function: This bit reflects the status of the MASSBUS Exception line. Cleared by drive clear, INIT, or power-up.

Bit: 13 Name: EBL RM03 EBL (End of Block)
Function: Set by the adapter to indicate that the last block of data on the disk has been transferred. Cleared by drive clear, INIT, or power-up.
Bit: 14  Name: R/G RUN AND GO (Run and Go)
Function: Set when the MASSBUS Run line is active and the GO bit is set. Cleared when the GO bit is reset.

Bit: 15  Name: OCC OCCUPIED (Occupied)
Function: Set by the adapter during a valid data transfer operation. Cleared on the trailing edge of the GO bit.

**Maintenance Register No. 1 (RMMR1) Bit Assignments for Write-Only Bits**

Bit: 0  Name: DMD (Diagnostic Mode)
Function: The maintenance register is enabled by setting the DMD bit. This bit completely isolates the drive mechanism and analog circuitry from the disk control logic. The DMD bit must remain set as long the maintenance register is functioning. All read/write commands will function in the normal fashion except for the fact that the data will wrap around itself instead of actually being written on the disk.

Bit: 1  Name: MSC MR SECT COMP (Sector Compare)
Function: During normal search operations, the 5 bit sector count from the drive is compared with the address in the RMDA register. The sector compare bit allows diagnostic software the capability of forcing a sector compare, thus allowing a successful search and further testing of the data path.

Bit: 2  Name: MI MR INDEX (Index Pulse)
Function: Used to check out the change of format logic.
Bit: 3  **Name:** MWP MR WRT PROT  
**Function:** Without having to operate the switch, this allows the diagnostic program to verify the write protect functions.

Bit: 4  **Name:** Not used.

Bit: 5  **Name:** MS MR SECT PULSE  
**Function:** Used to clock logic elements in the sector compare circuits.

Bit: 6  **Name:** MDF MR DRIVE FAULT (Drive Fault)  
**Function:** Used to test error-handling logic in the adapter.

Bit: 7  **Name:** MSER MR SEEK ERR (Seek Error)  
**Function:** A seek error cannot be forced by specifying a cylinder address greater than 822 since the adapter would detect this as an invalid address and inhibit the execution of the seek.

Bit: 8  **Name:** MDC MR ON CYL (On Cylinder)  
**Function:** Set by a diagnostic program to simulate the On Cylinder signal sent from the drive when the servo has positioned the heads over a data track. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.

Bit: 9  **Name:** MUR MR UNIT READY (Unit Ready)  
**Function:** The Unit Ready signal indicates that the pack is up to speed, heads are loaded, and no drive fault exists.

Bit: 10  **Name:** MRD MR READ DATA (Read Data)  
**Function:** By using the read data bit, diagnostic software can wrap around data at the adapter level and verify the data path independent of the drive.

Bit: 11  **Name:** MCLK MAINT CLK (Maintenance Clock)  
**Function:** This clock has two distinct functions depending on whether a read or write operation is being performed. With read gate on, simulates the Read Clock signal from the drive; with write gate on, simulates the Servo Clock signal from the drive.

Bit: 12  **Name:** MSEN SRCH TO DIS (Search Timeout Disable)  
**Function:** Normally the search timeout circuits generate an OPI signal if the drive was unable to locate the desired sector within two revolutions.

Bit: 13  **Name:** DEBL (Diagnostic EBL)
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**Function:** This bit also allows diagnostic programs to step through the command sequencer without going through a complete data transfer (independently of the read/write timing sequencer).

**Bit: 14** **Name:** DBEN DEBUG EN (Debug Clock Enable)

**Function:** When the debug clock enable bit is reset, the command sequencer clock is derived from the system clock, causing the command sequencer to run at its normal rate.

**Bit: 15** **Name:** DBCK DEBUG CLK (Debug Clock)

**Function:** Set by the diagnostic program as the source for the command sequencer clock. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.

**Attention Summary Pseudo-Register (RMAS)—**The attention summary register is not like the other addressable register in the drive. While it is considered as being a 16 bit register, it is actually composed of up to eight flip-flops. Each bit is physically located in one of the eight possible drives that can be connected to a single controller. Each flip-flop is connected to the control bus line whose line number corresponds to the number assigned to the drive. The eight flip-flops are actually in parallel and it is this configuration that is called a pseudoregister.

The attention summary register allows the program to examine the attention status of all the drives with only one register read operation. It also provides the means for resetting the attention logic in a selected group of drives. The bit displayed in each of the eight low-order positions of this register is identical to the ATA bit displayed in RMDS for the corresponding drive. When fewer than eight drives are attached to the controller, the bits corresponding to the missing drives are always 0.

**Bit: 0-7** **Name:** ATA (00:07) (Attention Active) Read/write

**Function:** Any drive’s ATA bit set is displayed in bit 15 of RMDS. Each drive responds in the bit position that corresponds to its unit select plug number; e.g., drive 2 sets bit position 2 in RMAS.

**Bit: 8-15** **Name:** Not used.

**Function:**

**Sector/Track Address Register (RMDA)—**This device register is used to address the sector and track on the disk to or from which a transfer is desired. The RMDA register is associated with the
drive whose unit number appears in bits 00:02 of the status register RMCS2. Before a transfer, the RMDA is loaded by the program with the address of the first block to be transferred. The RMDA is incremented each time a block of data has been transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred.

The RMDA register contains a 5 bit sector address providing for 30 sectors per data track (18 bit format) or for 32 sectors per data track (16 bit format). The register also contains a 3 bit track address providing for five data tracks. The sector and track addresses are noncontiguous; however, when the sector count fills up with a count of 29 or 31 (depending on format), the next word read or written will cause the track address to increment and the sector address to clear. When the sector address and track address reach their full counts, the next word will cause both sector and track addresses to increment to 0 and a mid-transfer seek to occur.

The RMDA register can only be loaded with a 16 bit word. Any attempt to write a byte causes the entire word to be written. Any attempt to write in this register while the drive’s GO bit is asserted will cause an RMR (register modify refused) error (RMER1, bit 02) and the register is not modified.

**Desired Sector Track Address Register RMDA**

**Bit:** 0-4

**Function:**

**Bit:** 5-7

**Function:**

**Bit:** 8-12 **Name:** TA (1,2,4,8,16) (Track Address)

**Function:** Incremented by the drive when sector 31 (16 bit format) or sector 29 (18 bit format) is reached. Read/write.

**Bit:** 13-15 **Name:** SP (Spare)

**Function:** Spare bits for future expansion. Read/write.

**Drive-Type Register (RMDT)—**This read-only register allows the program to distinguish between different classes of drives. The register is located in the drive whose unit number appears in bits 00 through 02 of RMCS2.

**Drive-Type Register (RMDT) Bit Assignments**

**Bit:** 0-8 **Name:** DT (Drive Tape)
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Function: This 9-bit field contains a unique number assigned to each drive on the bus. The device type number for the drive is installed on the back panel. (20024 for single port or 24024 for dual port). Read Only

Bit:  9-10  Name:  Not used

Function:

Bit:  11   Name:  DRQ (Drive Request Required)
Function: The status of this bit indicates the availability of the dual-port option as follows:
1 = Dual Port
0 = Single Port
Read Only

Bit:  12   Name:  Not Used

Function:

Bit:  13   Name:  (Moving Head)
Function: Since the RM03 is a moving head device, this bit is hardwired to the 1 state. Read Only

Bit:  14-15 Name:  Not Used

Function:

Look-Ahead Register (RMLA)—This read-only register contains the count of the sector that is currently positioned under the heads. This value is represented as a binary number in bit locations 6-10, where bit 6 is the least significant bit. The maximum count for a 16 bit/word format is 31 and for an 18 bit/word format is 29.

The count value is reset to 0 by the index pulse at the beginning of the first sector and is incremented by one at each sector pulse. The count value is not valid for 200 \( \mu \text{sec} \) after either an index or sector pulse.

Look-Ahead Register (RMLA)

Bit:  0-5  Name:  Not Used

Function: Always read as 0's.

Bit:  6-10 Name:  SC(1,2,4,8,16) (Sector Count)
Read Only

Function: Set to correspond with the sector count value. Reset by the index pulse.

Bit:  11-15 Name:  Not Used.

Function: Always read as 0's.
Serial Number Register (RMSN)—This read-only register permits the program to identify drives attached to the same controller. The serial number provides a means of distinguishing between different drives with identical characteristics that are connected to the same controller. This information is useful during error logging of on-line software diagnostics to allow errors to be associated with a particular drive. The serial number register differs from the drive-type register in that the drive type refers to different classes of drives such as single- or dual-port operation.

Offset Register (RMOF)—The drive has the ability to offset the positioner approximately 200 \( \mu \text{in} \) from the track centerline in either direction.

The positioner offsetting information is supplied to the drive directly from the software operating system prior to the issuance of the offset command.

Desired Cylinder Register (RMDC)—This read/write register contains the address of the cylinder to which the drive positioner moves the heads for a seek, search, or data-handling command. Since the maximum number of cylinders in the RM02 or RM03 is 823, only 10 bits are necessary to specify the desired cylinder address.

Holding Register (RMHR)—This is an addressable register with no drive function. It is used only by diagnostic software.

Maintenance Register No. 2 (RMMR2)—The RMMR2 register operates in conjunction with the Maintenance Register No. 1 to configure the RM03 MASSBUS adapter in the maintenance mode.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Read Only</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-9</td>
<td>BB (Bus In Lines)</td>
<td></td>
<td>These 10 bus lines represent the lines going to the drive which establish the cylinder address, head address, or control depending on which tag is issued.</td>
</tr>
</tbody>
</table>
Bit: 10  Name: CNT/HD (Control or Head Select)
Function: Set when the tag to the drive is either a control select or head select tag. Cleared by drive clear, INIT, or power-up. Read Only

Bit: 11  Name: CNT/CYL (Control or Cylinder Select)
Function: Set when the tag to the drive is either a control select or cylinder address tag. Cleared by drive clear, INIT, or power-up. Read Only

Bit: 12  Name: TEST BIT (Test Bit)
Function: Set when the command sequencer in the adapter is branching. Used by diagnostics during a branch test sequence. It tells the control sequencer whether to branch or increment. Read Only

Bit: 13  Name: TAG (Tag)
Function: Indicates the status of the Control Select Tag line. Read Only

Bit: 14  Name: REQB (Request B)
Function: When set, indicates that a request for service has been received from port B. Cleared by drive clear, or by a release command in addition to RESET. Read Only

Bit: 15  Name: REQA
Function: When set, indicates that a request for service has been received from port A. Cleared by drive clear or by a release command in addition to RESET.

Error Register No. 2 (RMER2)—The read/write register contains detailed error status information and is primarily used for monitoring the electromechanical performance of the drive rather than the interface. Whenever any of the bits in this register are set, the ERR bit (bit 14) in the status register (RMDS) is set and the ATA bit in the RMAS register is set. All Error Register No. 2 errors are considered catastrophic errors.

All unsafe errors, with the exception of read/write unsafes, cause the drive to retrack the heads from the pack area; prevent a head load from occurring; deselect all heads; and disable the read, write, recalibrate, seek, and offset commands.

All error bits are reset when a drive clear command or an INIT pulse is received. If the heads are retracted from the disk pack upon receiving a drive clear or an initialize pulse, the drive attempts to reload the heads unless the error persists.
Errors are classified into two categories: class A and class B.

- A class A error is handled at the completion of a nondata transfer command, or in the case of a data transfer command, at a sector boundary provided the Run line is inactive.
- A class B error is handled immediately and causes termination of a command or a termination as soon as possible.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-2</td>
<td>Not used</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>DPE (Data Parity Error)</td>
<td>When DPE sets, it also causes bit 3 of RMER1 to set. DPE is a class B error.</td>
</tr>
<tr>
<td>4-6</td>
<td>Not Used</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>DVC (Device Check)</td>
<td>DVC is a class B error.</td>
</tr>
<tr>
<td>8-9</td>
<td>Not Used</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>LBC (Loss of Bit Check)</td>
<td>The bit clock is derived from the read clock and the servo clock. LBC is a class B error.</td>
</tr>
<tr>
<td>11</td>
<td>LSC (Loss of System Clock)</td>
<td>LSC is a class B error.</td>
</tr>
<tr>
<td>12</td>
<td>IVC (Invalid Command)</td>
<td>IVC is a class B error.</td>
</tr>
<tr>
<td>13</td>
<td>OPE (Operator Plug Error)</td>
<td>While the plug is removed, the drive is considered to be nonexistent to the program. OPE is a class B error.</td>
</tr>
</tbody>
</table>
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if the plug is removed during a data-handling command and a class A error if it occurs at any other time.

Bit: 14  Name: SKI (Seek Incomplete)
Function: Due to a positioner malfunction it is possible for the seek not to complete. The drive will assume a positioner hardware problem and will:
• Set the SKI bit (RMER2, bit 14)
• Set the ATA bit (RMDS, bit 15)
• Reset the PIP bit (RMDS, bit 13)
• Set the RDY bit (RMCS1, bit 7)
This indicates to the software that the seek operation did not complete and the exact positioner location is unknown.
A SKI condition will cause the drive to determine that the drive is unsafe to operate and will cause the UNS (RMER1, bit 14) bit to set. The software can diagnose the trouble by monitoring the error registers.

Bit: 15  Name: BSE (Bad Sector Error)
Function: A bad sector is indicated when this bit is cleared. This is a class B error which causes termination of a read command after checking the CRC word.
In the case of a read header and data command, this is a class A error.

ECC Position Register (RMEC1)—The drive has Error Correction Code (ECC) capabilities that detect and correct errors by reconstructing a portion of data. In the specified code word length, the ECC code corrects an error that falls within an 11-bit burst.

Any errors outside the specified burst length are detected but not corrected. The ECC hardware, in this case, yields an ECC uncorrectable error (bit 6 of RMER1 sets). The drive logic contains the hardware to find the burst in which the read error is included and to determine the exact location of the burst within the data field.

The ECC pattern register (RMEC2) contains the actual error burst and the ECC position register (RMEC1) contains the address that determines the actual location of the error burst within the data field. The actual correction of the data field is done by the software with the help of the ECC position and ECC pattern registers.

Following the completion of the error correction procedure, the
ECC position register contains the exact location of the error burst within the data field.

**ECC Pattern Register (RMEC2)**—The read-only register is used in conjunction with the ECC position register (RMEC1) and contains the actual error burst available at the completion of the ECC process.

The software uses the contents of the ECC position register to find the actual location of the error burst in the data field. Then the error burst itself determines the bits within the 11 bit field.

**Command Codes**
The programmer initiates operations by selecting a drive and the control register (776 700), loading the register with a function code and setting the GO bit. The function code specifies a specific command. Upon assertion of the GO bit, the RM03 proceeds to execute the command. The commands can be divided into three categories: positioning commands, data transfers and housekeeping operations. These commands and their corresponding octal function codes are listed below.

<table>
<thead>
<tr>
<th>Positioning Commands</th>
<th>Function Codes (Octal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Seek</td>
<td>5</td>
</tr>
<tr>
<td>Recalibrate</td>
<td>7</td>
</tr>
<tr>
<td>Offset</td>
<td>15</td>
</tr>
<tr>
<td>Return to Centerline</td>
<td>17</td>
</tr>
<tr>
<td>Search</td>
<td>31</td>
</tr>
</tbody>
</table>

**Data Transfer Commands**
- Write Check Data: 51
- Write Check Header and Data: 53
- Write Data: 61
- Write Header and Data (Format): 63
- Read Data: 71
- Read Header and Data: 73

**Housekeeping Operations**
- No-Op: 1
- Drive Clear: 11
- Release: 13
- Read-In Preset: 21
- Pack Acknowledge: 23
Positioning Commands
Positioning commands are mechanical movement commands used to position the heads over the disk pack; they take milliseconds to complete. These commands assert the ATTN line after their normal completion. The positioning commands are:

Seek—This command causes the heads to be moved to the cylinder address specified by the desired cylinder register (RMDC). The current cylinder is made equal to the desired cylinder address following the completion of the command.

Recalibrate—This command positions the heads over cylinder 0.

Offset—An offset allows the heads to be moved off the track centerline. It is used in error recovery processing and moves the heads 200 µin either toward the spindle (positive offset) or away from the spindle (negative offset).

Return to Centerline—This command is used to return to the track centerline after an offset operation. A return to centerline always follows a read command in offset mode.

Search—This command combines the seek command with a search for the desired sector address and can be considered a synchronization command between the software and the desired disk address.

Data Transfer Commands
These commands involve the transfer of data to or from the disk and usually require the completion of a positioning command by either a seek or search command or with an implied seek as part of the data command. The data transfer commands are:

Read Header and Data—A read header and data command transfers 2 words of header information and 256 data words per sector from the disk pack to the RH controller.

Read Data—A read data command transfers 256 data field words from the disk pack to the RH controller for each sector specified. If an error is detected in the header, this command will abort immediately following the CRC check and there will be no data transferred.

Write Check Header and Data—A read header and data command transfers the first 2 words of the header and 256 words of data to the RH controller. Errors in the header, however, cause termination of the command after the CRC word of the head is checked in the drive.
Write Check Data—This command is identical to a read data command.

Write Header and Data—A write header and data command, also referred to as a "format" command, writes all gaps, header, and data for specified sector(s). The drive generates the gaps including the sync byte, CRC, and ECC. The RH controller supplies 2 header words and 256 data words for each sector.

Write Data—A write data command transfers 256 words of data for each specified sector from the controller to the drive. This data field is preceded by a sync byte and followed by a 32 bit ECC, both generated by the drive. A header error will cause the command to abort immediately after checking the CRC word.

Housekeeping Commands
Housekeeping commands are used to place the drive logic into known or initial state. ATTN is not raised at the completion of the housekeeping commands unless there is a persistent error condition. The five housekeeping commands are:

No-op—Upon recognizing this code in the control register (RMCS1) and the GO bit, the drive resets the GO bit. This command is considered a filler command.

Drive Clear—A drive clear command clears bits in the following registers in the MASSBUS adapter.

Status (RMDS) Bit 14 (ERR), bit 15 (ATA)
Error No. 1 (RMER1) All bits
Error No. 2 (RMER2) All bits
Attention Summary (RMAS) All bits (on the selected drive)
Maintenance No. 1 (RMAS) All bits
ECC Pattern (RMEC2) All bits

The drive clear command also clears all error indications in the drive (provided the error condition no longer exists). A pulse on the MASSBUS Initialize line performs the same functions as the drive clear command.

Release—The release command releases the drive for use by the other port. It must be preceded by a drive clear command if there is an error condition.

Read-in Preset—The read-in preset command sets the volume valid (VV) bit (06) in the status register (RMDS) for the port that issued the command. This command also clears all bits in the
desired sector/track address register (RMDA) and all bits in the
desired cylinder address register (RMDC). It also clears the offset
mode and the following bits in the offset register (RMOF).

OFD (bit 07)—Offset Direction
HCl (bit 10)—Header Compare Inhibit
ECI (bit 11)—Error Correction Code Inhibit
FMT 16 (bit 12)—Format

Pack Acknowledge—The pack acknowledge command sets the
volume valid (VV) bit (06) in the status register (RMDS) for the
port that issued the command. This command must be issued
before any data transfer or positioning commands can be given
if the pack has gone off-line and then on-line (i.e., if MOL changes
state). It is primarily intended to avoid unknown pack changes on
a dual-controller drive configuration.

Operation of Error Correcting Code (ECC)
The drive contains error correcting code logic that has the capa-
bility to detect errors in the data being read off the disk and pro-
vide information to the software to permit data recovery. The ECC
code employed, called burst error correcting code, locates an
error that falls within a 11-bit burst. Any errors outside this 11-bit
burst length are detected but not correctable. For uncorrectable
errors, the ECC logic generates an ECC hard error (ECH) indica-
tion. An uncorrectable error is defined as any error field larger
than the 11-bit burst. Isolated dropped bits (for example, one bit
in word 0 and one bit in word 225) are uncorrectable by this
definition. If the conditions named occur, the drive indicates the
ECC uncorrectable error to the software by setting the ECC hard
error bit (ECH) in error register No. 1 (RMER1). The drive ECC
logic performs the following functions:

1. Finds the 11-bit burst where the read error is located.
2. Determines the exact location of the burst within the data field.

This error information is provided to the controller through two
registers.

ECC Pattern Register (RMEC2) Contain the actual 11-bit error
burst
ECC Position Register (RMEC1) Contains the address of the
first bit of the error burst
within the data field.

The actual correction of the data field is done by the software
using the data contained in these two registers. In the event of an ECC hard error, the contents of the ECC pattern and ECC position registers are of no significance.

**RM02/03 Specifications**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Limit</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>RM03</strong></td>
<td><strong>RM02</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Seek Time</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum seek (822 cylinders)</td>
<td>55 msec</td>
<td>55 ms</td>
<td></td>
</tr>
<tr>
<td>One cylinder seek (maximum)</td>
<td>6 ms</td>
<td>6 ms</td>
<td></td>
</tr>
<tr>
<td>Average seek</td>
<td>30 ms</td>
<td>30 ms</td>
<td></td>
</tr>
<tr>
<td>Seek to the same cylinder</td>
<td>37.5 ms</td>
<td>37.5 ms</td>
<td></td>
</tr>
<tr>
<td><strong>Latency</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Speed</td>
<td>3600 rev/min</td>
<td>2400 rev/min</td>
<td></td>
</tr>
<tr>
<td>Maximum latency</td>
<td>17.3 ms</td>
<td>25.9 ms</td>
<td></td>
</tr>
<tr>
<td>Average latency</td>
<td>8.33 ms</td>
<td>12.5 ms</td>
<td></td>
</tr>
<tr>
<td><strong>Start/Stop time</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Start (maximum)</td>
<td>35 sec</td>
<td>25 s</td>
<td></td>
</tr>
<tr>
<td>Start (typical)</td>
<td>25 s</td>
<td>15 s</td>
<td></td>
</tr>
<tr>
<td>Stop (with power)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Heads</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read/write heads</td>
<td>5</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td><strong>Data Rates</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit cell time</td>
<td>103.3 ns</td>
<td>155.0 ns</td>
<td></td>
</tr>
<tr>
<td>Word rate (16 bit)</td>
<td>1.65 μsec</td>
<td>2.48 us</td>
<td></td>
</tr>
<tr>
<td>Word rate (18 bit)</td>
<td>1.86 us</td>
<td>2.79 us</td>
<td></td>
</tr>
<tr>
<td>Bit rate</td>
<td>9.677 MHz</td>
<td>6.45 MHz</td>
<td></td>
</tr>
<tr>
<td>No. of Addressable Registers in RM02/03 Adapter</td>
<td>16</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td><strong>Error Detection/Correction</strong></td>
<td>32 bit ECC/sector</td>
<td>32 bit ECC/sector</td>
<td></td>
</tr>
<tr>
<td>Time for Correction</td>
<td>4.47 ms, maximum</td>
<td>5.96 ms, maximum</td>
<td></td>
</tr>
</tbody>
</table>
**Environmental Limits**

**Temperature**
- Operating: 15.0° to 32.2°C (159° to 90°F) with a maximum gradient of 6.7°C (12°F) per hour.
- Nonoperating: −40° to 60°C (−40° to 151°F) with a maximum gradient of 14° (25°F) per hour.

**Relative humidity**
- Operating: 20 to 80 percent (providing there is no condensation)
- Nonoperating: 5 to 95 percent (providing there is no condensation)

**Altitude**
- Operating: 305 m (1000 ft) below sea level to 2000 m (6500 ft) above sea level.
- Nonoperating: 305 m (1000 ft) below sea level to 4572 m (15,000 ft) above sea level.

**RM03**
- Electrical voltages available (single-phase):
  - 120 Vac + 8, −18; 60 Hz
  - 240 Vac + 17, −27; 50 Hz
  - 100 Vac + 10, −10; 60 Hz
  - 100 Vac + 10, −10; 50 Hz

**RM02**
- 120 Vac + 8, −18; 60 Hz
- 240 Vac + 17, −27; 50 Hz

Start current for:
- 120 Vac, 60 Hz: 30 A rms, max
- 240 Vac, 50 Hz: 22 A rms, max
- 100 Vac, 60 Hz: 33 A rms, max
- 100 Vac, 50 Hz: 33 A rms, max

Running current in motion:
- Total: 12 A rms

Disk and carriage current:
- 120 Vac, 60 Hz: 5.5 A rms
- 240 Vac, 50 Hz: 12.5 A rms
- 100 Vac, 60 Hz: 12.1 A rms
- 100 Vac, 50 Hz: 5.2 A rms
DISKS

RM02/RM03

In standby mode
120 Vac, 60 Hz  4.5 A rms
240 Vac, 50 Hz  3.5 A rms
100 Vac, 60 Hz  4.5 A rms
100 Vac, 50 Hz  5.5 A rms
Line Cord Length  213.4 cm (7 ft)
Plug Type
120 V/60 Hz    NEMA 5-15 P
240 V/50 Hz    NEMA 6-15 P
100 V/60 Hz    NEMA 5-15 P
100 V/50 Hz    NEMA 5-15 P
Disk Cartridge Type
              RM03P

Specifications
Type
Disk Diameter
Number of Disks
Number of Recording Services
Cylinders per Disk Pack 823
Total Number of Tracks 4115 per disk pack
Tracks per cylinder 5
Bad Sector File Cylinder 822, track 4
Environmental Requirements
Temperature range (operation)

Limits
9877 disk pack
35.56 cm (14 in.)
5 (the upper and lower disks are not used for recording)
5 read/write and 1 read-only servo surface
10° to 57°C (50° to 135°F); temperature change rate not to exceed 0.1°C (0.2°F) per minute.
—40° to 65°C (—40° to 150°F); temperature change rate not to exceed 14°C (25°F) per hour.
8 to 80 percent

Relative Humidity
Operating and nonoperating
Wet Bulb Reading
Operating
Nonoperating
Altitude

25°C (78°F), maximum
30°C (85°F), maximum
DISKS

RM02/RM03

Operating Mean sea level to 3050 m (10,000 ft)
Nonoperating Mean sea level to 12,190 m (40,000 ft)

Stray magnetic fields Not to exceed 50 oersteds.
Operating and nonoperating
The RP04, RP05 and RP06 disk drives comprise DIGITAL's large-capacity disk family. Offering both high performance and the lowest price per megabyte of storage, these drives use a removable disk pack, and have a wide variety of features. The RP04, RP05, and RP06 drives can be mixed on the same controller and are software compatible.

**FEATURES:**

**Speed**
- 28 milliseconds average seek time
- 1.24 microsecond/byte peak transfer time
- overlapped seeks
- direct memory access
- dual access option

**Capacity**
- RP04/RP05: 100 million 8-bit bytes per disk pack (unformatted)
- RP06: 200 million 8-bit bytes per disk pack (unformatted)
- a maximum of 1.6 billion 8-bit bytes per controller
Human Engineering
- on-line pack formatting

Reliability
- error detection, logging, and correction
- extensive diagnostic software support
- parity checking on all data and control transfer between controller and disk drive
- offset positioning

<table>
<thead>
<tr>
<th>Name</th>
<th>RP04</th>
<th>RP05</th>
<th>RP06</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Formatted Capacity</td>
<td>88M</td>
<td>88M</td>
<td>176M</td>
</tr>
<tr>
<td>per Drive (bytes)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of Drives</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>per Control</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Formatted Capacity</td>
<td>704M</td>
<td>704M</td>
<td>1408M</td>
</tr>
<tr>
<td>(on-line) per Control</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(bytes)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Access Time</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Average Access Time</td>
<td>36 msec</td>
<td>36 msec</td>
<td>36 msec</td>
</tr>
<tr>
<td>Average Transfer Time</td>
<td>1.24μsec</td>
<td>1.24μsec</td>
<td>1.24μsec</td>
</tr>
<tr>
<td>per Byte</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

DESCRIPTION

Disk Drive
The RP04 and RP05 have a formatted disk capacity of 88 megabytes, the RP06 has a formatted 176 megabyte capacity. The RP05 is field-upgradable to an RP06: the high track density of the RP06 requires different media, read/write circuitry, and heads.

All three drives function identically. Average access time is 36 milliseconds, which includes the time for head positioning and rotational latency. The peak transfer rate is 806,000 bytes per second.

The disk drives are designed for reliability. A phase-lock-loop clock system and modified frequency modulation (MFM) recording offer the latest in reliable reading and recording techniques. Error detection and correction hardware in each drive provide an error correction code (ECC) for correcting any error burst of up to 11 consecutive bits within a 512-byte data field. Software can correct these data field errors without rereading the disk.
Program-controlled head offset positioning corrects for slight mechanical misalignment between the heads and the disk pack; the head can be moved about the track centerline in incremental steps. This feature virtually guarantees that packs can be transported between different drives.

To further increase data integrity, the drive has a hardware write-check capability and verification of sector, track, and cylinder positioning. Built-in registers for disk data path checkout simplify maintenance. Both the RP04 and RP05 use the same disk pack so that packs written on one type of drive can be read on the other. The RP06 uses a pack that is RP06-specific.

The RP05 and RP06 drives have removable logical address units that plug into the front of the drive to simplify subsystem reconfiguration. This feature is optionally available on the RP04 with a logical address selection switch from Computer Special Systems (see the section on the RP04H).

**Disk Subsystem**
The RP04, RP05 and RP06 disk drives use the same controllers and can be intermixed.

There are two disk subsystems:
- RJP04/05/06 for the PDP-11/34 through the PDP-1160 systems
- RWP04/05/06 for the PDP-11/70

All subsystems are expandable to eight disk drives per controller, that is to 800 megabytes on the RP04/RP05 subsystems, and to 1600 megabytes on the RP06 subsystems. The removable disk packs offer the flexibility of unlimited off-line storage. All subsystems transfer at the same speed (1.24 microseconds per byte maximum).

On multidrive systems, positioning operations can be overlapped for efficiency. While one drive is reading or writing, one or more other drives can be positioning to a new cylinder for the next transfer.

Parity checking is done on both data and control information transfers for increased reliability. The controller also detects and flags memory parity errors. The disk system interrupts the processor on command completion and on error conditions. Extensive error indicators allow on-line diagnostics, and status indicators allow complete program control.
The RJP04/05/06 have additional program-controlled hardware features:

- hardware-generated rotational position sensing (RPS). Available for optimizing scheduling programs.
- implied seek. For ease of programming, the read command causes automatic seek, when not on the cylinder.
- mid-transfer seek, issues an automatic seek to the next cylinder, following the operation of the last track and sector of the current cylinder, to enhance spiral read/write operation.
- header-compare inhibit, data can be read with or without header information.
- error-correction inhibit, disables the error-correction process to allow for throughput flexibility.

**Programmable Features**

**REGISTERS**

**Control and Status 1 Register (RJCS1) 776 700**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>Special Condition (SC)</td>
<td>Set by TRE or ATTN or I/O bus control parity error. Cleared by UNIBUS A INIT, Controller Clear, or by removing the ATTN condition. Read only.</td>
</tr>
<tr>
<td>14</td>
<td>Transfer Error (TRE)</td>
<td>Set by DLT, WCE, UPE, NED, NEM, PGE, MF, MDPE, or a drive error during a data transfer. Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or by loading a data transfer command with GO set. Read/write.</td>
</tr>
<tr>
<td>13</td>
<td>Mass I/O Control Bus Parity Error (MCPE)</td>
<td>Set by parity error on control bus while reading a remote register (located in the drive). Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or by loading a data transfer command with the GO set. Parity errors, which occur on the I/O control bus while</td>
</tr>
</tbody>
</table>

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writing a drive register, are detected by the drive and cause the PAR error (RPER1 Register, bit 3) to set. Read only.

Bit: 12  Name: Not used
Function: Always read as a 0.

Bit: 11  Name: Drive Available (DVA)
Function: Set when device is not busy on another port.
Reset by device from the other port when device is busy on that port. This bit is used in dual controller configurations. Read only.

Bit: 10  Name: Port Select (PSEL)
Function: When PSEL = 1, data transfer is via UNIBUS B; when PSEL = 0, data transfer is via UNIBUS A. Cleared by UNIBUS A INIT, Controller Clear, or by writing a 0 in this bit position. Read/write.

Bit: 9  Name: UNIBUS Address Extension Bits (A17)
Function: Cleared by UNIBUS A INIT, Controller Clear, or by writing zeros in these bit positions. Upper extension bits of the BA Register. Read/write.

Bit: 8  Name: UNIBUS Address Extension Bits (A16)
Function: Cleared by UNIBUS A INIT, Controller Clear, or by writing zeros in these bit positions. Upper extension bits of the BA Register. Read/write.

Bit: 7  Name: Ready (RDY)
Function: RDY normally = 1. During data transfers, RDY = 0. When a data transfer command code (51(sub)8-77(sub)8) is written into RPCS1, RDY is reset. At the termination of the data transfer, RDY is set. Read only.

Bit: 6  Name: Interrupt Enable (IE)
Function: IE is a control bit which can be set only under program control. When IE = 1, an interrupt may occur due to RDY or ATTN being asserted. Cleared by UNIBUS A INIT, Controller Clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled. Read/write.

Bit: 5-0  Name: F4-F0 and GO Bit.
Function: F4-F0 and the GO bit (FO) are function (command) code control bits.
<table>
<thead>
<tr>
<th>F4F4</th>
<th>F3F3</th>
<th>F2F2</th>
<th>F1F1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>Unload</td>
<td>(Standby)</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>Recalibrate</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Drive Clear</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>Release (Dual Port Operation)</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>Search Command</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Write Check Data</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Write Check Header and Data</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Write Data</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Write Header and Data</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Read Data</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Read Header and Data</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Seek Command</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Offset Command</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Return To Centerline</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Pack</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Acknowledge</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>144</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### DISKS

<table>
<thead>
<tr>
<th>F4F4</th>
<th>F3F3</th>
<th>F2F2</th>
<th>F1F1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Read-in-Preset</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>Illegal Functions</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

The GO bit (RPCS1, bit 0) must be set to cause the controller or drive to respond to a command. The GO bit is reset by the drive after command execution. The function code bits are stored in the selected drive.

Cleared by UNIBUS A INIT or Controller Clear (will abort command execution in all drives). Read/write.

### Word Count Register (RPWC) 776 702

<table>
<thead>
<tr>
<th>Bit: 15-0</th>
<th>Name: Word Count (WC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function:</td>
<td>Set by the program to specify the number of words to be transferred (twos complement form). This register is cleared only by writing zeros into it. Increment for each data transfer. Read/write.</td>
</tr>
</tbody>
</table>

### UNIBUS Address Register (RPBA) 776 704

<table>
<thead>
<tr>
<th>Name: UNIBUS Address (BA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Loaded by the program to specify the starting memory address of a transfer. Cleared by UNIBUS A INIT or by Controller Clear. The BA Register is incremented by 2 after each transfer of a word to or from memory. Read/write.</td>
</tr>
</tbody>
</table>

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**DISKS**

**RP04/05/06**

**DESIRED SECTOR/TRACK ADDRESS (RPDA) REGISTER (776706)**

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>D</td>
<td>D</td>
<td>TA5</td>
<td>TA4</td>
<td>TA3</td>
<td>TA2</td>
<td>TA1</td>
<td>D</td>
<td>D</td>
<td>S35</td>
<td>S34</td>
<td>S33</td>
<td>S32</td>
<td>S31</td>
<td></td>
</tr>
</tbody>
</table>

**Bit: 12-8 Name:** Track Address (TA)

**Function:** Set by the program to specify the track on which a transfer is to start. Cleared by UNIBUS A INIT, Controller Clear, or by performing a Drive Clear function. Incremented by the drive when sector 21 (16-bit format) or sector 19 (18-bit format) is reached. Read/write.

**Bit: 5-0 Name:** Sector Address (SA)

**Function:** Set by a program to specify the sector on which a transfer is to start. Cleared by UNIBUS A INIT, Controller Clear, or by performing a Drive Clear function. Incremented by the drive after each sector has been transferred. Read/write.

**Control and Status Register (RPCS2) 776 710**

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>DLT</td>
<td>WCE</td>
<td>UPE</td>
<td>NED</td>
<td>NEM</td>
<td>PGE</td>
<td>MXF</td>
<td>MOPE</td>
<td>OR</td>
<td>IR</td>
<td>CLR</td>
<td>PAT</td>
<td>BAI</td>
<td>U2</td>
<td>U1</td>
<td>U0</td>
</tr>
</tbody>
</table>

**Bit: 15 Name:** Data Late (DLT)

**Function:** Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write-check operation at the time the drive demands a transfer. Also set when the controller is performing a data transfer operation over the second UNIBUS (PSEL = 1) and a UNIBUS B INIT is received on that port. Cleared by UNIBUS A INIT, Controller Clear, 1 Error Clear or loading a data transfer command with GO set.

DLT causes TRE. A DLT error indicates a severely overloaded bus. Can also be set by the program reading or writing the RPDB Register. Read only.

**Bit: 14 Name:** Write Check Error (WCE)

**Function:** Set when the controller is performing a write-check operation and a word on the disk does not match the corresponding word in memory. Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.

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DISKS

RP04/05/06

WCE causes TRE. If a mismatch is detected during a write-check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RPBA (and extension) is the address of the word following the one which did not match (if BAI is not set). The mismatched data word from the disk is displayed in the data buffer (RPDB). Read only.

**Bit: 13**  **Name:** Parity Error (PE)

**Function:** Set if the parity lines indicate a parity error while the controller is performing a write or write-check command. Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.

PE causes TRE. When the UNIBUS is selected to do 18-bit data transfers, the PE error is disabled. When a parity error occurs, the RPBA Register contains the address +2 of the memory word with the parity error (if BAI is not set). This bit may be set by program control for diagnostic purposes. Read/write.

**Bit: 12**  **Name:** Non-existent Drive (NED)

**Function:** Set when the program reads or writes a drive register in a drive (selected by U(2:0)) which does not exist or is powered down. (The drive fails to assert TRA within 1.5us after assertion of DEM.) Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. NED causes TRE. Read only.

**Bit: 11**  **Name:** Non-existent Memory (NEM)

**Function:** Set when the controller is performing a DMA transfer and the memory address specified in RPBA is non-existent (does not respond to MSYN within 10us). Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. NEM causes TRE. The RPBA contains the address +2 of the memory location causing the error. Read only.

**Bit: 10**  **Name:** Program Error (PGE)

**Function:** Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.

147
PGE causes TRE. The data transfer command code is inhibited from being written. Read only.

**Bit: 9**  
**Name:** Missed Transfer (MXF)  
**Function:** Set if the drive does not respond to a data transfer command within 250ms. Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.

MXF causes TRE. This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive which has ERR set, or if the drive fails to initiate the command for any reason (such as a parity error). Read/write.

**Bit: 8**  
**Name:** Mass Data Bus Parity Error (MDPE)  
**Function:** Set when a parity error occurs on the I/O bus data while doing a read or write-check operation. Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.

MDPE causes TRE. Parity errors on the data bus during write operations are detected by the drive and cause the PAR error (RPER1 Register, bit 3). Read only.

**Bit: 7**  
**Name:** Output Ready (OR)  
**Function:** Set when a word is present in RPDB and can be read by the program. Cleared by UNIBUS A INIT, Controller Clear, or by reading DB.

Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to read the DB Register before OR is asserted will cause a DLT error. Read only.

**Bit: 6**  
**Name:** Input Ready (IR)  
**Function:** Set when a word may be written in the DB Register by the program. Cleared by reading the DB.

Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to write the DB Register before IR is asserted will cause a DLT error. Read only.

**Bit: 5**  
**Name:** Controller Clear (CLR)  
**Function:** When a 1 is written into this bit, the controller and all drives are initialized. UNIBUS A INIT also causes Controller Clear to occur. Write only.
Bit: 4  Name: Parity Test (PAT)
Function: While PAT is set, the controller generates even parity on both the control bus and data bus of the I/O bus. When clear, odd parity is generated. Cleared by UNIBUS A INIT or Controller Clear. While PAT is set, the controller checks for even parity received on the data bus but not on the control bus. Read/write.

Bit: 3  Name: UNIBUS Address Increment Inhibit (BAI)
Function: When BAI is set, the controller will not increment the BA Register during a data transfer. This bit cannot be modified while the controller is doing a data transfer (RDY negated). Cleared by UNIBUS A INIT or Controller Clear. When set during a data transfer, all data words are read from or written into the same memory location. Read/write.

Bit: 2-0  Name: Unit Select (U2:0)
Function: These bits are written by the program to select a drive. Cleared by UNIBUS A INIT or Controller Clear.
The unit select bits can be changed by the program during data transfer operations without interfering with the transfer. The RP04 Registers contain bits which come from the selected drive. Read/write.

**Drive Status Register (RPDS) 776 712**

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<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
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<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATA</td>
<td>ERR</td>
<td>P2P</td>
<td>MOL</td>
<td>WRL</td>
<td>LST</td>
<td>PGM</td>
<td>DPR</td>
<td>DRY</td>
<td>VV</td>
<td>DE1</td>
<td>DL64</td>
<td>DRV</td>
<td>DGB</td>
<td>DF20</td>
<td>DF5</td>
</tr>
</tbody>
</table>

Bit: 15  Name: Attention Active (ATA)
Function: An attention condition in a drive will set the ATA bit and summary line. It is cleared by UNIBUS A INIT, Controller Clear, loading a command with the GO bit set, or loading a one in the RPAS Register corresponding to the drive's unit number. The last two methods of clearing the ATA bit will not clear the error indicators in the drive.

An attention condition is caused by any error in the Error Registers except during data transfers, the completion operation, the completion of a start up cycle (with the MOL bit set), dual controller operation with drive presently available (drive was requested before
but was not available) and correct sector identification (Search command only). Read only.

NOTE
The ATA bit will not set if the drive was switched from a neutral position. The ATA bit may be reset by writing a 1 into the Attention Summary Register. Writing a zero into register has no effect.

Bit: 14  Name: Error (ERR)
Function: Set when one or more of the errors in the Error Registers (RPER1, RPER2, RPER3) in a selected drive is set. Cleared by UNIBUS A INIT, Controller Clear, or Drive Clear.

A composite error bit which is the logical OR of all the error conditions in the RPER1, RPER2, or RPER3 Registers. This ERR bit is not cleared by loading a command other than Drive Clear. While ERR is asserted, commands other than Drive Clear are not accepted by the drive. Read only.

Bit: 13  Name: Positioning in Progress (PIP)
Function: Set by the drive when a positioning command is accepted. These commands are Seek, Offset, Return to Center line, Recalibrate, Unload, and Search. The PIP bit will not be set during implied seeks or mid-transfer seeks. Cleared when the moving function is completed. The DRY and ATA bits are also set at this time (normal termination). Read only.

Bit: 12  Name: Medium On-Line (MOL)
Function: Set by the drive upon the successful completion of the start up cycle. Cleared when the spindle is powered down or the device is switched off-line (with the spindle still up to speed) for diagnostic purposes. Read only.

Bit: 11  Name: Write Lock (WRL)
Function: Set when the RP04 will not accept Write commands. Read only.

Bit: 10  Name: Last Sector Transferred (LST)
Function: Set by the drive on the rising edge of EBL pulse when the last addressable sector on the disk pack has been read or written. Cleared when a new function command is received. Read only.
Bit: 9  Name: Programmable (PGM)
Function: Set when the CONTROLLER SELECT switch is in the A/B position indicating that the device is accessible from either Port A or Port B. Cleared when the CONTROLLER SELECT switch is in Port A or Port B position. Read only.

Bit: 8  Name: Drive Present (DPR)
Function: Always set for single controller operation. In dual controller operation, this bit is set for the controller which has seized the RP04 and is reset for the other controller. When the RP04 switches from one controller to a second controller and the ATA line (bit 15) is high, DPR is set. This indicates that the RP04 is connected to the asynchronous control bus of this controller. If the RP04 is in the programmable state (PGM bit = 1) when requested, DPR will be set and the drive will switch immediately regardless of the ATA bit. Read only.

Bit: 7  Name: Drive Ready (DRY)
Function: Set at the completion of every command, data handling, or mechanical motion. Cleared at the initiation of a command. If this bit is reset, the controller cannot issue another command. When set, this bit indicates the readiness of the RP04 device to accept a new command. Read only.

Bit: 6  Name: Volume Valid (VV)
Function: Set by the Pack Acknowledge or Read-In Preset command from either port. Cleared by the drive whenever it cycles up from the off state.

When reset, this bit indicates when the drive has been put off-line and on-line and when a disk pack may have been changed. Read only.

Bit: 5  Name: Difference Equals 1 (DE1)
Function: Set when the device has detected a value equal to 1 in the difference counter during a head load sequence. Cleared by a File Ready at the completion of a head load sequence. Read only.

Bit: 4  Name: Difference Less Than 64 (DL64)
Function: Set when the device has detected a value less than 64 in the difference counter during the reverse seek of
the head load sequence. Cleared by a File Ready at the completion of a head load sequence. Read only.

Bit: 3  Name: Go Reverse (GRV)
Function: Set when the device has detected the GO Reverse signal during a head load sequence. Cleared by File Ready at the completion of a head load sequence. Read only.

Bit: 2  Name: Drive to Inner Guard Band (DIGB)
Function: Set when the drive has detected the Drive to Inner Guard Band signal during a head load sequence. Cleared by File Ready at the completion of a head load sequence. Read only.

Bit: 1  Name: Drive Forward 20 in./sec (DF20)
Function: Set by the drive when it has detected the DF20 Signal during a head load sequence. Cleared by File Ready at the completion of a head load sequence. Read only.

Bit: 0  Name: Drive Forward 5 in./sec (DF5)
Function: Set when the drive has detected a DF5 signal while in the head load mode after a sequence start pulse was recognized. Cleared by File Ready at the completion of a head load sequence. Read only.

Error Register 01 (RPER1) 776 714

Bit: 15  Name: Data Check (DCK)
Function: Set during a read operation when the ECC hardware has detected an ECC error after the ECC bytes have been looked at. Cleared by a Drive Clear command, UNIBUS A INIT, Controller Clear, or by writing zeros into the register.

If the Error Correction Code/Inhibit (ECI) bit is off, the RP04 will go into the error correction process. DCK will remain set. If ECI bit is on, the error correction process is inhibited even though an ECC error was detected at the end of a data transmission. Read/write.

Bit: 14  Name: Unsafe (UNS)
Function: Set when the drive detects a condition which prevents
it from operating. Cleared by a Drive Clear or by writing zeros into the register. If this does not cause the UNS condition to disappear, the RP04 must be powered down and cycled up to insure clearing the errors including the UNS bit. This bit is a composite error bit of the unsafe error conditions in the RPER2 and RPER3 Registers. Read/write.

**Bit: 13 Name:** Operation Incomplete (OPI)

**Function:** Set when a Read or Write command, involving header search, has not begun transmitting data (sync clocks) within three index pulses. OPI will also set during a search operation where a sector count match is not made after a maximum of three index pulses have been encountered. Cleared by a UNIBUS A INIT, Drive Clear, Controller Clear, or by writing zeros into the register. Read/write.

**Bit: 12 Name:** Drive Timing Error (DTE)

**Function:** Set when a failure has occurred in the clocking or timing circuits of the drive. Cleared by UNIBUS A INIT, Drive Clear, Controller Clear, or by writing zeros into the register. Read/write.

**Bit: 11 Name:** Write Lock Error (WLE)

**Function:** Set when the operating system attempts to issue a write command on a device in Write Protect mode. A manual WRITE PROJECT switch can place the device in this mode during normal operations. Cleared by UNIBUS A INIT, Drive Clear, Controller Clear, or by writing zeros into the register. Read/write.

**Bit: 10 Name:** Invalid Address Error (IAE)

**Function:** Set when the address in the Desired Cylinder Register (RPDC) and the Desired Sector/Track Address Register (RPDA) is invalid and a seek or search operation is initiated. Cleared by UNIBUS A INIT, Drive Clear, Controller Clear, or by writing zeros into the register. Read/write.

**Bit: 9 Name:** Address Overflow Error (AOE)

**Function:** Set when the Desired Cylinder Register (RPDC) overflows during a read or write. Cleared by UNIBUS A INIT, Drive Clear, Controller Clear, or by writing zeros into the register. Setting of this bit indicates that the Desired Cylinder Address Register has exceeded cylinder address 410. Read/write.
<table>
<thead>
<tr>
<th>Bit: 8</th>
<th><strong>Name:</strong> Header CRC Error (HCRC)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Function:</strong></td>
<td>Set by a CRC error in the header. Cleared by UNIBUS A INIT, Drive Clear, Controller Clear, or by writing zeros into the register. Read/write.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit: 7</th>
<th><strong>Name:</strong> Header Compare Error (HCE)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Function:</strong></td>
<td>If the sector counter is equal to the desired field, the header associated with that sector is compared with the desired header words. If the header matches the desired cylinder sector/track address, the header field is the required one. If the header does not match the desired cylinder and sector/track address, the HCE bit is set. If the sector address and sector count match, but a CRC error is detected following the header compare, the HCE bit is reset and the HCRC bit is set. Cleared by UNIBUS A INIT, Drive Clear, Controller Clear, or by writing zeros into the register. Read/write.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit: 6</th>
<th><strong>Name:</strong> ECC Hard Error (ECH)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Function:</strong></td>
<td>Set when the conclusion of the error correction procedure indicates that the error was a noncorrectable ECC error. Cleared by UNIBUS A INIT, Drive Clear, Controller Clear, or by writing zeros into the register. Read/write.</td>
</tr>
</tbody>
</table>

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<thead>
<tr>
<th>Bit: 5</th>
<th><strong>Name:</strong> Write lock Fail (WCF)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Function:</strong></td>
<td>Set during a write operation when the Write Clock signals are not received by the drive. Cleared by UNIBUS A INIT, Drive Clear, Controller Clear, or by writing zeros into the register. Upon recognizing a WCF condition, the drive will abort the command. Read/write.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit: 4</th>
<th><strong>Name:</strong> Format Error (FER)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Function:</strong></td>
<td>Set where the prerecorded (pack formatting) flag bit on the header is not equal to the corresponding flag bit in the Offset Register (bit location 12, RPOF). Cleared by UNIBUS A INIT, Drive C‘ear, Controller Clear, or by writing zeros into the register. Read/write.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit: 3</th>
<th><strong>Name:</strong> Parity Error (PAR)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Function:</strong></td>
<td>Set when a parity error is detected during data transmission over the asynchronous control bus (odd parity) or over the synchronous data bus. Cleared by a Drive Clear command, an Initialize pulse, or by writing zeros into the register. Read/write.</td>
</tr>
</tbody>
</table>

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<thead>
<tr>
<th>Bit: 2</th>
<th><strong>Name:</strong> Register Modification Refused (RMR)</th>
</tr>
</thead>
</table>
Function: Set when a write is attempted into any register (except RPAS) during an operation. Cleared by UNIBUS A INIT, Drive Clear, Controller Clear, or by writing zeros into the register. Read/write.

Bit: 1 Name: Illegal Register (ILR)
Function: See when the device control logic decodes a nonexistent register address from the register select line (RS00-RS04). Cleared by UNIBUS A INIT, Drive Clear, Controller Clear or by writing zeros into the register. Attempting to write into a read-only register will not cause the ILR to set; the bits received will be ignored and no other error will be flagged. Read/write.

Bit: 0 Name: Illegal Function (ILF)
Function: Set when the function code in the Control Register does not correspond to an implemented command on this drive. Cleared by UNIBUS A INIT, Drive Clear, Controller Clear, or by writing zeros into the register. Read/write.

Attention Summary Register (RPAS) 776 716

<table>
<thead>
<tr>
<th>Bit</th>
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</table>

Bit: 7-0 Name: Attention Active (ATA)
Function: Each bit sets when the corresponding drive asserts its ATA bit. All bits are cleared by UNIBUS A INIT or Controller Clear. Individual bits are cleared by loading a function code with the GO bit in the corresponding drive or by writing a 1 in the ATA bit positions of this register. Writing a zero has no effect.

Each drive’s ATA bit is displayed individually in bit 15 of RPDS. Each drive responds in the bit position which corresponds to its unit number, drive 2 responds in bit position 2. Read/write.

Look Ahead Register (RPLA) 776 720

<table>
<thead>
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<th>Bit</th>
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</tbody>
</table>
Bit: 10-6  Name: Sector Count (SC)
Function: These five-bit registers address the required sector on the data track through an exclusive OR network in conjunction with the RPDA Register. The sector count is continually being incremented on the rising edge of each sector pulse and reflects the exact location of the data track in relation to the head. Each time the rising edge of the index pulse is encountered, the sector count field resets to zero. The maximum sector count is 21 for the 16-bit word format and 19 for the 18-bit data word format. If a sector count malfunction occurs during an operation, the RP04 will set the Operation Incomplete (OPI) error bit after three index pulses, without a sector count/desired sector field match. A malfunctioning sector count field is a catastrophic error since the required sector cannot be recovered. The RP04 looks at every header on the data track. In the event of an error condition, no error is reported until after the sector counter matches the sector field, which is an indication that the desired sector has been found. Read only.

Bit: 5-4  Name: Encoded Extension Field (EXT)
Function: These two bits are used to specify the approximate location of the heads within a sector.

```
<table>
<thead>
<tr>
<th>EXT 1</th>
<th>EXT 0</th>
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<tbody>
<tr>
<td>Head Location</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>20 to 40%</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>40 to 80%</td>
<td>1</td>
</tr>
<tr>
<td>&gt; 80% (in last 20% of sector)</td>
<td></td>
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</table>
```

Data Buffer Register (RPDB) 776 722

```
<table>
<thead>
<tr>
<th>DB15</th>
<th>DB14</th>
<th>DB13</th>
<th>DB12</th>
<th>DB11</th>
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</tbody>
</table>
```

Bit: 15-0  Name: Data Buffer (DB)
Function: When read, the contents of OBUF (internal register)
are delivered. Upon completion of the read, the next sequential word in the Silo will be clocked into OBUF. When written, data is loaded into IBUF (internal register) and allowed to sequence into the Silo if space is available. Used by the program for diagnostic purposes. Read/write.

Maintenance Register (RPMR) 776 724
The Maintenance Register simulates various signals from the disk for diagnostic testing.

<table>
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<tr>
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<td>ZDT</td>
<td>DEN</td>
<td>ECCE</td>
<td>MWR</td>
<td>MRD</td>
<td>MSCLK</td>
<td>MIND</td>
<td>MCLK</td>
<td>DMD</td>
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FUNCTION BITS

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<tr>
<td>NBA</td>
<td>TAP</td>
<td>MOH</td>
<td>Ø</td>
<td>DRQ</td>
<td>Ø</td>
<td>Ø</td>
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<td>DT04</td>
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<td>DT01</td>
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</tbody>
</table>

Drive Type Register (RPDT) 776 726

Bit: 15-14 Name:
Function: Always a 0.

Bit: 13 Name: Moving Head (MOH)
Function: Always a 1. Read only.

Bit: 11 Name: Drive Request Required (DRQ)
Function: DRQ = 1 dual controller option available;
DRQ = 0 dual controller option not available. Read only.

Bit: 8-0 Name: Drive Type Number (DT)
Function: The device type number for the RP04 is 20(sub)8 — 27(sub)8. Read only.

Serial Number Register (RPSN) 776 730

<table>
<thead>
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<th>15</th>
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The purpose of this register is to distinguish a drive from similar drives attached to the same controller. The serial number provides a means of distinguishing between different RP04s with identical characteristics, which are connected to the same controller. Read only.

**Offset Register (RPOF) 776 732**

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<tr>
<td></td>
<td>SCG</td>
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<td>FMT</td>
<td></td>
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<td>ECI</td>
<td></td>
<td></td>
<td>HCI</td>
<td></td>
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</tr>
</tbody>
</table>

**Bit: 15**  **Name:** Sign Change (SCG)

**Function:** Used when a DDU and alignment (CE) pack are available to verify head alignment. Beginning from a known position and issuing continuous Offset commands toward the actual track center line, the bit is guaranteed to change states when the head R/W gap is actually over the true track center line. Read/write.

**Bit: 12**  **Name:** Format Bit (FMT 22)

**Function:** Set to a 1 when 16-bit/word format is used (16 bits/word X 256 words/sector). Set to a zero when 18-bit/word format is used (18 bits/word X 256 words/sector). Cleared by Read-in Preset command.

This bit will be written in the cylinder address sector recorded on the data pack. Normally, this bit will be written during the format operation (write header and data). Upon reading a header from the pack, the recorder bit will be compared with bit 12 of the Offset Register. If the bits do not compare, the Format Error (FER) bit will be set. Read/write.

**Bit: 11**  **Name:** Error Correction Code Inhibit (ECI)

**Function:** Set when the software desires to inhibit error correction. If ECI is set, error correction code is disallowed; if ECI is reset, the error correction process is allowed. Cleared by Read-In Preset command.

If a data error is detected at the end of the data transmission in the read mode with the ECI bit reset, the RP04 device will immediately go into the ECC correction process. Prior to beginning the correction routine, the device will also set the Data Check (DCK) error
bit, which will remain set until a Drive Clear command or an INIT pulse is received. Read/write.

**Bit: 10**  **Name:** Header Compare Inhibit (HCI)

**Function:** Set when the software desires to inhibit header compare. Cleared by Read-In Preset command. When the RP04 sees this bit asserted, it will ignore the header compare logic and CRC check. With HCI set, the device logic depends only on the sector count field/desired address field comparison for sector identification. If the sector count field is out of sequence, the wrong sector may be affected. Read/write.

**Bit: 7-0**  **Name:** Offset Information (OFS)

**Function:** Set under software control. Cleared by Read-In Preset command or at the completion of the offset operation.

<table>
<thead>
<tr>
<th>Position</th>
<th>Code Word OF0-OF7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value/Direction</td>
<td>(microinches)</td>
</tr>
<tr>
<td>OF7  OF6  OF5  OF4</td>
<td>OF3-OF0</td>
</tr>
<tr>
<td>1st offset 0</td>
<td>0 0 0 1</td>
</tr>
<tr>
<td>0 +400 2nd offset 1</td>
<td>0 0</td>
</tr>
<tr>
<td>1 0 -400 3rd offset 0</td>
<td>0 0</td>
</tr>
<tr>
<td>1 0 0 +800 4th offset 1</td>
<td>0 0</td>
</tr>
<tr>
<td>0 1 0 0 -800 5th offset</td>
<td>0 0 0 1</td>
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<tr>
<td>0 0 1 1 1 0 +12006th offset</td>
<td>1 0 0 -1200Track</td>
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<tr>
<td>Center line</td>
<td>Read/write.</td>
</tr>
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</table>

**Desired Cylinder Register (RPDC) 776 734**

- **NOT USED**
- **NINE-BIT DESIRED CYLINDER ADDRESS**

This register is a read/write register and contains the address of the cylinder to which the positioner is to move. This address is loaded in the Desired Cylinder Address Register via the interface.

The device logic will immediately compare the contents of the Desired Cylinder Address Register with the Current Cylinder Address Register through the subtract logic.
DISKS

The Current Cylinder Address Register reflects, at all times, the address of the cylinder which the positioner is presently addressing. The results of the subtraction between the two registers will specify the magnitude and the direction of seek.

After the Desired Cylinder Address Register has been loaded, a function code (Read, Write, or Seek command) specified, and the GO bit set in the Control Register, the following events will take place:

• If the subtract logic output equals 0, the desired cylinder address equals the current cylinder address and the positioner will not move.

• If the subtract logic output is not equal to 0, the RP04 device will initiate a seek whose direction and magnitude are specified by the output of the subtract logic. Consequently, when the GO bit sets with a Read, Write, Search, or Seek command in the Control Register, the contents of the Desired Cylinder Address Register are presumed valid.

Prior to informing the controller that the seek was completed, the RP04 drive will internally transfer, in parallel, the contents of the Desired Cylinder Address Register into the Current Cylinder Address Register, so that the latter reflects the actual cylinder the positioner is addressing.

Throughout the search portion of a Read or Write command and the actual data transfer, registers have identical contents.

If the command was a Seek command, the actual command termination would occur with the DRY bit set and the Desired Cylinder Address transferred into the Current Cylinder Address at the actual completion of the seek instruction.

Throughout the actual mechanical movement, the output of the subtract logic will indicate the magnitude and direction of the seek. The device logic will actually do the decrementing of a cylinder difference counter and move the positioner to address the right cylinder.

The Desired Cylinder Address Register will be cleared by the Read-in Preset command.

Although the Desired Cylinder Address is a read/write register, the RP04 will not allow any writing in this register during a seek operation. Since the maximum number of cylinders in the RP04 is 411, only 9 bits are necessary to specify the Desired Cylinder Address Register.
The Invalid Address Error (IAE) bit will be set when, upon asserting the GO bit, the contents of the Desired Cylinder Address Register contain an address larger than 410.

**Current Cylinder Address Register (RPCC) 776 736**

This register is a read-only register and operates in conjunction with the Desired Cylinder Address Register.

By monitoring this register, the software can determine the time required to execute the next Seek command based on the address in this register. This address reflects the exact position of the RP04 positioner whenever it is not in motion.

The Current Cylinder Address Register will reset to zero:
- on a recalibrate instruction
- on a catastrophic error (where the device retracts the heads automatically)
- following the completion of the cycle-up process (heads loaded)

The Current Cylinder Address Register will not reset to zero if:
- a Drive Clear command is issued
- an initialize (INIT) pulse is received.

**Error Register 2 (RPER2) 776 740**

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<th>15</th>
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<tbody>
<tr>
<td>ACU</td>
<td>Ø8</td>
<td>PLU</td>
<td>NRVU</td>
<td>IVE</td>
<td>NHS</td>
<td>MHS</td>
<td>WRU</td>
<td>FEN</td>
<td>TUF</td>
<td>TOF</td>
<td>MSE</td>
<td>CSU</td>
<td>WSU</td>
<td>CSF</td>
<td>WCU</td>
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</tbody>
</table>

**Bit: 15**  
Name: AC Unsafe (ACU)  
Function: When set, this bit indicates that the RP04 has detected an interruption of ac power for the dc power supply. Cleared by a Drive Clear command or an INIT pulse. Read/write.

**Bit: 14**  
Name:  
Function: Not used.
Bit: 13  **Name:** PLO Unsafe (PLU)
**Function:** Set when the RP04 has detected a loss of synchronization of the read/write phase-locked oscillator (PLO). Cleared by a Drive Clear or an INIT pulse. Read/write.

Bit: 12  **Name:** 30 Volts Unsafe (30 VU)
**Function:** Set when the drive has detected a loss of unregulated 30-volt dc power. Cleared by a Drive Clear or an INIT pulse. Read/write.

Bit: 11  **Name:** Index Error (IXE)
**Function:** Set when the RP04 detects a missing index pulse or an invalid index pulse. Cleared by the next valid pulse. Read/write.

Bit: 10  **Name:** No Head Selection (NHS)
**Function:** Set when the RP04 detects the absence of head selection when a Read or Write command is present. Cleared by a Drive Clear or an INIT pulse. Read/write.

Bit: 9  **Name:** Multiple Head Select (MHS)
**Function:** Set when the RP04 has detected the concurrent selection of more than one head. Cleared by a Drive Clear or an INIT pulse. Read/write.

Bit: 8  **Name:** Write Ready Unsafe (WRU)
**Function:** Set when the RP04 detects the presence of a Write command when the heads are not on the cylinder. Cleared by a Drive Clear or an INIT pulse. Read/write.

Bit: 7  **Name:** Failsafe Enabled (FEN)
**Function:** Set when the RP04 detects an open circuit breaker in the 48-volt power driver supply. Upon detecting this error bit, the only way to reset it is to physically reset the circuit breaker and initiate a new start sequence. Read/write.

Bit: 6  **Name:** Transitions Unsafe (TUF)
**Function:** Set when the RP04 detects the absence of write transitions during a write operation. Cleared by a Drive Clear or an INIT pulse.

Bit: 5  **Name:** Transitions Detector Failure (TDF)
**Function:** Set when the RP04 detects write transitions without the presence of a Write command. Cleared by a Drive Clear or an INIT pulse. Read/write.

Bit: 4  **Name:** Motor Sequence Error (MSE)
Function: Set if any of the following unsafe conditions are detected.

- SSR (Solid State Relay) failure
- power sequence failure
- brush in pack error

Cleared by successfully initiating a new start sequence. Read/write.

Bit: 3  Name: Current Switch Unsafe (CSU)
Function: Set when the RP04 detects an incorrect write current level during a write operation. Cleared by a Drive Clear or an INIT pulse. Read/write.

Bit: 2  Name: Write Select Unsafe (WSU)
Function: Set when the RP04 detects that both even-side and odd-size heads are simultaneously enabled for writing. Cleared by a Drive Clear or an INIT pulse. Read/write.

Bit: 1  Name: Current Sink Failure (CSF)
Function: Set when the RP04 detects the current sink nonoperative without the presence of a Write command. Cleared by a Drive Clear or an INIT pulse. Read/write.

Bit: 0  Name: Write Current Unsafe (WCU)
Function: Set when the RP04 detects the presence of write current without the presence of a Write command. Read/write.

Error Register 03 (RPER3) 776 742

<table>
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<td>PSU</td>
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</table>

Bit: 15  Name: Off Cylinder (OCYL)
Function: Set when an invalid off cylinder condition is detected resulting in a Seek Incomplete. Cleared by a Drive Clear or an INIT pulse. An off cylinder error will also cause an automatic recalibrate operation to occur. Read/write.

Bit: 14  Name: Seek Incomplete (SKI)
Function: Set when a seek operation fails to complete within 85ms from a seek initiation. Due to the positioner mal-
function, it is possible for the seek not to complete. The RP04 will assume a positioner hardware problem and will:

- set the SKI bit
- set the ATA bit
- reset the PIP bit
- set the RDY bit

This indicates to the software that the seek operation did not complete and the exact positioner location is unknown.

A SKI condition will cause the RP04 to determine that the drive is unsafe to operate and will cause the UNS (RPER1, bit 14) bit to set. The software can diagnose the trouble by monitoring the Error Register. Read/write.

**Bit: 6**  
**Name:** DC Low (DCL)  
**Function:** Set when the RP04 detects a loss of regulated 5Vdc power, which powers the interface electronics. Cleared by a Drive Clear or an INIT pulse. The detection of the DCL error condition will cause an automatic head retraction. Read/write.

**Bit: 5**  
**Name:** AC Low (ACL)  
**Function:** Set when the RP04 detects an interruption of primary ac power for the dc power supply which powers the interface electronics. Cleared by a Drive Clear or an INIT pulse. The detection of the ACL error condition will cause an automatic head retraction. Read/write.

**Bit: 3**  
**Name:** Any Unsafe Except Read/Write (UWR)  
**Function:** Set if any of the following unsafe conditions are detected (indicates a head retract has occurred):

- pack speed unsafe
- 30 Volt unsafe
- velocity unsafe
- servo unsafe
- ac unsafe
- dc unsafe

Cleared by a DC Clear or an INIT pulse. Read/write.

**Bit: 1**  
**Name:** Velocity Unsafe (VUF)
Function: Set when the RP04 detects an excessive positioner velocity. Cleared by a DC Clear or an INIT pulse. Read/write.

Bit: 0 Name: Pack Speed Unsafe (PSU)
Function: Set when the RP04 detects the pack speed to be below approximately 80% of normal while the heads are positioned within the pack area. Cleared by a Drive Clear or an INIT pulse. Read/write.

ECC Position Register (RPER1) 776 744

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<tr>
<td>00</td>
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<td>00</td>
<td>BLC 4096</td>
<td>BLC 2048</td>
<td>BLC 1024</td>
<td>BLC 512</td>
<td>BLC 256</td>
<td>BLC 128</td>
<td>BLC 64</td>
<td>BLC 32</td>
<td>BLC 16</td>
<td>BLC 8</td>
<td>BLC 4</td>
<td>BLC 2</td>
<td>BLC 01</td>
</tr>
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</table>

The RP04 has an ECC (Error Correction Code) capability which will generate, detect and correct an error by reconstructing a portion of the data. Within the specified code word length, which is fixed, the burst ECC code will correct an error which must fall within the specified length of the burst. The actual location of the burst within the code word (data field of a sector) is irrelevant.

Any errors outside the specified burst length will be detected but not corrected. The ECC hardware, in this case, will yield an ECC uncorrectable error. The RP04 logic contains the hardware to find the burst within which the read error is included and to determine the exact location of the burst within the data field.

The ECC Pattern Register contains the actual burst and the ECC Position Register contains the address for determining the actual location of the error burst within the data field.

**NOTE**
The actual correction of the data field is done by the software with the help of the ECC Position and ECC Pattern Registers.

The ECC Position Register contains the exact location of the error burst within the data field following the completion of the error correction procedure.

Upon completion of the ECC process, the device will load this register with the necessary information. The EXC line is raised upon initiation of the error correction procedure and the ATA bit is set at the trailing edge of EBL and EXC.
DISKS

RP04/05/06

ECC Pattern Register (RPEC2) 776 746

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<td>BIT</td>
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</table>

This register is used in conjunction with the ECC Position Register and contains the actual error burst available at the completion of the ECC internal to the RP04 device logic error correction process.

The software will use the contents of the ECC Position Register to find the actual location of the error burst in the data field. Then the error burst itself will determine the bits in error within the 11-bit field.

RJP04 SPECIFICATIONS

Main Specifications
- Storage medium: Disk pack (3336 type)
- Capacity/pack: 43,980,288 words
- Data transfer speed: 2.5usec/word
- Time for 1/2 revolution: 8.3msec
- Disk rotation speed: 3600 RPM
- Drives/control, maximum: 8

Track Positioning Time
- One cylinder seek: 7msec
- Average seek: 28msec

Data Organization
- Maximum seek (typ): 50msec
- Surfaces/pack: 19
- Tracks/surfaces: 411
- Sectors/track: 22
- Words/sector: 256
- Bits/words: 16
- Recording method: Modified Frequency Modulation (MFM)
- Recording density: 4040 bits/inch, max.
- Access with single read/write: 1 to 65,536 words
DISKS

UNIBUS Interface
Interrupt vector address 254
Priority level BR5
Data transfer NPR
Bus loading 1 bus load, each controller port

Mechanical
Mounting

Size
Weight 600 lbs
Cables

Disk: 1 free-standing unit
Control Unit: 2 systems unit
(mounts in a CPU or expander box)
40"H x 31"W or 32"D

Control-to-drive—25 ft standard, 40 ft optional
Drive-to-drive—2 ft standard, 10 ft optional
All cables, total—60 ft max.
RP04-H

DESCRIPTION
The RP04-H unit select switch is an eight-position, pull-to-turn octal coded rotary switch that mounts on a replacement control panel compatible with any RP04 disk drive. Each switch position (0-7) is displayed in the light-emitting diode (LED) unit number window. The unit select switch provides a reliable and convenient method for changing the RP04's physical drive address. Utilization of the switch is transparent to the disk controller; therefore all standard RP04 software can be used. The only software restrictions are: the unit select switch should not be changed while any transfer is in progress, and no two separate drives can have the same physical drive address.

SPECIFICATIONS
Panel Dimensions 2.7 in. × 19.81 in.
Rotary Switch Eight-position, 45° pull-to-turn action, stays between each position, three wafers, one pole per wafer. Gold plated contacts.

CSS
FEATURES:
- fast access—8.5 milliseconds average (10.2 milliseconds at 50 Hz)
- high-speed transfer rate—4 microseconds per word maximum (4.8 microseconds per word at 50 Hz)
- dual port control with programmable data port
- 256K (RJS03) or 512K (RJS04) words of storage per disk, expandable to over four million words
- real-time look-ahead on multidrive systems with interrupts on sector-compare for up to eight drives at the same time
- overlapped data transfer and look-ahead operations
- high data reliability

DESCRIPTION
The RJS03 and RJS04 fixed-head disk systems have been designed specifically for applications requiring fast, reliable, online storage. With an average access time of 8.5 milliseconds and a transfer rate of 4 microseconds per word, the RJS03 and RJS04 increase throughout substantially for timesharing applications that involve significant amounts of program swapping. Phase lock loop reading techniques and CRC (Cyclic Redundancy Check) error detection make these disk systems ideal for real-time data acquisition and control systems requiring a high level of reliability.
DISKS

RS03, RS04

The RJS03 includes a controller and a rack-mounted RS03 fixed-head disk drive with a storage capacity of 256K 16-bit words. The RJS04 includes a controller and an RS04 fixed-head disk drive with a storage capacity of 512K 16-bit words. The RJS03 and RJS04 are expandable by adding either RS03 and RS04 drives—up to a total of eight drives per controller. A single controller may have a mix of RS03 and RS04 drives. For instance, a requirement for 768K words of fixed-head disk storage can be met with a combination of an RJS03 and RS04 or an RJS04 and an RS03. Two drives may be mounted in a single cabinet.

The controller for the RJS03 and RJS04 requires two system unit mounting spaces in any PDP-11 CPU or in an H960-D or H960-E expansion box.

To minimize start-up current on multiple-drive systems, drives are automatically started in sequence when power is turned on.

The controller for both the RJS03 and RJS04 includes a large (66 word) data buffer. This data buffer maximizes configuration flexibility on large PDP-11 systems where there may be several high-speed DMA devices.

Operation
Data is stored in blocks of 64 words for the RS03 and in blocks of 128 words for the RS04. The RS03 uses one read/write head at a time; the RS04 uses two heads in parallel. There are 64 heads for the RS03 and 128 heads for the RS04. The higher capacity RS04 records information on both surfaces of the disk, whereas the RS03 uses only one surface. The number of sectors, 64, is the same, but the RS04 achieves double capacity by recording odd-numbered bits on one surface and even-numbered bits on the other surface.

Fast track-switching time permits spiral read/write from one track to the adjacent track in a single transfer operation. When the last sector on a track has been transferred, the disk automatically advances to the next track without any delay in the transfer rate. Up to 64K words can be transferred in a single operation.

The RJS03 and RJS04 also feature real-time look ahead. This feature permits the program to monitor the current angular position of the disk minimizing access time in a multidiive system when multiple requests are pending. Using interrupts when comparing sectors, program time can be kept to a minimum. Except for the drive currently engaged in a data transfer, all drives can perform searches simultaneously.
DISKS

RS03, RS04

Each disk drive has a set of six Write-Lock switches and a Write-Lockout Enable/Disable switch. The settings of the six Write-Lock switches correspond to the number of a track. When the Write-Lock Enable/Disable switch is enabled, all tracks numbered from 0 to the track number selected by the Write-Lock switches are write-protected.

Each controller has two UNIBUS ports. The first port can be used for data only. Data transmission can be switched from one port to the other under program control.

Reliability
The RJS03 and RJS04 offer a high level of data reliability. They have been designed to provide a recoverable error rate of less than 1 in 10**(2)11 bits read and a nonrecoverable error rate of less than 1 in 10**(2)12 bits transferred.

The use of a 16 bit Cyclic Redundancy Check (CRC) character per data block greatly reduces the probability of undetected error. To ensure maximum reliability in the transmission of information between disk drive and control, a differential bus is used with parity generated and checked at the drive and at the control for both control and data transfers.

A phase lock loop clock system and MFM recording offer the latest in reliable reading and recording techniques. In addition, a write-check capability is used to verify data written on any disk without modifying either the disk or the memory data and without the overhead of a programmed comparison between the original data in memory and the data written on the disk.

For maximum disk life and minimum down time, a prefilter and a high-efficiency air filter are used to keep the disk enclosure at a positive pressure. This air system maintains a clean room environment for the disk and heads.

REGISTERS

Control and Status 1 Register (RSCSI) 772 040

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<tr>
<th>15</th>
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<td>F1</td>
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<td>GO</td>
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</tbody>
</table>

LOCATED IN DRIVE

LOCATED IN CONTROLLER
### DISKS

**RS03, RS04**

<table>
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<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>Special Condition (SC)</td>
<td>Set by TRE or ATTN or I/O bus Control Parity Error. Cleared by UNIBUS A INIT, Controller Clear, or by removing the ATTN condition. Read only.</td>
</tr>
<tr>
<td>14</td>
<td>Transfer Error (TRE)</td>
<td>Set by DLT, WCE, UPE, NED, NEM, PGE, MXF, or MDPE or by a drive error during a data transfer. Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or by loading a data transfer command with GO set. Read/write.</td>
</tr>
<tr>
<td>13</td>
<td>MASSBUS I/O Control Bus Parity Error (MCPE)</td>
<td>Set by parity error on control bus while reading a remote register (located in the drive). Cleared by UNIBUS A INIT, Controller Clear, or Error Clear or by loading a data transfer command with a GO set. Parity errors which occur on the I/O control bus while writing a drive register are detected by the drive and cause the PAR error (RSER register, bit 3) to set. Read only.</td>
</tr>
<tr>
<td>12</td>
<td>Not used</td>
<td>Always read as a 0.</td>
</tr>
<tr>
<td>11</td>
<td>Drive Available (DVA)</td>
<td>Always a 1 in the RS04/RS03 when read from an existing drive. Read only.</td>
</tr>
<tr>
<td>10</td>
<td>Port Select (PSEL)</td>
<td>When PSEL = 1, data transfer is via UNIBUS B; when PSEL = 0, data transfer is via UNIBUS A. Cleared by UNIBUS A INIT, Controller Clear, or by writing a 0 in this bit position. Read/write.</td>
</tr>
<tr>
<td>9</td>
<td>UNIBUS Address Extension Bits (A17)</td>
<td>Cleared by UNIBUS A INIT, Controller Clear, or by writing zeros in these bit positions. Upper extension bits of the BA register. Read/write.</td>
</tr>
<tr>
<td>8</td>
<td>UNIBUS Address Extension Bits (A16)</td>
<td>Cleared by UNIBUS A INIT, Controller Clear, or by writing zeros in these bit positions. Upper extension bit of the BA register. Read/write.</td>
</tr>
<tr>
<td>7</td>
<td>Ready (RDY)</td>
<td></td>
</tr>
</tbody>
</table>

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**Function:** RDY normally = 1. During data transfers, RDY = 0. When a data transfer command code (51(sub)8-77(sub)8) is written into RSCS1, RDY is reset. At the termination of the data transfer, RDY is set. Read only.

**Bit: 6 Name:** Interrupt Enable (IE)

**Function:** IE is a control bit which can be set only under program control. When IE = 1, an interrupt may occur due to RDY or ATTN being asserted. Cleared by UNIBUS A INIT, Controller Clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.

**Bit: 5-0 Name:** F4-F0 and GO Bit

**Function:** F4-F0 are function (command) code control bits which determine the action to be performed.

<table>
<thead>
<tr>
<th>F4</th>
<th>F3</th>
<th>F2</th>
<th>F1</th>
<th>F0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No operation</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Drive Clear</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Search</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Write Check</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Write</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Read</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

The GO bit (RSCS1, bit 0) must be set to cause the controller or drive to respond to a command. The GO bit is reset by the drive after command execution.

The function code bits are stored in the selected drive. Cleared by UNIBUS A INIT or Controller Clear (will abort command execution in all drives). Read/write.

**Word Count Register (RSWC) 772 042**

<table>
<thead>
<tr>
<th>WC</th>
<th>WC</th>
<th>WC</th>
<th>WC</th>
<th>WC</th>
<th>WC</th>
<th>WC</th>
<th>WC</th>
<th>WC</th>
<th>WC</th>
<th>WC</th>
<th>WC</th>
<th>WC</th>
<th>WC</th>
<th>WC</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>09</td>
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<td>05</td>
<td>04</td>
<td>03</td>
<td>02</td>
<td>01</td>
</tr>
</tbody>
</table>

173
**Bit: 15-0  Name: Word Count (WC)**

**Function:** Set by the program to specify the number of words to be transferred (twos complement form). This register is cleared only by writing zeros into it. Incremented for each data transfer. Read/write.

**UNIBUS Address Register (RSBA) 772 044**

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
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<th>07</th>
<th>06</th>
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<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
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</thead>
<tbody>
<tr>
<td>BA</td>
<td>BA</td>
<td>BA</td>
<td>BA</td>
<td>BA</td>
<td>BA</td>
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<td>BA</td>
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<td>BA</td>
<td>BA</td>
</tr>
</tbody>
</table>

**Bit: 15-1  Name: UNIBUS Address (BA)**

**Function:** Loaded by the program to specify the starting memory address of a transfer. Cleared by UNIBUS A INIT or by Controller Clear. The BA register is incremented by 2 after each transfer of a word to or from memory. Read/write.

**Desired Address Register (RSDA) 772 046**

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
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<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>SP</td>
<td>SP</td>
<td>SP</td>
<td>SP</td>
<td>TA</td>
<td>TA</td>
<td>TA</td>
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<td>TA</td>
<td>TA</td>
<td>TA</td>
<td>TA</td>
</tr>
</tbody>
</table>

**Bit: 15-12  Name: Spare (SP)**

**Function:** If set when an operation is begun by setting the GO bit, an IAE error (RSER, bit 10) will be posted. Cleared by UNIBUS A INIT, Controller Clear, or by performing a Drive Clear function.

Spare bits for future expansion. The bits are incremented by a carry from the track address. Read/write.

**Bit: 11-6  Name: Track Addr (TR)**

**Function:** Set by the program to specify the track on which a transfer is to start. Cleared by UNIBUS A INIT, Controller Clear, or by performing a Drive Clear function. Incremented by the drive when a carry out of SA (bit 5) occurs. Read/write.

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**Bit: 5-0  Name:** Sector Addr (SA)  
**Function:** Set by the program to specify the sector on which a transfer is to start. Cleared by UNIBUS A INIT, Controller Clear, or performing a Drive Clear function. Incremented by the drive after each sector has been transferred. Read/write.

**Control and Status Register (RSCS2) 772 050**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>DLT</td>
<td>Data Late (DLT)</td>
</tr>
<tr>
<td>01</td>
<td>U2</td>
<td></td>
</tr>
<tr>
<td>02</td>
<td>U1</td>
<td></td>
</tr>
<tr>
<td>03</td>
<td>BAI</td>
<td></td>
</tr>
<tr>
<td>04</td>
<td>BA2</td>
<td></td>
</tr>
<tr>
<td>05</td>
<td>CLR</td>
<td></td>
</tr>
<tr>
<td>06</td>
<td>OR</td>
<td></td>
</tr>
<tr>
<td>07</td>
<td>IR</td>
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</tr>
<tr>
<td>08</td>
<td>MOPE</td>
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</tr>
<tr>
<td>09</td>
<td>MXF</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>PGE</td>
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</tr>
<tr>
<td>11</td>
<td>NEM</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>UED</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>WCE</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>UPE</td>
<td></td>
</tr>
</tbody>
</table>

**Bit: 15  Name:** Data Late (DLT)  
**Function:** Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write-check operation at the time the drive demands a transfer. Also set when the controller is performing a data transfer operation over the second UNIBUS (PSEL = 1) and a UNIBUS B INIT is received on that port. Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or by loading a data transfer command with GO set.

DLT causes TRE. A DLT error indicates a severely overloaded bus. Can also be set by the program reading or writing the RSDB register. Read only.

**Bit: 14  Name:** Write Check Error (WCE)  
**Function:** Set when the controller is performing a write-check operation and a word on the disk does not match the corresponding word in memory. Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or by loading a data transfer command with GO set.

WCE causes TRE. If a mismatch is detected during a write-check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RSBA [and extension is the address of the word following the one which did not match (if BAI is not let)]. The mismatch data word from the disk is displayed in the data buffer (RSDB). Read only.

**Bit: 13  Name:** Parity Error (PE)
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Function: Set if the parity lines indicate a parity error while the controller is performing a write or write-check command. Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or by loading a data transfer command with GO set.

PE causes TRE. When the UNIBUS is selected to do 18 bit data transfers, the PE error is disabled. When a parity error occurs, the RSBA register contains the address +2 of the memory word with the parity error (if BAI is not set). This bit may be set by program control for diagnostic purposes. Read/write.

Bit: 12 Name: Non-Existent Drive (NED)

Function: Set when the program reads or writes a drive register (CS1, DA, DS, ER, LA, MR, or DT) in a drive (selected by U 2-0) which does not exist or is powered down (if the drive fails to assert TRA within 1.5 μsec after assertion of DEM). Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or by loading a data transfer command with GO set. NED causes TRE. Read only.

Bit: 11 Name: Non-Existent Memory (NEM)

Function: Set when the controller is performing a DMA transfer and the memory address specified in RSBA is non-existent (does not respond to MSYN within 10 μsec). Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or by loading a data transfer command with GO set. NEM causes TRE. The RSBA contains the address +2 of the memory location causing the error. Read only.

Bit: 10 Name: Program Error (PGE)

Function: Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. Cleared by UNIBUS A INIT, Controller Clear, or by loading a data transfer command with GO set.

PGE causes TRE. The data transfer command code is inhibited from being written. Read only.

Bit: 9 Name: Miss Transfer (MXF)

Function: Set if the drive does not respond to a data transfer command within 250 μsec. Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or by loading a data transfer command with GO set.

MXF causes TRE. This bit can be set or cleared by the
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program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive which has ERR set, or if the drive fails to initiate the command for any reason (such as a parity error). Read/write.

Bit: 8  Name: MASSBUS I/O Data Bus Parity Error (MDPE)
Function: Set when a parity error occurs on the MASSBUS data while doing a read or write-check operation. Cleared by UNIBUS A INIT, Controller Clear, Error Clear, or by loading a data transfer command with GO set.
MDPE causes TRE. Parity errors on the I/O bus data bus during write operations are detected by the drive and cause the PAR error. Read only.

Bit: 7  Name: Output Ready (OR)
Function: Set when a word is present in RSDB and can be read by the program. Cleared by UNIBUS A INIT, Controller Clear, or by reading DB.
Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to read the DB register before OR is asserted will cause a DLT error. Read only.

Bit: 6  Name: Input Ready (IR)
Function: Set when a word may be written in the DB register by the program. Cleared by reading the DB.
Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to write the DB register before IR is asserted will cause a DLT error. Read only.

Bit: 5  Name: Controller CLEar (CLR)
Function: When a 1 is written into this bit, the controller and all drives are initialized. UNIBUS A INIT also causes Controller Clear to occur. Write only.

Bit: 4  Name: Parity Test (PAT)
Function: While PAT is set, the controller generates even parity on both the control bus and data bus of the I/O bus. When clear, odd parity is generated. Cleared by UNIBUS A INIT or Controller Clear. While PAT is set, the controller checks for even parity received on the data bus but not on the control bus. Read/write.

Bit: 3  Name: UNIBUS Address Increment Inhibit (BAI)
Function: When BAI is set, the controller will not increment the BA register during a data transfer. This bit cannot be
modified while the controller is doing a data transfer (RDY negated). Cleared by UNIBUS A INIT or Controller Clear. When set during a data transfer, all data words are read from or written into the same memory location. Read/write.

**Bit: 2-0**  **Name:** Unit Select (U 2-0)

**Function:** These bits are written by the program to select a drive. Cleared by UNIBUS A INIT or Controller Clear.

The unit select bits can be changed by the program during data transfer operations without interfacing with the transfer. The CS1, DA, DS, ER, LA, MR, and DT registers contain bits which come from the selected drive. Read/write.

**Drive Status Register (RSDS) 772 052**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
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<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td></td>
</tr>
</tbody>
</table>

**Bit: 15**  **Name:** Attention Active (ATA)

**Function:** Set by the drive when there is an Attention condition in that drive. Cleared by UNIBUS A INIT, Controller Clear, loading a command with the GO bit set, or loading a 1 in the RSAS register in the bit position corresponding to the drives' unit numbers. (The last two methods of clearing the ATA bit will not clear the error indicators in the drive.)

An Attention condition occurs at the completion of a Search command, at the completion of a data transfer in which the drive detected an error, if an error condition occurs while the drive is not performing a command, and if there is any change in status of MOL. When the ATA bit of any drive is set, the ATTN line is asserted. Read only.

**Bit: 14**  **Name:** Error Summary (ERR)

**Function:** Set when one or more of the error bits is set in the RSER register of the selected drive. Cleared by UNIBUS A INIT, Controller Clear, or Drive Clear.

This bit is the logical OR of all the bits in the RSER register. This bit is not cleared by loading a command other than Drive Clear. While ERR is asserted, com-
mands other than Drive Clear are not accepted by the drive. Read only.

**Bit: 13**  
**Name:** Positioning in Progress (PIP)  
**Function:** Set by the drive while a Search command is underway; cleared at the completion of the search operation. Read only.

**Bit: 12**  
**Name:** Medium On Line (MOL)  
**Function:** Set by the drive when the drive is up to speed and power is within limits. Cleared when the drive is powered down and during power-up sequencing. Read only.

**Bit: 11**  
**Name:** Write Locked (WRL)  
**Function:** Set by the drive when the address in the RSDA register is among those which are write protected (and the write lock switch is in the enable position). Cleared by loading RSDA with an address which is not write protected. Read only.

**Bit: 10**  
**Name:** Last Block Transferred (LBT)  
**Function:** Set by the drive at the end of the data transfer to the highest address sector. Cleared by UNIBUS A INIT, Controller Clear, loading a new address in the RSDA register, or performing a Drive Clear function. Read only.

**Bit: 9**  
**Name:** Not used  
**Function:** Always read as a 0.

**Bit: 8**  
**Name:** Drive Present (DPR)  
**Function:** Always read as a 1. This bit is for use in dual-controller configurations. Read only.

**Bit: 7**  
**Name:** Drive Ready (DRY)  
**Function:** Set whenever the drive is on-line and prepared to accept a command. Cleared whenever a valid command (with GO set) is loaded into RSCS1. Read only.

**Bit: 6-0**  
**Name:** Not used  
**Function:** Always a 0.

**Error Register (RSER)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>OCK</td>
</tr>
<tr>
<td>14</td>
<td>UNS</td>
</tr>
<tr>
<td>13</td>
<td>DPI</td>
</tr>
<tr>
<td>12</td>
<td>DTE</td>
</tr>
<tr>
<td>11</td>
<td>WLE</td>
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<td>1</td>
<td>ILR</td>
</tr>
<tr>
<td>0</td>
<td>ILF</td>
</tr>
</tbody>
</table>
Bit: 15  Name: Data2Check (DCK)  
Function: Set by the drive when an error in the cyclic redundancy check is detected during a read or write-check operation. Cleared by UNIBUS A INIT, Controller Clear, or Drive Clear. Read/write.

Bit: 14  Name: Unsafe (UNS)  
Function: Set by the drive upon detection of low power; cleared upon restoration of power.

If a transfer is in progress when ac power loss occurs in the drive, the transfer is aborted. ATTN is asserted by this drive for as long as dc power lasts, whether or not a transfer was in progress. Read/write.

Bit: 13  Name: Operation Incomplete (OPI)  
Function: Set when the drive fails to complete an operation within the expected time. Cleared by UNIBUS A INIT, Controller Clear, or Drive Clear.

A data transfer operation is considered incomplete if the RUN line is not asserted within two disk revolutions after a data transfer command was loaded. This would indicate a failure. A Search command is considered incomplete if not terminated within two disk revolutions; this would indicate a drive failure. Read/write.

Bit: 12  Name: Drive Timing Error (DTE)  
Function: Set by the drive when it detects timing fault (loss of clock or index pulse, dropping or picking up clock pulses). Cleared by UNIBUS A INIT, Controller Clear, or Drive Clear. Read/write.

Bit: 11  Name: Write Lock Error (WLE)  
Function: Set by the drive when a write function is attempted at an address which is write protected. Cleared by UNIBUS A INIT, Controller Clear, Drive Clear. Read/write.

Bit: 10  Name: Invalid Address Error (IAE)  
Function: Set by the drive when a data transfer or Search command is loaded while an invalid address is in the RSDA (desired address) register. Cleared by UNIBUS A INIT, Controller Clear, or Drive Clear. In the RS04/RS03, an invalid address is one which is larger than the maximum address. Read/write.
Bit: 9  Name: Address Overflow (AO)
Function: Set by the drive when the controller attempts to con-
tinue to transfer data after the last sector on the last
track has been written or read. Cleared by UNIBUS A
INIT, Controller Clear, or Drive Clear. When this error
occurs, no further data transfer can occur. The RSDA
register contains an invalid address. Read/write.

Bit: 3  Name: Bus Parity Error (PAR)
Function: Set when incorrect parity is detected by the drive dur-
ing a register write operation or on a data transfer
during a write operation. Cleared by UNIBUS A INIT,
Controller Clear, or Drive Clear. If a control bus parity
error is detected when writing into any drive register,
that register will not be modified. Read/write.

Bit: 2  Name: Register Modify Refused (RMR)
Function: Set by the drive when an attempt is made by the pro-
gram to write into the RSDA, RSER, or RSCS1 regis-
ters, while the drive is busy (DRY bit is negated).
Cleared by UNIBUS A INIT, Controller Clear, or Drive
Clear. Drive operation can be aborted by program con-
trol only by performing Controller Clear or Reset.
These must be used with caution due to their effects
on other devices. Read/write.

Bit: 1  Name: Illegal Register (ILR)
Function: Set by the drive when the program attempts to read or
write a drive register whose address is not recognized
by the drive. Cleared by UNIBUS A INIT, Controller
Clear, or Drive Clear. Indicates a hardware failure in
the controller or drive address logic. Read/write.

Bit: 0  Name: Illegal Function (ILR)
Function: Set by the drive when the GO bit is set and the core in
the Function Register (RSCS1, bits 5-1) is not an im-
plemented code. Cleared by UNIBUS A INIT, Controller
Clear, or Drive Clear. Read/write.

Attention Summary Register (RSAS) 772 056

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
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<td>ATA</td>
<td>01</td>
<td>ATA</td>
<td>00</td>
</tr>
</tbody>
</table>

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Bit: 7-0  **Name:** Attention Active (ATA)
**Function:** Each bit sets when the corresponding drive asserts its ATA bit. All bits are cleared by UNIBUS A INIT or Controller Clear. Individual bits are cleared by loading a function code with the GO bit in the corresponding drive or by writing a 1 in the ATA bit positions of this register. Writing a 0 has no effect.

Each drive's ATA bit is displayed individually in bit 15 of RSDS. Each drive responds in the bit position which corresponds to its unit number; e.g., drive 2 responds in bit position 2. Read/write.

**Look-Ahead Register (RSLA) 772 060**

<table>
<thead>
<tr>
<th>Bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>03</td>
<td>03</td>
<td>03</td>
<td>03</td>
<td>03</td>
<td>03</td>
<td>03</td>
<td>03</td>
<td>03</td>
<td>03</td>
<td>03</td>
<td>03</td>
<td>00</td>
</tr>
</tbody>
</table>

**Bit:** 11-6  **Name:** Current Sector Addr (CS)
**Function:** Indicates the sector address currently under the read/write heads of the drive whose unit number appears in RSCS2 (2:0). Read only.

**Bit:** 5-0  **Name:** Sector Fract (SF)
**Function:** Indicates the fraction of the current sector which has passed the read/write heads in one 64th of a sector. Read only.

**Data Buffer Register (RSDB) 772 062**

<table>
<thead>
<tr>
<th>Bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
<td>DB</td>
</tr>
</tbody>
</table>

**Bit:** 15-0  **Name:** Data Buffer (DB)
**Function:** When read, the contents of OBUF (internal register) are delivered. Upon completion of the read, the next sequential word in the Silo will be clocked into OBUF. When written, data is loaded into IBUF (internal register) and allowed to sequence into the Silo if space is available. Used by the program for diagnostic purposes. Read/write.
DISKS

RS03, RS04

Maintenance Register (RSMR) 772 064—The Maintenance register is a 16-bit register which simulates various signals from the disk to allow diagnostic testing of the drive logic circuits.

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLK</td>
<td>MRDT</td>
<td>CRCW</td>
<td>MWDB</td>
<td>SB</td>
<td>LSR</td>
<td>AC</td>
<td>SP</td>
<td>WRT</td>
<td>RD</td>
<td>MRDT</td>
<td>MIND</td>
<td>MCLK</td>
<td>MRDS</td>
<td>O</td>
<td>DMO</td>
</tr>
</tbody>
</table>

*Located in the encode/decode logic.

Drive Type Register (RSDT) 772 066

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>NSA</td>
<td>TAP</td>
<td>MOH</td>
<td>7CH</td>
<td>ORQ</td>
<td>SPR</td>
<td>O</td>
<td>DT</td>
<td>DT</td>
<td>DT</td>
<td>DT</td>
<td>DT</td>
<td>DT</td>
<td>DT</td>
<td>DT</td>
<td>DT</td>
</tr>
</tbody>
</table>

Bit: 15-9

Function: Always 0 in RS04/RS03.

Bit: 8-0

Name: Drive Type (DT)

Function: These bits contain a unique number for each drive type. The following drive type numbers are assigned to RS04/RS03.

- 000<sub>8</sub> RS03
- 001<sub>8</sub> RS03 with sector interleave
- 002<sub>8</sub> RS04
- 003<sub>8</sub> RS04 with sector interleave

Read only.

SPECIFICATIONS
(RJS04 is the same except where noted)

Main Specifications

<table>
<thead>
<tr>
<th>Storage medium</th>
<th>Fixed-head disk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity/disk</td>
<td>RJS03: 262,144 words (256K)</td>
</tr>
<tr>
<td></td>
<td>RJS04: 512K words</td>
</tr>
<tr>
<td>Data transfer speed</td>
<td>RJS03: 4 or 8μsec/word (4.8 or 9.6μsec/word at 50 Hz)</td>
</tr>
<tr>
<td></td>
<td>RJS04: 4μsec/word (4.8μsec/word at 50 Hz)</td>
</tr>
</tbody>
</table>
### DISKS

#### RS03, RS04

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average access time (1/2 rev)</td>
<td>8.5 msec (10.2 msec at 50 Hz)</td>
</tr>
<tr>
<td>Minimum access time</td>
<td>6.4 μsec (7.7 μsec at 50 Hz)</td>
</tr>
<tr>
<td>Disk rotation speed</td>
<td>3530 RPM (2940 RPM at 50 Hz)</td>
</tr>
<tr>
<td>Controller data buffer size</td>
<td>66 words</td>
</tr>
<tr>
<td>Disk/control, max</td>
<td>8</td>
</tr>
</tbody>
</table>

#### Data Organization

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tracks</td>
<td>64</td>
</tr>
<tr>
<td>Sectors/tracks</td>
<td>64</td>
</tr>
<tr>
<td>Words/sector</td>
<td>RJS03: 64</td>
</tr>
<tr>
<td></td>
<td>RJS04: 128</td>
</tr>
<tr>
<td>Bits/word</td>
<td>16</td>
</tr>
<tr>
<td>Recording method</td>
<td>MFM (modified frequency modulation)</td>
</tr>
<tr>
<td>Recording density</td>
<td>2200 bits/inch, maximum</td>
</tr>
<tr>
<td>Spare Tracks</td>
<td>RJS03: 1 timing +4 data</td>
</tr>
<tr>
<td></td>
<td>RJS04: 1 timing +8 data</td>
</tr>
</tbody>
</table>

#### Register Addresses

<table>
<thead>
<tr>
<th>Specification</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control/status 1</td>
<td>(RSCS1) 772 040</td>
</tr>
<tr>
<td>Word count</td>
<td>(RSWC) 772 042</td>
</tr>
<tr>
<td>UNIBUS address</td>
<td>(RSBA) 772 044</td>
</tr>
<tr>
<td>Desired block address</td>
<td>(RSDA) 772 046</td>
</tr>
<tr>
<td>Control/status 2</td>
<td>(RSCS2) 772 050</td>
</tr>
<tr>
<td>Drive status</td>
<td>(RSDS) 772 052</td>
</tr>
<tr>
<td>Error</td>
<td>(RSER) 772 054</td>
</tr>
<tr>
<td>Attention summary</td>
<td>(RSAS) 772 056</td>
</tr>
<tr>
<td>Look-ahead</td>
<td>(RSLA) 772 060</td>
</tr>
<tr>
<td>Data buffer</td>
<td>(RSDB) 772 062</td>
</tr>
<tr>
<td>Maintenance</td>
<td>(RSMR) 772 064</td>
</tr>
<tr>
<td>Drive type</td>
<td>(RSDT) 772 066</td>
</tr>
</tbody>
</table>

#### UNIBUS Interface

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt vector address</td>
<td>204</td>
</tr>
<tr>
<td>Priority level</td>
<td>BR5</td>
</tr>
<tr>
<td>Data transfer</td>
<td>NPR</td>
</tr>
<tr>
<td>Number of ports</td>
<td>2</td>
</tr>
<tr>
<td>Bus loading</td>
<td>1 bus load, each controller port</td>
</tr>
</tbody>
</table>
DISKS

RS03, RS04

Mechanical

Mounting

Disk drive mounts in a standard PDP-11 cabinet (supplied); controller is 2 system units, mounting assembly is not supplied

Size

15-3/4-inch front panel height for disk drive

Weight (cab and 1 drive)

350 lbs.

Weight (drive only)

120 lbs (RS04), 110 lbs (RS03)

Power Requirements

Drive

DC

None

AC

90-132 Vac, 60±1 Hz or 50±1 Hz; 180-264 Vac, 60±1 Hz or 50±1 Hz

Starting current

13 A max at 115 Vac; 6.5 A max at 230 Vac for 25 sec max

Running current

6 A max at 115 Vac; 3 A max at 230 Vac

Dissipation

350 Watts

Controller

DC

16 A at +5V; 0.6 A at −15V

AC

None

Environment

Relative humidity: 10% to 90% Max. 0% to 90% Max.

Operating

Wet Bulb 28°C

10°C to 40°C

Min. dew point 2°C

Altitude: 8,000 ft. 30,000 ft.

Models

RJS03-BA: Disk drive and control, 256K words, 115 Vac, 60 Hz
RJS03-BD: Disk drive and control, 256K words, 230 Vac, 50 Hz
RJS04-BA: Disk drive and control, 512K words, 115 Vac, 60 Hz
RJS04-BD: Disk drive and control, 512K words, 230 Vac, 50 Hz
RS03-AA: Add-on disk, 256K words, 115 Vac, 60 Hz
RS03-AD: Add-on disk, 256K words, 230 Vac, 50 Hz
RS04-AA: Add-on disk, 512K words, 115 Vac, 60 Hz
RS04-AD: Add-on disk, 512 words, 230 Vac, 50 Hz
FEATURES

- high reliability
- industry compatibility
- ease of maintenance
- simple operation
- use as an I/O device or a random-access file device
- low-cost, compact, removable diskettes
- 256,256 bytes of data storage capacity per diskette
- average access time of 483 milliseconds
- head loaded only when reading or writing
- extensive operating system and diagnostic software support

DESCRIPTION

The RX01 Floppy Disk, RX11 Floppy Disk System, is a highly reliable, low-cost, mass storage subsystem, capable of storing up to 256,256 8-bit bytes per drive in an industry-compatible format. It provides a compact data interchange and software description medium for critical I/O applications. In addition, the RX11's random-access capability allows configuring very low-cost, disk-based systems with small PDP-11 processors. Such systems can
satisfy the needs of applications that could never before afford random access storage.

The RX11 Floppy Disk System consists of an RX01 Floppy Disk drive unit and a PDP-11 quad interface module requiring a single SPC slot. The RX01 includes either one or two drives, a micro-programmed controller module, and a read/write electronics module. These are housed in a 10 1/2 inch, rack-mountable chassis. Up to two drives can be supported by each controller for a total storage capacity of 512,512 bytes.

Given an absolute sector address, the RX01 locates the desired sector and performs the indicated function. It automatically verifies head position and generates and verifies the Cyclic Redundancy Check (CRC) character.

Track-to-track moves require ten milliseconds for the move plus twenty milliseconds for settling time if the head is loaded for a read or write. The rotational speed of the diskette is 360 rpm, which results in an average latency time of 83 milliseconds. The track-to-track move, head settling, and latency time produce an average access time of 483 milliseconds. During a sequential access, the whole diskette can be read in about thirty seconds.

THE MEDIA
The RX01 Floppy Disk uses the industry-standard "diskette" or "floppy" media. These are thin, flexible, oxide-coated disks similar in size to a 45-rpm phonograph record. The disk is recorded on one side only and is permanently contained in an 8-inch square, flexible envelope.

The envelope has a large center hole for the drive spindle, a small hole for track index sensing, and a large slit for the read/write. A solenoid contact load pad is located on the opposite side of the envelope. The inside of the envelope is covered with a soft material designed to wipe the disk surface clean just before reading.

The diskette contains 77 tracks and 26 sectors per track. Each sector can store 128 8-bit bytes for a total formatted capacity of 256,256 8-bit bytes.

The diskette is an ideal storage, interchange, and software distribution medium. Compared to disk cartridges or disk packs, it is very inexpensive. Because it is flat and thin, the diskette is compact, enabling large amounts of data to be stored conveniently
in a small space. Diskettes can be easily transported in a briefcase or a manila envelope.

Because the diskette is preformatted in the industry standard, it insures industry compatibility and drive-to-drive interchangeability. The RX01 can read diskettes written on other standard floppy disk equipment and vice versa. Preformatted diskettes also reduce hardware costs by eliminating the circuitry required to generate the correct format.

Reliability
The RX01 provides exceptional reliability as well as low cost. The simple mechanical construction of the drive and the use of a microprogrammed controller that reduces hardware complexity contribute to the design goal MTBF (Mean Time Between Failures) of 5000 hours. To enhance disk life, the head contacts the disk only during reading or writing. With the head loaded on a given track, the media can withstand one million passes.

The RX01 performs parity checks and provides error indications. Each sector has a cyclic redundancy check (CRC) character as part of the header field and another CRC character as part of the data field. The RX01 generates and verifies the CRC characters and provides error indications.

Operation
The RX01 Floppy Disk drive unit is simple to operate. When the door is opened, the diskette, properly oriented, can be inserted. When the door is closed, the diskette is engaged on the registration hub. Once the diskette drive attains operating speed, the software takes over. The diskette removal procedure is the reverse of the insertion procedure. Elimination of any other operator controls greatly simplifies operation.

REGISTERS

Command and Status Register (RXCS) 777 170
Loading this register while the RX01 is not busy and with bit 0 = 1 will initiate a function as described below. Bits 0 – 4 are write-only bits.
BIT       DESCRIPTION
Bit: 15   Name: Error
Function: This bit is set by the RX01 to indicate that an error has
          occurred during an attempt to execute a command. This bit is cleared
          by the initiation of a new command or an Initialize. Read only.
Bit: 14   Name: RX11 Initialize
Function: This bit is set by the program to initialize the RX11
          without initializing all of the devices on the UNIBUS. Write only.
          CAUTION: Loading the lower byte of the RXCS will also
          load the upper byte of the RXCS.
          Upon setting this bit in the RXCS, the RX11 will negate
          Done and move the head position mechanism of drive 1 (if two are available) to track 0. Upon completion of a
          successful Initialize, the RX01 will zero the Error and Status register, set Initialize Done and set RXES bit 7
          (DRV RDY) if unit 0 is ready. It will also read sector 1
          of track 1 on drive 0.
Bit: 8-13  Name:
Function: Unused
Bit: 7    Name: Transfer Request
Function: This bit signifies that the RX11 needs data or has data
          available. Read only.
Bit: 6    Name: Interrupt Enable
Function: This bit is set by the program to enable an interrupt
          when the RX01 has completed an operation (Done). The
          condition of this bit is normally determined at the time
          a function is initiated. This bit is cleared by Initialize.
          Read/write.
Bit: 5    Name: Done
Function: This bit indicates the completion of a function. Done
          will generate an interrupt when asserted if Interrupt
          Enable (RXCS bit 6) is set. Read only.
Bit: 4    Name: Unit Select
Function: This bit selects one of the two possible disks for execu-
          tion of the desired function. Write only.
Bit: 1-3  Name: Function Select
**DISKS**

**RX01**

**Function:** These bits code one of the eight possible functions. These are write-only bits.

<table>
<thead>
<tr>
<th>Code</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>Fill Buffer</td>
</tr>
<tr>
<td>001</td>
<td>Empty Buffer</td>
</tr>
<tr>
<td>010</td>
<td>Write Sector</td>
</tr>
<tr>
<td>011</td>
<td>Read Sector</td>
</tr>
<tr>
<td>100</td>
<td>Not used</td>
</tr>
<tr>
<td>101</td>
<td>Read Status</td>
</tr>
<tr>
<td>110</td>
<td>Write Deleted Data Sector</td>
</tr>
<tr>
<td>111</td>
<td>Read Error Register</td>
</tr>
</tbody>
</table>

**Bit: 0**  **Name:** Go

**Function:** Initiates a command to the RX01. Write only.

**Data Buffer Register (RXDB) 777 172**

This register serves as a general purpose data path between the RX01 registers according to the protocol of the function in progress.

This register is read/write if the RX01 is not in the process of executing a command; it may be manipulated without affecting the RX01 subsystem. If the RX01 is actively executing a command, this register will accept data only if RXCS bit 7 (TR) is set. In addition, valid data can be read only when TR is set.

**CAUTION:** Violation of protocol in manipulating this register may cause permanent data loss.

**RXTA—RX Track Address**—This register is loaded to indicate on which of the $114_8$ tracks a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.

```
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
```

**RXSA—RX Sector Address**—This register is loaded to indicate on which of the $32_8$ sectors a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.
RX Data Buffer (RXDB)
All information transferred to and from the floppy media passes through this register and is addressable only under the protocol of the function in progress.

RX Error and Status (RXES)
This register contains the current error and status conditions of the drive selected by bit 4 (Unit Select) of the RXCS. This read-only register can be addressed only under the protocol of the function in progress. The RXES is located in the RXDB upon completion of a function.

BIT
Bit: 7  Name: Drive Ready
Function: This bit is asserted: if the unit currently selected exists, is properly supplied with power, has a diskette installed correctly, has its door closed, and has a diskette up to speed.

NOTE
The Drive Ready bit is only valid when retrieved via a Read Status function or at completion of Initialize when it indicates status of drive 0.
If the Error bit was set in the RXCS but Error bits are not set in the RXES, then specific error conditions can be accessed via a Read Error Register function.
Bit: 6  Name: Deleted Data Detected
Function: During data recovery, the identification mark preceding the data field was decoded as a deleted data mark.

Bit: 3-5  Name: Unused

Bit: 2  Name: Initialize Done
Function: This bit is asserted in the RXES to indicate completion of the Initialize routine which can be caused by RX01 power failure, system power failure, or programmable or UNIBUS Initialize.

Bit: 1  Name: Parity Error
Function: A parity error was detected on command or address information being transferred to the RX01 from the UNIBUS interface. A parity error indication means that there is a problem in the interface cable between the RX01 and the interface. Upon detection of a parity error, the current function is terminated, the RXES is moved to the RXDB, and Error and Done are asserted.

Bit: 0  Name: CRC Error
Function: A cyclic redundancy check error was detected as information was retrieved from a data field of the diskette. The RXES is moved to the RXDB, and Error and Done are asserted.

SPECIFICATIONS

Main Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage medium</td>
<td>Preformatted diskette</td>
</tr>
<tr>
<td></td>
<td>(industry-compatible)</td>
</tr>
<tr>
<td>Capacity per diskette</td>
<td>256, 256 8-bit bytes</td>
</tr>
<tr>
<td>Data Transfer speed</td>
<td>18μsec per byte</td>
</tr>
<tr>
<td>Time for half revolution</td>
<td>83 msec</td>
</tr>
<tr>
<td>Diskette rotation speed</td>
<td>360 rpm</td>
</tr>
<tr>
<td>Drives per control</td>
<td>2 (maximum)</td>
</tr>
</tbody>
</table>

**Track Positioning Time**

<table>
<thead>
<tr>
<th>Time</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>One track move</td>
<td>10 msec</td>
</tr>
<tr>
<td>Average track seek</td>
<td>380 msec</td>
</tr>
<tr>
<td>Maximum track seek</td>
<td>760 msec</td>
</tr>
</tbody>
</table>
**DISKS**

**RX01**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Head settling</td>
<td>20 msec</td>
</tr>
<tr>
<td>Average access time</td>
<td>483 msec</td>
</tr>
<tr>
<td><strong>Data Organization</strong></td>
<td></td>
</tr>
<tr>
<td>Surfaces per diskette</td>
<td>1</td>
</tr>
<tr>
<td>Tracks</td>
<td>77</td>
</tr>
<tr>
<td>Sectors</td>
<td>26</td>
</tr>
<tr>
<td>Capacity per sector</td>
<td>128 8-bit bytes</td>
</tr>
<tr>
<td>Recording method</td>
<td>Double frequency</td>
</tr>
<tr>
<td>Recording density</td>
<td>3200 bits per inch maximum</td>
</tr>
<tr>
<td><strong>Register Addresses</strong></td>
<td></td>
</tr>
<tr>
<td>Command status</td>
<td>(RXCS) 777 170</td>
</tr>
<tr>
<td>Data buffer</td>
<td>777 172</td>
</tr>
<tr>
<td><strong>UNIBUS Interface</strong></td>
<td></td>
</tr>
<tr>
<td>Interrupt vector address</td>
<td>264</td>
</tr>
<tr>
<td>Priority level</td>
<td>Normally BR5</td>
</tr>
<tr>
<td>Data transfer</td>
<td>Programmed I/O</td>
</tr>
<tr>
<td>Bus loading</td>
<td>2 bus loads</td>
</tr>
<tr>
<td><strong>Mechanical</strong></td>
<td></td>
</tr>
<tr>
<td>Mounting</td>
<td>RX01 mounts in a standard PDP-11 cabinet. Interface requires one SPC slot.</td>
</tr>
<tr>
<td>Size</td>
<td>10 1/2 inch front panel height +1 SPC</td>
</tr>
<tr>
<td>Weight</td>
<td>60 lb (dual drive)</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td></td>
</tr>
<tr>
<td>Running current</td>
<td>5A maximum at 115V, 60 Hz (dual drive); 2.5A maximum at 230V, 50 Hz (dual drive)</td>
</tr>
<tr>
<td>Interface current</td>
<td>1.5A maximum at +5 Vdc</td>
</tr>
<tr>
<td>Heat dissipation</td>
<td>500 watts maximum (dual drive)</td>
</tr>
<tr>
<td><strong>Environmental</strong></td>
<td></td>
</tr>
<tr>
<td>Temperature</td>
<td>15°C (59°F) to 32°C (90°F) with a maximum temperature gradient of 20°F per hour or 11°C per hour</td>
</tr>
<tr>
<td>Relative humidity</td>
<td>20% to 80% with a maximum wet bulb of 25°C (77°F) and a minimum dew point of 2°C (36°F).</td>
</tr>
</tbody>
</table>
### DISKS

**RX01**

**RX11**

<table>
<thead>
<tr>
<th>Models</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX11-AA</td>
<td>Single-drive system, 115Vac, 60 Hz</td>
</tr>
<tr>
<td>RX11-AD</td>
<td>Single-drive system, 230 Vac, 50 Hz</td>
</tr>
<tr>
<td>RX11-BA</td>
<td>Dual-drive system, 115Vac, 60 Hz</td>
</tr>
<tr>
<td>RX11-BD</td>
<td>Dual-drive system, 230 Vac, 50 Hz</td>
</tr>
</tbody>
</table>
FEATURES

- double density floppy with single density selectable mode
- 512,512 bytes of data storage capacity per diskette in double density mode
- direct memory access for transferring data
- baseline RX01 industry compatibility through single density mode
- greater ease of maintenance
- high reliability
- simple operation
- identical form factor to RX01
- use as an I/O device or a random-access file device
- microprocessor-based controller
- low-cost, compact, removable diskettes
- retains field-proven RX01 cooling
- average access time of 262 milliseconds
- head loaded only when reading, writing, or seeking
- extensive operating system and diagnostic software support
- power fail indication
- improved error reporting ability
- soft write protect
DISKS

RX02

DESCRIPTION
The RX02 Floppy Disk System is a highly reliable, low cost, mass storage subsystem, capable of storing up to 512,512 bytes one each of two diskette drives in the double density mode. Baseline RX01 and industry-compatible format is provided through the single density mode which has a storage capacity of 256,256 bytes. Data is transferred using Direct Memory Access. This allows for quicker data transfer as well as more efficient utilization of the host processor. The RX02 provides a compact data interchange and software distribution medium for critical I/O applications. In addition the RX02 random-access capability allows configuration of very low-cost, disk-based systems with small PDP-11 processors. Such systems can satisfy the needs of applications that have outgrown the 256K bytes capacity of the RX01.

The RX021-series floppy disk System consists of an RX02 floppy disk drive unit and a PDP-11 quad interface module which requires a single SPC slot. The RX02 includes two drives, a microprogrammed controller module, and a read/write electronics module, all housed in a 10 1/2 inch, rack-mountable chassis. Two drives furnished with each controller provide a total storage capacity of up to 1,025,025 bytes.

Given an absolute sector address, the RX02 locates the desired sector and performs the indicated function. It automatically verifies head position and generates and verifies the cyclic redundancy check (CRC) character.

Track-to-track moves require six milliseconds for the move plus twenty-five milliseconds for settling time if the head is loaded for a read or write. The rotational speed of the diskette is 360 rpm, which results in an average latency time of 83 milliseconds. The track-to-track move, head settling, and latency time produce average access time to data of 262 seconds. During a sequential access, the whole diskette can be read in about thirty seconds.

THE MEDIA
The RX02 Floppy Disk uses the RX01K industry-standard diskette or floppy media, which are thin, flexible, oxide-coated disks similar in size to a 45-rpm phonograph record. This disk is recorded on one side only and is permanently contained in an 8-inch square, flexible envelope.

The envelope has a large center hole for the drive spindle, a small hole for track index sensing, and a large slit for the read/write head. A solenoid contact load pad is located on the opposite side of the envelope. The inside of the envelope is covered with a soft
DISKS

RX02

material, designed to wipe the disk surface clean just before reading.

The diskette contains 77 tracks and 26 sectors per track. In the simple density mode each sector can store 128 8-bit bytes for a total formatted capacity of 256,256 8-bit bytes. In the double density mode each sector can store 256 8-bit bytes for a total formatted capacity of 512,512 8-bit bytes.

The diskette is an ideal storage, interchange, and software distribution medium. Compared to disk cartridges or disk packs, it is very inexpensive. Because it is flat and thin, the diskette is compact, enabling large amounts of data to be conveniently stored in a small space. Diskettes can also be easily transported in a briefcase or in a manila envelope.

Because the diskette is preformatted in the industry-standard format, it ensures industry compatibility and drive-to-drive interchangeability. In single density mode, the RX02 can read diskettes written on other standard floppy disk equipment and vice versa. Preformatted diskettes also reduce hardware costs and improve reliability by eliminating the circuitry required to generate the correct format.

RELIABILITY
The RX02 provides exceptional reliability as well as low cost. The simple mechanical construction of the drive and the use of a microprogrammed controller that reduces hardware complexity contribute to the design goal MTBF (Mean Time Between Failures) of 5000 hours. To enhance disk life, the head contacts the disk only during reading or writing, or seeking. Heads are automatically unloaded if operational requests exceed 200 msec intervals. With the head loaded on a given track, the media can withstand one million passes.

The RX02 performs checks and provides error indications. Each sector has a cyclic redundancy check (CRC) character as part of the header field and another CRC character as part of the data field. The RX02 generates and verifies the CRC characters and provides error indications.

The Read Error Register command in addition to reporting the definitive error code gives the current track of drive 0, the current track of drive/target track, target sector, word count, and internal controller status.

A soft write protect is achieved through the structure of the RX02 operating system software.
Both the RX02 and RX01 controller cannot initiate a "write" command unless specifically instructed by the operating system's file handler software. Specific circuits have been incorporated that prevent spurious activity in the write chain during up or down power transitions.

**OPERATION**
The RX02 Floppy Disk drive unit is simple to operate. When the door is opened, the diskette, properly oriented, can be inserted. When the door is closed, the diskette is engaged on the registration hub. Once the diskette drive attains operating speed, the software takes over. The diskette removal procedure is the reverse of the insertion procedure. Elimination of any other operator controls greatly simplifies operation.

**REGISTERS**

**Command and Status 777 170**
The Command and Status Register contains the unit select, function density, and function bits. There are three function bits giving a total of eight functions. The unit select bit is for logical selection of one of the two drives on the system.

**Function Codes:** Bits 1, 2, and 3 contain the function codes for the RX02. When DONE is set, the control will negate out and upon reception of the next Run, will negate DONE and then issue the appropriate number of SHIFT pulses to the interface. The interface will respond by asserting the proper bits in sequence to the data bus for transfer to the controller.

- Bit 0: GO bit which initiates a command
- Bit 4: UNIT SELECT
- Bit 5: DONE
- Bit 6: INTERRUPT ENABLE
- Bit 7: TRANSFER REQUEST
- Bit 8: COMMAND DENSITY
- Bit 11: RX02 Bit
- Bit 12, 13: EXTENDED ADDRESS
- Bit 14: INITIALIZE
- Bit 15: ERROR

**Data Buffer Register (RX2DB) 777 172**
This register is write only or read only depending on the function.

All data transferred to and from the floppy media passes through this register, and is addressable only under the protocol of the
function in progress. The element of data transfer to and from the host processor is a word. The element of data transfer to and from the controller is 8 bits.

**RX2BA—RX211 Bus Address Register**
This register specifies the bus address of data transferred during Fill Buffer, Empty Buffer, and Read Definitive Error operations. Incrementation takes place after a memory transaction has occurred. The RX2BA, therefore, is located with the address of the first data word to be transferred. This is a 16 bit write-only register

**Track Address Register (RX2TA)**
This 8-bit write-only register is loaded to indicate on which of the 77(sub)10 tracks a given function is to operate. It can be addressed only under the protocol of the function in progress.

```
 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
   |   |   |   |   |   |   |   |   |

0→1148
```

**Sector Address Register (RX2SA)**
This register is loaded to indicate on which of the 26(sub)10 sectors a given function is to operate. It can be addressed only under the protocol of the function in progress.

```
 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
   |   |   |   |   |   |   |   |   |

0 0 0
```

**Data Buffer Register (RX2DB)**
This register is write only or read only depending on the function. All data transferred to and from the floppy disk passes through this register. It is addressable only under the protocol of the function in progress. The element of data transfer to and from the host processor is a word. The element of data transfer to and from the control is 8 or 12 bits.

**Error and Status Register (RX2ES)**
This register contains the current error and status conditions of the selected drive. The contents of RX2ES is moved to the interface data buffer at the end of every function.
Bit: 11-15 Name:
Function: Unused

Bit: 10 Name: Word Count Overflow
Function: The Word Count Register resides in the control. If the control senses that the word count is beyond sector size, it will terminate the Fill or Empty Buffer operation and set Error and Done.

Bit: 9 Name: 0
Function: Reserved

Bit: 8 Name: Unit Select
Function: Drive 0 is selected if bit 8 = 0. This bit indicates the drive that is currently selected.

Bit: 7 Name: Drive Ready
Function: The selected drive is ready if bit 7 = 11. All conditions for disk operation are satisfied, such as door closed, power O.K., diskette up to speed, etc. The RX02 may be presumed to be ready to perform any operation. This bit is only valid when retrieved via a Read Status function or initialize.

Bit: 6 Name: Deleted Data
Function: In the course of recovering data, the "deleted data" address mark was detected at the beginning of the data field. The Dry Den bit (bits) indicates whether the mark was a single or double density deleted data address mark. The data following the mark will be collected and transferred normally, as the deleted data mark has no further significance other than to establish drive density. Any alteration of files or deletion of data due to this mark must be accomplished by user software.

Bit: 5 Name: Drive Density
RX02

**Function:** Indicates the density of the diskette in the drive selected (see bit 8). The density of the drive is determined during the Read and Write Sector operations.

**Bit: 4**  
**Name:** Density Error

**Function:** Indicates that the density of the function in progress does not match the Drive Density. Upon detection of this error, the control terminates the operation and asserts Error and Done.

**Bit: 3**  
**Name:** RXACL

**Function:** Indicates subsystem has lost power.

**Bit: 2**  
**Name:** Initialize Done

**Function:** Indicates completion of the initialize routine. Can be asserted due to: a) an RX02 power failure, b) system power failure, c) programmable or bus initialize.

**Bit: 1**  
**Name:** 0

**Function:** Not used.

**Bit: 0**  
**Name:** CRC Error

**Function:** The cyclic redundancy check at the end of the data field has indicated an error. The data collected must be considered invalid; it is suggested that the data transfer be re-tried up to 10 times, as most data errors are recoverable (soft).

**SPECIFICATIONS**

- Data transfer speed: 14 μsec per byte
- Time for half revolution: 83 msec
- Diskette rotation speed: 360 rpm
- Drives per control: 2

**Track Positioning Time**

- One track move: 6 msec
- Average track seek: 152 msec
- Maximum track seek: 456 msec
- Head settling: 25 msec
- Average access time: 262 msec

**Data Organization**

- Surfaces per diskette: 1
- Tracks: 77 (0-76)

201
Sectors: 26 (1-26)
Capacity per sector: 128 8-bit bytes—single density
256 8-bit bytes—double density
Recording method: MFM, FM
Recording density: 6400 bits per inch maximum

Register Addresses
Command status
(RXCS): 777 170
Data buffer: DMA

UNIBUS Interface
Interrupt vector address: 264
Priority level: normally BR5
Data transfer: programmed I/O
Bus loading: 2 AC loads

Mechanical
Mounting
RX02 mounts in a standard PDP-11 cabinet occupying 10 1/2” of rack height.
Interface requires one SPC slot.

Weight 60 lb (dual drive)

Power
Running current: 5A maximum at 115V, 60 Hz
2.5A maximum at 230V, 50 Hz
Interface current: 1.8A maximum at +5 Vdc
Heat dissipation: 500 watts maximum

Environmental
Temperature: 15°C (59°F) to 32°C (90°F) with a maximum temperature gradient of 20°F per hour or 11°C per hour
Relative humidity: 20% to 80% with a maximum wet bulb of 25°C (77°F) and a minimum dew point of 2°C (36°F)
The LP11/LS11/LA11 line printer systems are high-speed printer systems designed to interface with the PDP-11 UNIBUS family of processors.

The LP11 systems consist of two major components, a line printer and an interface unit referred to as the LP11 controller.

The LS11 systems consist of two components, a line printer and an interface module, referred to as the LS11 controller.

The LA11 systems also consist of two components, a DIGITAL line printer, LA180, and a LA11 controller.

**LP11 LINE PRINTER SYSTEMS**
The LP11 Line Printer system is designed to operate on-line with the PDP-11 UNIBUS systems and associated peripherals such as paper tape readers, magnetic tape units, card readers, or communications terminals. The line printer is mounted in a free-stand-
ing cabinet. The controller, which interfaces the line printer to the UNIBUS, is a single quad module.

When the printer memory is full, a print cycle is initiated and the characters are automatically printed in the first zone (columns 1-0). During the print cycle, the stored characters are scanned and compared in synchronism with the rotating characters on the drum. The printer actuates the appropriate hammer as the desired character approaches the print position. If the comparison indicates an invalid character, that character is erased from the memory.

After the first zone has been printed, the next 20 characters are loaded and printed out on the second zone (columns 21-40) provided no special control character (paper feed, form feed, or carriage return) is recognized by the printer. This process continues until all four zones have been printed. Any time that one of the three control characters is recognized, the current buffer contents are printed and the printer returns to the zone rather than continuing printing of the remaining zones.

The printer responds only to codes representing the character set and the three control characters. All other codes are ignored.

The line printer is a high-speed printer that produces hard copy output at rates up to 1250 lines per minute. The printer employs an impact-type mechanism with a revolving character drum and one hammer per column. Forms making up to six copies can be used when multiple copy printing is desired. The printer is available in three versions: 80 columns with a speed of up to 356 lines per minute for a full line; 132 columns with a speed of up to 245 lines per minute for a full line; 132 columns with a speed of up to 1250 lines per minute for a full line; or 132 columns with a speed of up to 300 lines per minute for a full line. All of the preceding print rates are based on the 64-character drum. The four line-printer models can be ordered with either a 64- or 96-character drum.

**LP11-C, D**—The LP11-C, D 132-column line printer has a maximum line length of 132 columns and prints at a rate of 900 lines per minute (LP11-C) or 660 lines per minute (LP11-D). Designed to handle heavy production loads, these fast, reliable printers feature a new cabinet design that reduces operation noise.

**LP11-F, H**—The LP11-F, H 80-column line printer has a maximum line length of 80 columns and prints at a rate of 356 full lines per minute. If the line length is decreased to 20 columns, the maxi-
mum printing rate is 1110 lines per minute. These rates are based on a 64-character set. If a 96 character set is used, printing rates decrease because of the larger character drum.

A single 80-character line is composed of four 20-character zones. This permits the 20 hammer drivers to be time-shared by the four zones. The printer contains a 20-character memory that stores the image of one zone. The character string is serially loaded into this memory by means of the line printer data buffer register in the LP11 Controller. Although the bits constituting an individual character are parallel loaded, the zone is serially loaded, character by character.

LP11-J, K—The LP11-J, K 132-column line printer has a maximum line length of 132 columns and prints at a rate of 245 full lines per minute, or 1100 lines per minute, if the line length is decreased to 24 columns. It is essentially the same as the 80-column model, except that the memory holds 24 characters and a line is composed of six zones.

LP11-R, S—The LP11-R, S 132-column line printer has a maximum line length of 132 columns and prints at a rate of 1250 full lines per minute when using the 64-character set and 925 full lines per minute when using the 96-character set. The LP11-R, S is distinguished from the two previous versions because it contains one 132-character memory; there are no zones. A print hammer is assigned to each of the 132 print positions. The LP11-R, S will print a line only after one of three control characters is sent to it.

LP11-V, W—The LP11-V, W 132-column line printer has a maximum line length of 132 columns and prints at a rate of 300 lines per minute when using the 64-character set, and 240 lines per minute when using the 96-character. A 132-column memory is contained within the line printer. Printing is accomplished by dividing the 132 columns into odd and even positions and sharing a hammer and associated drive circuit between two positions. The LP11-V, W will print a line only after one of three control characters is sent to it.

LP11-Y, Z—The LP11-Y, Z line printer systems have a line length of 132 columns (136 columns by special arrangement) and print at a rate of 600 lines per minute, when using the 64 ASCII character set, and 436 lines per minute when using the 96 ASCII character set.

Both models contain one 132-character memory with a print hammer assigned to each of the 132 print positions. Also available
with the printer is an optional Direct Access Vertical Format Unit (DAVFU) which is a highly reliable paper advance controller. The DAVFU is loaded and activated under control of the user's program, inserting special non-printing characters in the data stream being set to the printer. An output to the printer for setting the DAVFU control begins with a star code of 356 (octal) followed by paper advance command(s) and then terminated with a stop code of 357 (octal). Information following the stop code is considered printable data by the printer.

During the print cycle, the stored characters are scanned and compared in synchronism with the rotating character drum. The printer actuates the appropriate hammer as the desired character approaches the print position. If the comparison indicates an invalid character, then that character is erased from memory.

The printer responds only to codes representing the character set and the four control characters (paper feed, form feed, VFU command, and carriage return). All other codes are ignored.

Two types of print drums are available: EDP or Scientific.

**LS11 LINE PRINTER**
The LS11 Line Printer systems have the following features:

- Average printing speed is 132 characters/second, including the return time of the printing head.
- Line printing speeds are 60 lines/minute on full lines and up to 200 lines/minute on short lines.
- Print size is 10 characters/inch horizontally and 6 lines/inch vertically.

The line printer contains a 132-character memory buffer, which is loaded character-by-character via the LS11 controller. Once the 132-character memory is full, the printer automatically prints the 132 characters on a line and then performs an automatic carriage return. There is, however, a carriage return command that is performed for lines containing less than 132 characters as specified by the programmer.

Each character is transferred to the line printer in a parallel 7-bit format. These 7-bit characters are in ASCII code. This line printer does not print lowercase characters. Of the ASCII character set, the line printer uses nine commands.

**LA11 LINE PRINTER SYSTEMS**
The LA11 system operates on-line with a PDP-11 system and its associated peripherals. The line printer is a free-standing, ped-
estal-type terminal that is capable of printing a maximum of 132 characters per line. To initiate a print cycle, a line terminator character (LF, FF, CR) is required. The printer contains a $256 \times 8$ character buffer RAM which stores printable and nonprintable characters. This RAM is loaded character-by-character through a single character buffer via the LA11 controller under microprogramming control. After each character is stored in memory, a read function is performed to determine whether the line should be terminated, causing the line of stored data to be printed.

**CONTROLLER**  
The LP11/LS11/LA11 controller, under program control, interfaces the line printer to the PDP-11 UNIBUS. The controller synchronizes data transfer between the bus and the printer. The functions of the controller are to:

- indicate to the CPU the operational status of the line printer
- control transfer of data from the PDP-11 system into the printer
- enable the line printer to gain control of the bus and to perform an interrupt routine

**REGISTERS**  
All software control of the line printer controller is performed through two device registers. These registers have been assigned bus addresses, and can be read or loaded by any PDP-11 instruction that refers to their address.

**Line Printer Control and Status Register 777514**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>ERROR</td>
<td>Asserted (1) whenever an error condition exists in the line printer. Error conditions for the LP11 are: power off, no paper, printer drum gate open, oven-temperature alarm, PRINT INHIBIT switch off, printer off-line, or torn paper. LS11 errors are: paper empty, hardware alarm, light detection, or select.</td>
</tr>
</tbody>
</table>
LP11/LS11/LA11

LA11 errors are: fault (paper fault), or on-line switch (in off position).
Reset only by manual correction of error condition. Read only.

Bit: 14-8  Name:  
Function:  Not Used

Bit: 7  Name: READY (LP11)
Function:  Asserted (1) whenever printer is ready for next character to be loaded. Indicates that previous function is either complete or has been started and continued to a point where the printer can accept the next command. This bit, which must be on-line, is set by the printer; if the controller is being used, READY can be set by INIT. Read only.

Bit: 7 (cont)  Name: DONE (LS11/LA11)
Function:  Asserted (1) when the line printer is ready to accept another character. DONE is set by INIT and cleared by loading the LSDB. If Interrupt Enable is also set, the LS11 starts an interrupt sequence.

Bit: 6  Name: INTR ENB
Function:  Set or cleared under program control. Cleared by INIT (initialize) signal on UNIBUS. (INIT caused by programmed RESET instruction, console START function, or a power-up or power-down condition.) When set, an interrupt is requested when READY or ERROR becomes a 1.

Bit: 5-0  Name:  
Function:  Not Used.

Line Printer Data Buffer Register 777516

Bit: 15-7  Name:  
Function:  Not used. If these bits are loaded, data is lost in these bits.

Bit: 6-0  Name: DATA
Function:  7-bit ASCII character buffer. Characters are transferred to the line printer by loading this buffer. Can be loaded from the bus. Load only. Data in this buffer cannot be read. Always reads as all 0s.
LINE PRINTERS

LP11/LS11/LA11

SPECIFICATIONS

<table>
<thead>
<tr>
<th>ELECTRICAL</th>
<th>LP11-C, D</th>
<th>LP11-F, H</th>
<th>LP11-J, K</th>
</tr>
</thead>
<tbody>
<tr>
<td>115V ±10%</td>
<td>330W</td>
<td>500W</td>
<td></td>
</tr>
<tr>
<td>60 Hz ±3 Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>230V ±10%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>50 Hz ±3 Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>825W</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ENVIRONMENTAL

| Operating Temperature | 50°F (10°C) to 104°F (40°C) | 50°F (10°C) to 110°F (43°C) | 50°F (10°C) to 110°F (43°C) |
| Humidity             | 10% to 90%                   | 5% to 90%                     | 5% to 90%                     |

PRINT CHARACTERISTICS

Format
Top-of-form control; single line advance with automatic perforation step-over, and carriage return. Automatic vertical format control is optional.

Paper-Feed
One pair of pin-feed tractors for ½ in. hole center, edge-punched paper.

Paper slew speed
30 in. per sec
13 in. per sec
13 in. per sec

Print Area
13.2 in. wide left justified
8 in. wide left justified
13.2 in. wide left justified

Character Spacing
(horizontal)
0.1 (±0.005) in. between centers; maximum possible accumulative error for normal spacing is 0.01 in. per 80- or 132-character line.

Line Spacing
0.167 (±0.01) in. (6 lines per inch); each character within ±0.1 in. from mean line through character. Also, LP11-R, S and LP11V, W 0.125 in. (8 lines per inch).

Line Advance Time
20 ms max.
20 ms max.
20 ms max.

PHYSICAL CHARACTERISTICS

Printer
Height
44.5 in. (1.17m)
46 in. (1.19m)
47 in.

Width
33 in. (0.8m)
24 in. (0.6m)
49 in.
**LINE PRINTERS**

## LP11/LS11/LA11

<table>
<thead>
<tr>
<th></th>
<th>LP11-R, S</th>
<th>LP11-V, W</th>
<th>LP11-Y, Z CSS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Depth</strong></td>
<td>27.5 in.</td>
<td>22 in.</td>
<td>26 in.</td>
</tr>
<tr>
<td></td>
<td>(0.56m)</td>
<td>(0.56m)</td>
<td>(0.61m)</td>
</tr>
<tr>
<td><strong>Weight</strong></td>
<td>435 lbs.</td>
<td>220 lbs.</td>
<td>575 lbs.</td>
</tr>
<tr>
<td></td>
<td>(100kg)</td>
<td>(100kg)</td>
<td>(260kg)</td>
</tr>
<tr>
<td><strong>SPECIFICATIONS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## ELECTRICAL

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Operating</strong></td>
<td>1950W</td>
<td>700W</td>
<td>680W</td>
</tr>
<tr>
<td><strong>Temperature</strong></td>
<td>50°F (10°C)</td>
<td>50°F (10°C)</td>
<td>50°F (10°C)</td>
</tr>
<tr>
<td></td>
<td>to 110°F (43°C)</td>
<td>to 90°F (32°C)</td>
<td>to 90°F (32°C)</td>
</tr>
<tr>
<td><strong>Humidity</strong></td>
<td>10% to 90%</td>
<td>30% to 90%</td>
<td>30% to 90%</td>
</tr>
</tbody>
</table>

## ENVIRONMENTAL

<p>| | | | |</p>
<table>
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<tr>
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<td><strong>Temperature</strong></td>
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<tr>
<td></td>
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<td>to 90°F (32°C)</td>
<td>to 90°F (32°C)</td>
</tr>
<tr>
<td><strong>Humidity</strong></td>
<td>10% to 90%</td>
<td>30% to 90%</td>
<td>30% to 90%</td>
</tr>
</tbody>
</table>

## PRINT CHARACTERISTICS

<p>| | | | |</p>
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<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>Format</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Paper-Feed</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Paper speed</strong></td>
<td>35 in. per sec</td>
<td>20 in. per sec</td>
<td>25 in. per sec</td>
</tr>
<tr>
<td><strong>Print Area</strong></td>
<td>13.2 in. wide left justified</td>
<td>13.2 in. wide left justified</td>
<td>13.2 in. wide left justified</td>
</tr>
<tr>
<td><strong>Character Spacing (horizontal)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Line Spacing</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Line Advance</strong></td>
<td>14ms max.</td>
<td>50ms max.</td>
<td></td>
</tr>
<tr>
<td><strong>Time</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## PHYSICAL CHARACTERISTICS

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Printer</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Height</strong></td>
<td>46 in.</td>
<td>45 in.</td>
<td>45 in.</td>
</tr>
<tr>
<td></td>
<td>(1.17m)</td>
<td>(1.14m)</td>
<td>(1.14m)</td>
</tr>
<tr>
<td><strong>Width</strong></td>
<td>48.5 in.</td>
<td>32 in.</td>
<td>33 in.</td>
</tr>
<tr>
<td></td>
<td>(1.2m)</td>
<td>(0.81m)</td>
<td>(0.83m)</td>
</tr>
<tr>
<td><strong>Depth</strong></td>
<td>24.5 in.</td>
<td>22 in.</td>
<td>26 in.</td>
</tr>
<tr>
<td></td>
<td>(0.6m)</td>
<td>(0.56m)</td>
<td>(0.66m)</td>
</tr>
<tr>
<td><strong>Weight</strong></td>
<td>800 lbs.</td>
<td>330 lbs.</td>
<td>370 lbs.</td>
</tr>
<tr>
<td></td>
<td>(360kg)</td>
<td>(150kg)</td>
<td>(153kg)</td>
</tr>
</tbody>
</table>

210
The LP05K-LL Long Line Printer kit allows PDP-11 users to operate a line printer up to 2,000 feet away from the computer.

FEATURES
- compatible with the entire PDP-11 family of processors
- useful for applications where it is helpful to have the printer some distance from the computer (for example, real-time or industrial data acquisition or control systems)

DESCRIPTION
The LP05K-LL Long Line Printer operation is transparent to the printer options. There are no controls or indicators directly associated with the kit. The kit enables a user to position a line printer in the area that is most convenient, regardless of the distance (up to 2,000 feet) from the processor.

SPECIFICATIONS
- Mechanical
- Logic Mounting: CSS
- Logic Potential: one quad height module
- Module Type: one SPC slot
- Power Requirements: TTL
- 1.5 amps @ +5V
LINE PRINTERS

LXY11

The LXY11 is a high speed, high precision printer that operates at a line printer speed of 300 lines per minute.

FEATURES
• versatile, can be used as a line printer, as a plotter, or both simultaneously
• excellent print quality
• prints on single or multipart forms

DESCRIPTION
The LXY11 printer plotter system consists of a high speed, high precision printer and a module that provides the interface to the PDP-11 UNIBUS processor. Operating at 300 lines per minute, the impact printer/plotter can be used as a line printer, a plotter, or both. It prints on single or multi-part forms on continuous fanfold, edge-perforated paper from $4\frac{1}{2}$ to 16 inches wide. The printer produces high quality copy on multipart business forms and labels. The excellent print quality is achieved by overlapping dots of uniform density. A character is formed by a $9 \times 7$
dot matrix, with five overlapping dots in the horizontal plane on nine centers for accurate character rendition. The precision of the printing mechanism assures accurate dot placement.

The printer/plotter operates by the printer logic by receiving a line of incoming data, storing it in a 132-character register and decoding the commands that control the paper transport and other functions. The logic controls the handshaking cycle with which the printer communicates with the controller. When the printer memory 132 character register is full, a print cycle is initiated, and the characters are automatically printed.

REGISTERS

Line Printer Control and Status Register 777514

Bit: 15  Name: Error
Function: Asserted (1) whenever an error condition exists in the line printer. Error conditions are power off, no paper, printer off-line, torn paper, form thickness adjustment open.

Bit: 14-8  Name: Not Used
Function: Not Used

Bit: 7  Name: Ready
Function: Asserted (1) whenever printer is ready for next character to be loaded. Indicates that previous function is either complete or has started and continued to a point where the printer can accept the next command. This bit, which must be on-line, is set by the printer; if the controller is being used, Ready can be set by INIT. Read only.

Bit: 6  Name: Intr Enb
Function: Set or cleared under program control. Cleared by INIT (initialize) signal on UNIBUS. (INIT caused by programmed Reset instruction, console start function, or a power down condition). When set, an interrupt is requested when Ready or Error becomes a 1.

Bit: 5-0  Name: Not used
Function: Not used

Line Printer Data Buffer Register 777516

Bit: 15-8  Name: Not used
Function: If these bits are loaded, data is lost in these bits.
**LINE PRINTERS**

**LXY11**

**Bit: 6-0  Name: Data**

**Function:** 7-bit ASCII character buffer. Characters are transferred to the line printer by loading this buffer. Can be loaded from the bus. Load only. Data in this buffer cannot be read. Always as all 0’s.

**Bit: 7  Name: PI**

**Function:** Enables paper INST if EVFU or tape VFU is implemented.

All other bits are unused.

**SPECIFICATIONS**

**Printing/Plotting Speed**

- Printing PROM driven characters: 300 LPM
- Printing PROM driven characters and underlining or characters with descenders: 240 LPM
- Plotting, simultaneous printing/plotting at 50% dot density or printing double height characters: 170 LPM (16-2/3 in./min)
- Plotting or simultaneous printing/plotting at 25% dot density: 300 LPM (33-1/3 in./min)

**Print**

- **Standard Characters:** 96 EDP w or w/o underline
  - Double height EDP set w or w/o underline.
- **Characters/line:** Up to 132
- **Lines/inch:** 6 or 8
- **Dot matrix:** 
  - 9 × 7 for upper case
  - 9 × 9 for lower case
- **Dot Size Resolution:**
  - .020 in. diameter
  - 60 dots/in. horiz.
  - 70 dots/in. vert.

**Multipart Forms**

- Up to 6 parts

**Physical Characteristics**

- **Size:** 46.5 in. H; 30 in. W; 24.25 in. D
- **Weight:** 200 lbs. (approx.)
- **Features:** Quietized cabinet
  - (below 65dbA)
Environmental
Temperature
  Operating  10° to 38°C/42° to 100°F
  Non-operating  -40° to 65°C/−40° to 149°F
Humidity
  Operating  30 to 90% (non-condensing)
  Non-operating  5 to 95% (non-condensing)

Power Requirements
Voltage & Frequency 85 to 132 Vac
  60 Hz ± 2 Hz
  or
  170 to 264 Vac
  50 Hz ± 2 Hz.
Standby 200 Watts
Nominal 450 Watts
Maximum 800 Watts

CSS
CHAPTER 6

MAGNETIC TAPES

TE10

DESCRIPTION
The TE10 is a high-performance, low-cost magnetic tape ideally suited for writing, reading, and storing large volumes of data and programs in a serial manner. Because the system reads and writes in industry-compatible format, information can be transferred between a PDP-11 and other computers. For example, a PDP-11 might be used to collect data and record it for later processing on a large-scale computer. The 10½-inch tape reels contain up to 2400 feet of tape upon which over 180 million bits of data can be stored on high-density 9-track tape or over 140 million bits can be stored on high-density 7-track tape.

The TM11 system employs read after write error checking to verify that proper data is written on the tape. Should a tape dropout be detected, appropriate action can be taken to insure no loss of data.

Tape motion is controlled by vacuum columns and a servo-controlled single-capstan. Long tape life is possible because the only contact with the oxide surface is at the magnetic head and at a rolling contact on one low-friction, low-inertia bearing.

A magtape system consists of up to 8 tape transports and a control unit. Transports are capable of operation with seven or nine-track tape and a system can contain any combination of 7- and 9-track units. A TM11 includes a control unit and the first tape transport.

Operation
Reading and writing occurs when the tape is moving forward, but the control can move the tape to new positions in forward or reverse. For writing on tape, 8-bit data words are transferred from memory to a data buffer in the controller. The data buffer logic supplies the character to the tape transport write logic. For reading, the sequence is reversed and information is read from tape as 6-bit characters for 7-track tape (8 bits for 9-track tape) which are sent to the data buffer. When a word has been assembled in the data buffer, an NPR transfer is initiated to transfer the data buffer word into memory.

The 7- and 9-track systems use ½-inch mylar base tape which is coated on one side with an iron oxide composition. The method of recording is non-return-to-zero (NRZ). A seven-track tape includes six data channels and a lateral parity channel. Density
modes of 200, 556, and 800 bytes per inch are selectable. Nine-track tape is similar to the 7-track tape, but operation is only in the 800 bpi mode and it has the industry standard cyclic redundancy character at the end of each record. The load and end points of the tape are marked by reflective strips which are detected by photo diodes. About 10 inches of blank tape is wound on a reel and precedes the BOT and EOT strips; a gap of about 3 inches is left from the load point before writing can begin.

Each computer word contains two 8-bit tape characters. Record blocks are separated by 3/4-inch gaps on 7-track units and 1/2-inch gaps on 9-track units. The industry standard format has 7-track tape records containing from 24 to 4008 characters, and 9-track tape records from 18 to 2048 characters.

Magtape Format
REGISTERS
Status Register (MTS) 772 520

Bit: 15  Name: Illegal Command
Function: Set by any of the following illegal commands.
          Any DATO or DATOB to the Command Register MTC during the tape operation period.
          A write, write EOF, or write with extended IRG operation when the FILE PROTECT bit is a 1.
          A command to a tape unit whose SELECT REMOTE bit is a 0.
          The SELECT REMOTE (SELR) bit becoming a 0 during an operation.

In error conditions 1 through 3, the command is loaded into the MTC, but the GO pulse to the tape unit is not generated. In addition the CU ready bit remains set.

Bit: 14  Name: End of File (EOF)
Function: Set when an EOF character is detected during a read, space forward or space reverse operation. During the read or space forward operation, the EOF bit is set when the LPC (longitudinal parity check) character following the EOF character is read. During a space
reverse operation, the EOF bit is set when the EOF character following its LPC character is read. The ERR bit sets when the LPC character strobe is generated with the FILE MARK signal upon EOF detection.

Bit: 13  Name: Cyclical Redundancy Error (CRE)
Function: Detected only during a read operation. It compares the CRC character read from tape with that regenerated during the same read operation. If they are not the same, CRC ERROR from the tape unit becomes a 1 until the LPC character is detected.

Bit: 12  Name: Parity Error (PAE)
Function: The OR of the lateral and longitudinal parity errors. A lateral parity error is indicated on any character in the record while a longitudinal parity error occurs only when the LPC character is detected.

A parity error does not affect the transfer of data; that is, in a write operation, the entire record is transferred to tape and in a read operation, the entire record is written into core memory.

For all parity errors, the ERR bit sets only when the LPC character is detected. Both lateral and longitudinal parity errors are detected during a read, write, write EOF, and write with extended IRG operations. The entire record is checked, including the CRC and LPC characters. Longitudinal parity error occurs when an odd number of ones is detected on any track in the record. A lateral parity error occurs when an even number of ones is detected on any character when PEVN is a 0, or an odd number of ones is detected on any character when PEVN is a 1.

Function: Name: Bus Grant Late (BGL)
Bit: 11  Set when the control unit, after issuing a request for the bus, does not receive a bus grant before the control unit receives the bus request for the following tape character. The condition is tested only for NPR (non-processor request) operations. The ERR bit sets simultaneously with BGL, thus terminating the operation. If the BGL occurred during a write or write with extended IRG operation, the control unit does not send the signal WDS to the master, while the master writes the CRC character (if required) and LPC character onto the tape, terminating the record.
Bit: 10  Name: End of Tape (EOT)
Function: Set when the EOT marker is read while the tape is moving in the forward direction. The bit is cleared as soon as the same point is read while the tape is moving in the reverse direction. The ERR bit, as a result of the EOT bit at a 1, sets only in the tape forward direction and coincidentally with the reading of an LPC character.

Bit: 9  Name: Record Length Error (RLE)
Function: Detected only during a read operation. It occurs for long records only and is indicated as soon as MTBRC increments beyond 0, at which time both data transfer into memory and incrementing of the MTCMA and MTBRC stop.

However, the control unit reads the entire record and sets the ERR bit when the LPC character is read. CU ready remains at 0 until the LPC character is read.

Bit: 8  Name: Bad Tape Error (BTE)
Function: Sets when a character is detected (RDS pulse) during the gap shut-down or settling down period for all operations (except rewind). When BTE is detected, the ERR bit is set immediately, and if INT ENB is set, an interrupt sequence is started.

Bit: 7  Name: Non-Existent Memory (NXM)
Function: Set during NPR operations when the control unit is bus master and is performing data transfers into and out of the bus when the control unit does not receive a slave SYNC signal within 10 microseconds after it had issued a master sync signal. The operations which occur when the error is detected are identical to those indicated for the BGL error.

Bit: 6  Name: Select Remote (SELR)
Function: Cleared when the tape unit addressed does not exist, is off-line, or has its power turned off.

Bit: 5  Name: Beginning Of Tape (BOT)
Function: Set when the BOT marker is read, and cleared when the BOT marker is not read. BOT at a 1 does not produce a 1 in the ERR bit.

Bit: 4  Name: Seven Channel (7 CH)
Function: Set to indicate a 7-channel tape unit; cleared to indicate a 9-channel unit.
Bit: 3  Name: Tape Settle Down (SDWN)
Function: Set whenever the tape unit is slowing down. The master will accept and execute any new command during the SDWN period except if the new command is to the same tape unit as the one issuing SDWN and if the direction implied in the new command is opposite to the present direction.

Bit: 2  Name: Write Lock (WRL)
Function: Set to prevent the control unit from writing information on tape. Controlled by the presence or absence of the write protect ring on the tape reel.

Bit: 1  Name: Rewind Status (RWS)
Function: Set by the master as soon as it receives a rewind command from the control unit. Cleared by the master as soon as the tape arrives at the BOT marker in the forward direction. (It overshoots BOT in the reverse direction.)

Bit: 0  Name: Tape Unit Ready (TUR)
Function: Set when the selected tape unit is stopped and when the SELECT REMOTE is false. Cleared when the processor sets the GO bit and the operation defined by the function bit occurs.

Command Register (MTC) 772 522

Bit: 15  Name: Error (ERR)
Function: Set as a function of bits 7-15 of the Status Register MTS. Cleared on INIT or on the GO command to the tape unit.
**MAGNETIC TAPES**

**TE10**

**Bit: 14-13  Name: Density (DEN 8, DEN 5)**

**Function:** Cleared on INIT.

<table>
<thead>
<tr>
<th>Bit 14</th>
<th>Bit 13</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>200 bpi</td>
<td>7 channel</td>
</tr>
<tr>
<td>0 1</td>
<td>556 bpi</td>
<td>7 channel</td>
</tr>
<tr>
<td>1 0</td>
<td>800 bpi</td>
<td>7 channel</td>
</tr>
<tr>
<td>1 1</td>
<td>800 bpi</td>
<td>9 channel</td>
</tr>
</tbody>
</table>

**Bit: 12  Name: Power Clear (PCLR)**

**Function:** Provides the means for the processor to clear the control unit and tape units without clearing any other device in the system. The PCLR bit is always read back by the processor as 0.

**Bit: 11  Name: Lateral Parity (PEVN)**

**Function:** Set for even parity. Cleared for odd parity. A search for parity error is made in all tape moving operations except space forward, space reverse, and rewind.

**Bit: 10-8  Name: Unit Select**

**Function:** Specifies one of the eight possible magnetic tape units. All operations defined in the MTC and all status conditions defined in the MTS pertain to the unit indicated by these bits. Cleared on INIT.

**Bit: 7  Name: CU Ready (CUR)**

**Function:** Cleared at start of a tape operation, and set at end of tape operation. The control unit accepts as legal all commands it receives while the CU Ready bit is 1.

**Bit: 6  Name: Interrupt Enable (INT ENB)**

**Function:** When set, an interrupt occurs whenever either the CU Ready bit or the ERR bit change from 0 to 1 or whenever a tape unit that was set into rewind has arrived at the beginning of tape. In addition, an interrupt occurs on an instruction that changes the INT ENB from 0 to 1 and does not set the GO bit (i.e., CU READY or ERROR = 1).

**Bit: 5-4  Name: Address Bits**

**Function:** Extended memory bits for an 18-bit bus address. Bit 5 corresponds to XBA17, and bit 4 to XBA16. They are an extension of the MTCMA, and increment during a tape operation if there is a carry out of MTCMA.

**Bit: 3-1  Name: Function Bits**

**Function:** Selects 1 of 8 functions (programmable commands).
MAGNETIC TAPES

BIT 3     | BIT 2 | BIT 1
----------|-------|-------
0         | 0     | 0     
Off line  | 0     | 1     
Read      | 0     | 0     
Write     | 0     | 1     
Write EOF | 0     | 1     
Space Forward | 0   | 0     
Space Reverse | 1   | 1     
Write with Extended Interrecord Gap | 1   | 1     
Rewind    | 0     | 1     

Bit: 0     Name: Go

Function: When set, begins the operation defined by the function bits.

Byte Record Counter (MTBRC) 772 524
The MTBRC is a 16-bit binary counter which is used to count bytes in a read, write, or write with extended IRG operation, or records in a space forward or space reverse operation. When used in a write or write with extended IRG operation, the MTBRC is initially set by the program to the two's complement of the number of bytes to be written on tape. The MTBRC becomes 0 after the last byte of the record has been read from memory. When the next WDS (Write Data Strobe) signal occurs from the master, the control unit will not send the WDR (Write Data Request) to the master indicating that there are no more data characters in the record.

When the MTBRC is used in a read operation, it is set to a number equal to or greater than the two's complement of the number of words to be loaded into memory. A record length error (RLE) occurs for long records only, and is indicated when a read pulse for data (RDS occurring when CRCS or LPCS does not occur) occurs when the MTBRC is 0. The MTBRC increments by 1 immediately after each memory access.

When the MTBRC is used in a space forward or space reverse
operation, it is set to the twos complement of the number of records to be spaced. It is incremented by a 1 at LPC time, whether the tape is moving in the forward or reverse direction. A new GO pulse is sent to the tape unit during the SDWN time if the MTBRC is not 0 during that time. When the tape unit is moving in reverse, the LPC character is detected before SDWN, but before the entire record has been traversed. Thus, both SDWN and LPC characters appear to be in different positions on tape from those when the tape unit is moving forward.

**Current Memory Address Register (MTCMA) 772 526**
The MTCMA contains 16 of the possible 18 memory address bits. It is used in NPR operations to provide the memory address for data transfers in read, write, and write with extended IRG operations. Prior to issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a read operation, or from which the first byte is read in a write or write extended IRG operation. The MTCMA is incremented by 1 immediately after each memory access. Thus, at any instant of time, the MTCMA points to the next higher address than the one which had most recently been accessed. When the entire record has been transferred, the MTCMA contains the address plus 1 of the last character in the record. In the error conditions Bus Grant Late (BGL) and Non-Existent Memory (NXM), the MTCMA contains the address of the location in which the failure occurred.

The MTCMA is available to the processor on a DATI, except bit 0 which always reads as a zero under program control. Bit 0 can be asserted during NPRs to determine the selected byte. The bits are set or cleared on a processor DATO. INIT clears all bits in the MTCMA.

**Data Buffer (MTD) 772 530**
The data buffer is an 8-bit register which is used during a read, write, or write with extended IRG operation. In a read operation, the data buffer is a temporary storage register for characters read from tape before being stored into memory. In a processor read, all nine bits are stored into memory. Bits 0 through 7 in memory correspond to channels 7 through 0 respectively from tape, and bit 8 corresponds to the parity bit. In an NPR operation, only the data bits are read into memory and are alternately stored into the low and high bytes. In a write or write with extended ERG operation, the data buffer is a temporary storage register for characters read from core memory before they are written on tape. The polarity of the parity bit is determined by the PEVN bit in the MTC.
MAGNETIC TAPES

TE10

In a read operation, the LPC character enters the data buffer when bit 14 or MTRD is a 1, and inhibited from doing so when 14 is a 0. Thus, after reading a nine-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the CRC character when bit 14 is a 0. After reading a seven-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the last data character when bit 14 is a 0. After reading an EOF character, the data buffer contains all zeros when bit 14 is a 1 and the LPC character when bit 14 is 0. The MTD is available to the processor on a DATI. Bits 9 through 15 read identically to bits 1 through 7 respectively. Bits 0 through 7 are set or cleared on a processor DATO. Bits 8 through 15 are not affected by the processor DATO. INIT clears all bits in the MTD.

TU10 Read Lines (MTRD) 772 532
The memory locations allocated for the TU10 read lines are:
Bits 0-7 for the channels 7-0 respectively.
Bit 8 for the parity bit.
Bit 12 for the gap shutdown bit.
Bit 13 for the BTE error generation.
Bit 14 for the CRC, LPC character selector.
Bit 15 for the timer.

For correct longitudinal parity, bits 0-8 are 0 after writing a record or reading a record from tape. For a longitudinal parity error, one or more of the bits 0-8 remains at a 1; the bit(s) at a 1 indicating the channel(s) containing the error which sets the CU Ready bit. Thus, if the pulse is set during a tape operation, CU Ready sets prematurely, thus producing the gap shutdown period when characters are still being read. Bits 0-8 are set and cleared by the tape unit. Bit 13 is a pulse generated by the processor. Bit 14 is set and cleared by the processor and cleared by INIT. Bit 15 is uniquely controlled by the 100-microsecond timer. The MTRD is available to the processor on a DATI except that bit 13 reads back as a 0.

Timer
TIMER is a 10 KHz signal with a 50 duty cycle. The signal is used for diagnostic purposes in measuring the time duration of the tape operations. The timer is read as bit 15 in the MTRD.

SPECIFICATIONS FOR TM11
Main Specifications
Storage medium 1/2" wide magnetic tape (industry compatible)

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## MAGNETIC TAPES

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity/tape reel</td>
<td>5 to 20 million characters</td>
</tr>
<tr>
<td>Data transfer speed</td>
<td>36,000 char/sec</td>
</tr>
<tr>
<td>Drives/control, max</td>
<td>8</td>
</tr>
<tr>
<td><strong>Data Organization</strong></td>
<td></td>
</tr>
<tr>
<td>Number of tracks</td>
<td>7 or 9</td>
</tr>
<tr>
<td>Recording density</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7-track—200, 556, or 800 bits/inch; program selectable</td>
</tr>
<tr>
<td></td>
<td>9-track—800 bits/inch</td>
</tr>
<tr>
<td>Interrecord gap</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7-track—0.75 inches, min.</td>
</tr>
<tr>
<td></td>
<td>9-track—0.50 inches, min.</td>
</tr>
<tr>
<td>Recording method</td>
<td>NRZI</td>
</tr>
<tr>
<td><strong>Tape Motion</strong></td>
<td></td>
</tr>
<tr>
<td>Read/write speed</td>
<td>45 inches/sec</td>
</tr>
<tr>
<td>Rewind speed</td>
<td>150 inches/sec</td>
</tr>
<tr>
<td>Rewind time</td>
<td>3 minutes, typ</td>
</tr>
<tr>
<td><strong>Tape Characteristics</strong></td>
<td></td>
</tr>
<tr>
<td>Length</td>
<td>2,400 ft.</td>
</tr>
<tr>
<td>Type</td>
<td>Mylar base, iron-oxide coated</td>
</tr>
<tr>
<td>Reel diameter</td>
<td>10 1/2 inches</td>
</tr>
<tr>
<td>Handling</td>
<td>Direct-drive reel motors, servo-controlled single capstan, vacuum tape buffer changers with constant type winding tension.</td>
</tr>
</tbody>
</table>

### Register Addresses

<table>
<thead>
<tr>
<th>Address</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Status</td>
<td>(MTS) 772 520</td>
</tr>
<tr>
<td>Command</td>
<td>(MTC) 772 522</td>
</tr>
<tr>
<td>Byte Record Counter</td>
<td>(MTBRC) 772 524</td>
</tr>
<tr>
<td>Current Mem Address</td>
<td>(MTCMA) 772 526</td>
</tr>
<tr>
<td>Data Buffer</td>
<td>(MTD) 772 530</td>
</tr>
<tr>
<td>TU10 Read Lines</td>
<td>(MTRD) 772 532</td>
</tr>
</tbody>
</table>

### UNIBUS Interface

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt vector address</td>
<td>224</td>
</tr>
<tr>
<td>Priority level</td>
<td>BR5</td>
</tr>
<tr>
<td>Data transfer</td>
<td>NPR</td>
</tr>
<tr>
<td>Bus loading</td>
<td>1 bus load</td>
</tr>
</tbody>
</table>

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MAGNETIC TAPES

TE10

**Mechanical**

- **Mounting**: Mounts in a standard PDP-11 cabinet (supplied)
- **Size**: 26” panel height for tape drive + 10½” for control unit
- **Weight (incl. cab)**: 500 lbs.

**Power**

- **Input current**: 9 A at 115 Vac
- **Heat dissipation**: 1000W

**Environmental**

- **Operating temperature**: 15°C to 32°C
- **Relative humidity**: 20% to 80%

**Miscellaneous**

- **BOT, EOT detection**: Photoelectric sensing of reflective strip, industry compatible
- **Skew control**: Deskewing electronics included in tape transport to eliminate static skew
- **Write protection**: Write protect ring sensing on tape transport
- **Data checking features**: Read after write parity checking of characters; Longitudinal Redundancy Check (7- and 9-channel); Cyclic Redundancy Check (9-channel)
- **Extended features**: Self-test of Control with tape transport offline; core dump for 7-channel units.
- **Magnetic head**: Dual gap, read after write.

**Models**

- **TM11-EA**: Tape transport and control, 9 track, 115 Vac, 60 Hz
- **TM11-ED**: Tape transport and control, 9 track, 230 Vac, 50 Hz
- **TM11-FA**: Tape transport and control, 7 track, 115 Vac, 60 Hz
- **TM11-FD**: Tape transport and control, 7 track, 230 Vac, 50 Hz

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SPECIFICATIONS FOR TU10

Mechanical
Mounting
Mounts in a standard PDP-11 cabinet (supplied)
Size
26" front panel height
Weight (incl. cab)
450 lbs.
FEATURES

- 1600-bpi, 9-track data storage
- program-selectable recording at 1600 bpi (phase encoded) or 800 bpi (NRZI)
- data formats are industry compatible
- 72,000-character/second transfer rate
- up to 40 million characters of storage per reel
- reading in reverse (in addition to forward)
- expandable to eight tape drives in a single system
- vacuum column for tape buffer
- high reliability

DESCRIPTION

The TJE16 is a fully integrated, high-performance magnetic tape storage system that is specifically designed to operate with DIGITAL's PDP-11 computers. It uses standard recording formats, with densities of 1600 and 800 bits per inch, selectable under program
control. Reading and writing are performed at 45 inches/second. Since the industry standard format is used, data may be easily transferred between computers. For example, a PDP-11 system might be used to collect and record data for later processing on another larger computer. Use of magnetic tape permits unlimited off-line data storage.

There are two distinct TJE16 models: phase-encoded at 1600 bpi and NRZI at 800 bpi or NRZI only (both with 9-tracks). The TJE16 includes a control unit plus the master tape control electronics and the first tape drive supplied in a standard cabinet. One control unit can handle up to eight tape drives.

**Data Organization**

Each vertical frame of the 9-track tape represents one character and contains eight data bits plus one parity bit. Since the 16-bit PDP-11 word contains two 8-bit bytes, one byte corresponds to one tape character for efficient data storage.

Groups of characters form a record. The industry standard has 18 to 2048 characters in a single record. Each record block is separated by an interrecord gap (IRG) that is a minimum distance of one-half inch.

Parity is checked character-by-character when reading and writing on tape to verify the accuracy of data transfer. With NRZI, there is also a cyclic redundancy check (CRC) character generated or checked at the end of each record, plus a longitudinal parity check (LPC) character. If an error is detected, an error indication is made.

**Operation**

Reading can be performed while the tape is moving in the forward or the reverse direction, but writing occurs only in forward. The control unit can move the tape to new positions in forward or reverse; it also monitors tape operation. Interrupts are generated when processor attention is required or when an error occurs.

Tape motion is controlled by vacuum columns and a servocontrolled single capstan. Long tape life is possible because the only contact with the oxide surface is at the magnetic head and at a rolling contact on one low-friction, low-inertia bearing. The half-inch mylar-base tape is coated on one side with an iron oxide composition. The load and end points of the tape are marked by reflective strips which are detected by photo diodes. Approximately 10 feet of blank tape is wound on a reel preceding the beginning of tape (BOT) and end of tape (EOT) strips. With NRZI, a
MAGNETIC TAPES

TE16

gap of about three inches is left from the load point before writing can begin; with PE, an identification burst (IDB) is written in this gap.

The tape drive can be controlled locally by the control panel. Local (off-line) controls are: On-line/Off-line, Forward/Reverse/Rewind, Unit Select, Start/Stop, and Brake Release/Load. When on-line, program commands accepted by the transport are: Rewind and Go Off-line, Read Forward, Read Reverse, Write, Write Tape Mark, Space Forward, Space Reverse, Erase, and Rewind to BOT.

There is a provision to prevent accidental writing on a particular tape reel; an industry-standard write-protect ring on the reel is sensed by the tape drive.

Reliability
Data reliability of the TJE16 tape system is enhanced by the 1600-bpi, phase-encoding, self-clocking feature which is not dependent on precise tape skew control. In addition, the 800-bpi NRZI mode includes a tight read-after-write check. The written data is checked to insure that it far surpasses the minimum allowable reading level.

Bad tape error problems are minimized by a "runaway timer" which allows the system to recover from bad tape sections on the reel. If no reading or writing is performed within a tape distance of approximately 25 feet, tape movement will stop and an error will be indicated. Data will not be acknowledged as comprising a data block unless there are at least 12 characters in the block.

Control and Status 1 Register (MTCS1) 772 440

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
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</tr>
</thead>
<tbody>
<tr>
<td>SC</td>
<td>TRE</td>
<td>MCPE</td>
<td>O</td>
<td>DVA</td>
<td>PSEL</td>
<td>A17</td>
<td>A16</td>
<td>RDY</td>
<td>IE</td>
<td>F4</td>
<td>F3</td>
<td>F2</td>
<td>F1</td>
<td>FB</td>
<td>GO</td>
</tr>
</tbody>
</table>

Bit: 15  Name: Special Condition (SC)
Function: Set by TRE, ATTN, or I/O bus control parity error. Cleared by UNIBUS A INIT, controller clear, or by removing the ATTN condition. Read only.

Bit: 14  Name: Transfer Error (TRE)
Function: Set by DLT, WCE, UPE, NED, NEM, PGE, MXF, MDPE, or a drive error during a data transfer. Cleared by UNIBUS A INIT, controller clear, error clear, or loading a data transfer command with GO set. Read/write.

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Bit: 13
Name: Mass I/O Bus Control Bus Parity Error (MCPE)
Function: Set by parity error on control bus while reading a remote register (located in the drive). Cleared by UNIBUS A INIT, controller clear, error clear, or loading a data transfer command with the GO bit set. Read only.
Parity errors that occur on the I/O control bus while writing a drive register are detected by the drive and cause the PAR error (MTER register, bit 3) to set.

Bit: 12
Name: Not used
Function: Always read as 0.

Bit: 11
Name: Drive Available (DVA)
Function: Always a 1 in the TM02 when read from an existing drive. Read only.

Bit: 10
Name: Port Select (PSEL)
Function: When PSEL = 1, data transfer is via UNIBUS B; when PSEL = 0, data transfer is via UNIBUS A. Cleared by UNIBUS A INIT, controller clear, or by writing a 0 in this bit position, Read/write.

Bit: 9
Name: UNIBUS Address (A17)
Function: Upper extension bit of the MTBA register. Cleared by UNIBUS A INIT, controller clear or by writing zeros in these bit positions.

Bit: 8
Name: UNIBUS Address Read/Write (A16)
Function: Upper extension bit of the MTBA register. Cleared by UNIBUS A INIT, controller clear or by writing zeros in these bit positions.

Bit: 7
Name: Ready (RDY)
Function: RDY normally = 1. During data transfers, RDY = 0. When a data transfer command code (51(sub)8 - 77 (sub)8) is written into MTCS1, RDY is reset. At the termination of the data transfer, RDY is set. Read/only.

Bit: 6
Name: Interrupt Enable (IE)
Function: IE is a control bit which can be set only under program control. When IE = 1, an interrupt may occur due to RDY or ATTN being asserted. Cleared by UNIBUS A INIT, controller clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled. Read/write.
MAGNETIC TAPES

Bit: 5-0  Name: F4-F0 and GO
Function: F4-F0 are function (command) code control bits that
determine the action to be performed. The function
code bits are stored in the selected drive.

The GO bit (MTCS1, bit 0) must be set to cause the
controller or drive to respond to a command. The GO
bit is reset by the drive after command execution.

Cleared by UNIBUS A INIT or controller clear (will
abort command execution in all drives). Read/write.

Operation
No Op
Rewind Off-line*
Rewind
Drive Clear
Erase
Write Tape Mark
Space Forward
Space Reverse
Write Check Forward
Write Check Reverse
Write Forward
Read Forward
Read Reverse

Function Code F(0-5)
(Octal)
01-
03
07
11
25
27
31
33
51
57
61
71
77

* Requires manual intervention to return transport on-line.

Word Count Register (MTWC) 772 442

Bit: 15-0  Name: Word Count (WC)
Function: Set by the program to specify the number of words to
be transferred (twos complement form). This register is
cleared only by writing zeros into it. Incremented for
each data transfer. Read/write.

UNIBUS Address Register (MTBA) 772 444

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**MAGNETIC TAPES**

**Bit: 15-1  Name: UNIBUS Address (BA 15-1)**

**Function:** Loaded by the program to specify the starting memory address of a transfer. Cleared by UNIBUS A INIT or by controller clear. The BA register is incremented by 2 after each transfer of a word to or from memory. Read/write.

**Frame Count Register (MTFC) 772 446**

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
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<td>FC</td>
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</table>

**Bit: 15-0  Name: Frame Count (FC 15-0)**

**Function:** Cleared by writing zeros in the bit locations. Designates, in twos complement form, the number of records to be spaced over, characters to be written, or characters that have been read. Initiating a write or space command when the frame count register is loaded with zeros implies a count of 2(**)16. Read/write.

**Control and Status 2 Register (MTCS2) 772 450**

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
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<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>DLT</td>
<td>WCE</td>
<td>UPE</td>
<td>NED</td>
<td>NEM</td>
<td>PSE</td>
<td>MAP</td>
<td>MDP</td>
<td>OR</td>
<td>CLR</td>
<td>PAT</td>
<td>BAI</td>
<td>U2</td>
<td>U1</td>
<td>U6</td>
<td></td>
</tr>
</tbody>
</table>

**Bit: 15  Name: Data Late (DLT)**

**Function:** Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write-check operation at the time the drive demands a transfer. Also set when the controller is performing a data transfer operation over the second UNIBUS (PSEL = 1) and a UNIBUS B INIT is received on that port. Cleared by UNIBUS A INIT, controller clear, error clear, or loading a data transfer command with GO set.

DLT causes TRE. A DLT error indicates a severely overloaded bus. Can also be set by the program reading or writing the MTDB register. Read only.

235
**Bit: 14**  
**Name:** Write Check Error (WCE)  
**Function:** Set when the controller is performing a write-check operation and a word on the tape does not match the corresponding word in memory. Cleared by UNIBUS A INIT, controller clear, error clear, or by loading a data transfer command with GO set.

WCE causes TRE. If a mismatch is detected during a write-check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in MTBA (and extension) is the address of the word following the one which did not match (if BAI is not set). The mismatched data word from the tape drive is displayed in the data buffer (MTDB). Read only.

**Bit: 13**  
**Name:** Parity Error (PE)  
**Function:** Set if the parity lines indicate a parity error while the controller is performing a write or write-check command. Cleared by UNIBUS A INIT, controller clear, error clear, or by loading a data transfer command with GO set.

PE causes TRE. When the UNIBUS is selected to do 18-bit data transfers, the PE error is disabled. When a parity error occurs, the MTBA register contains the address +2 of the memory word with the parity error (if BAI is not set). This bit may be set by program control for diagnostic purposes. Read/write.

**Bit: 12**  
**Name:** Non-Existent Drive (NED)  
**Function:** Set when the program reads or writes a drive register (CS1, DS, ER, MR, FC, DT, CK, TC, or SN) in a drive (selected by U 2-0) which does not exist or is powered down. (The drive fails to assert TRA within 1.5μs after assertion of DEM.) Cleared by UNIBUS A INIT, controller clear, error clear, or by loading a data transfer command with GO set. NED causes TRE. Read only.

**Bit: 11**  
**Name:** Non-Existent Memory (NEM)  
**Function:** Set when the controller is performing a DMA transfer and the memory address specified in MTBA is non-existent (does not respond to MSYN within 10μs). Cleared by UNIBUS A INIT, controller clear, error clear, or by loading a data transfer command with GO set. NEM causes TRE. The MTBA contains the address +2 of the memory location causing the error. Read only.
Bit: 10  Name: Program Error (PGE)  
Function: Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. Cleared by UNIBUS A INIT, controller clear, error clear, or by loading a data transfer command with GO set. Read only.

PGE causes TRE. The data transfer command code is inhibited from being written.

Bit: 9  Name: Missed Transfer (MXF)  
Function: Set if the drives does not respond to a data transfer command within 250 ms. Cleared by UNIBUS A INIT, controller clear, error clear, or by loading a data transfer command with GO set.

MXF causes TRE. This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive which has ERR set, or if the drive fails to initiate the command for any reason (such as a parity error). Read only.

Bit: 8  Name: Mass I/O Bus Data Bus Parity Error (MDPE)  
Function: Set when a parity error occurs on the data bus while doing a read or write-check operation. Cleared by UNIBUS A INIT, controller clear, error clear, or by loading a data transfer command with GO set.

MDPE causes TRE. Parity errors on the bus data bus during write operation are detected by the drive and cause the PAR error. Read only.

Bit: 7  Name: Output Ready (OR)  
Function: Set when a word is present in MTDB and can be read by the program. Cleared by UNIBUS A INIT, controller clear, or by reading DB.

Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to read the DB Register before OR is asserted will cause a DLT error. Read only.

Bit: 6  Name: Input Ready (IR)  
Function: Set when a word may be written in the DB Register by the program. Cleared by reading the DB.

Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to write the DB Register before IR is asserted will cause a DLT error. This bit is for diagnostic purposes only. Read only.
Bit: 5  Name: Controller Clear (CLR)
Function: When a 1 is written into this bit, the controller and all drives are initialized. UNIBUS A INIT also causes controller clear to occur. Write only.

Bit: 4  Name: Parity Test (PAT)
Function: While PAT is set, the controller generates even parity on both the control bus and data bus of the I/O bus. When clear, odd parity is generated. Cleared by UNIBUS A INIT or controller clear. While PAT is set, the controller checks for even parity received on the data bus but not on the control bus. Read/write.

Bit: 3  Name: UNIBUS Address Increment Inhibit (BAI)
Function: When BAI is set, the controller will not increment the BA Register during a data transfer. This bit cannot be modified while the controller is doing a data transfer (RDY negated). Cleared by UNIBUS A INIT or controller clear. When set during a data transfer, all data words are read from or written into the same memory location. Read/write.

Bit: 2-0  Name: Unit Select (U 2-0)
Function: These bits are written by the program to select a drive. Cleared by UNIBUS A INIT or controller clear.

The unit select bits can be changed by the program during data transfer operations without interfering with the transfer. The CS1, DS, ER, MR, FC, DT, CK, TC, and SN registers contain bits that come from the selected drive. Read/write.

Drive Status Register (MTDS) 772 452

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
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<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATA</td>
<td>ERH</td>
<td>P/I</td>
<td>MOL</td>
<td>WRL</td>
<td>EOT</td>
<td>NOT</td>
<td>USED</td>
<td>DPE</td>
<td>DRY</td>
<td>SSC</td>
<td>PES</td>
<td>SDWN</td>
<td>IOC</td>
<td>TM</td>
<td>BOT</td>
</tr>
</tbody>
</table>

Bit: 15  Name: Attention Active (ATA)
Function: Set by the drive when there is an attention condition in that drive. Cleared by UNIBUS A INIT, controller clear, drive clear, by loading a command with the GO bit set, or by loading a 1 in the MTAS Register in the bit position corresponding to the drives’ unit number. (The last two methods of clearing the ATA bit will not clear the error indicators in the drive.)
An attention condition indicates one of the following:

- the TM02 and the selected transport require servicing due to SSC (see bit 6 in this Table)
- the TM02 and the selected transport have become ready after non-data transfer operation
- at the completion of any operation with EOT asserted

**Bit: 14  Name: Error Summary (ERR)**
**Function:** Set when one or more of the error bits is set in the MTER Register of the selected drive. Cleared by UNIBUS A INIT, controller clear, or drive clear.

This bit is the logical OR of all the bits in the MTER register. It is not cleared by loading a command other than drive clear. While ERR is asserted, commands other than drive clear are not accepted by the drive. Read only.

**Bit: 13  Name: Positioning In Progress (PIP)**
**Function:** Set by the drive while the space or rewind command is under way. Cleared at the completion of the operation. Read only.

**Bit: 12  Name: Medium On-Line (MOL)**
**Function:** Set when the selected slave is loaded and the on-line switch activated. This condition is necessary for response to any commands; if GO = 1 and MOL = 0, the command is aborted and UNS and ATA are asserted. This bit is not affected by drive clear or INIT. Indicates selected slave is ready for immediate use. Any change in status of MOL will set ATA. Read only.

**Bit: 11  Name: Write Locked (WRL)**
**Function:** Set whenever a reel of tape without a write enable ring is loaded on the selected slave. This bit is not affected by drive clear or INIT. Indicates that the selected slave transport is write protected. Read only.

**Bit: 10  Name: End Of Tape (EOT)**
**Function:** Set when the EOT marker is recognized during forward tape motion. Cleared when the EOT marker is passed over during reverse tape motion. This bit is not affected by drive clear or INIT but the execution of a rewind command causes EOT to be cleared. Read only.

**Bit: 8  Name: Drive Present (DPR)**
**Function:** Always a 1. Read only.
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Bit: 7  Name: Drive Ready (DRY)
Function: Set by INIT or at the completion of a command. Cleared whenever a valid command (with the GO bit asserted) is loaded into MTCS1. Indicates that the drive is on-line and prepared to accept a command. Read only.

Bit: 6  Name: Slave Status Change (SSC)
Function: Set when any slave transport requires attention due to one of the following conditions:
  • completion of a rewind
  • power failure
  • coming on-line
  • going off-line
Cleared by INIT. Drive clear will clear this bit if the SSC condition was raised by the selected slave and no other slaves are posting SSC. Read only.

Bit: 5  Name: Phase Encoded Status (PES)
Function: Set when the selected slave is in PE mode. Cleared when the selected slave is in NRZ1 mode. This bit is not affected by drive clear or INIT. Read only.

Bit: 4  Name: Slowing Down (SDWN)
Function: Set during the period when tape motion is stopping. This bit is not affected by drive clear or INIT. Read only.

Bit: 3  Name: Identification Burst (IDB)
Function: Set in PE mode on recognition of the PE identification burst. Cleared when another command is issued, or cleared by drive clear or INIT.
In the forward direction, the bit remains set through the reading, writing or spacing operation. On a PE tape, IDB should be asserted after any tape motion operation which began from BOT. Read only.

Bit: 2  Name: Tape Mark (TM)
Function: Set when a tape mark is detected and remains set until the next tape motion operation is initiated. Cleared by INIT or drive clear. Read only.

Bit: 1  Name: Beginning Of Tape (BOT)
Function: Set when the selected slave detects the BOT marker. This bit is not affected by drive clear or INIT. Cleared
by passing BOT (Beginning of Tape) in the forward
direction. Read only.

Bit: 0  Name: Slave Attention (SLA)
Function: Set by a selected slave which requires attention due to
coming on-line. Cleared by drive clear or INIT. Read only.

Error Register (MTER) 772 454

<table>
<thead>
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<th>15</th>
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</tr>
</thead>
<tbody>
<tr>
<td>COR/</td>
<td>UNS</td>
<td>OPI</td>
<td>DTE</td>
<td>NEF</td>
<td>CS/</td>
<td>ITM</td>
<td>FCE</td>
<td>NSG</td>
<td>PEP/</td>
<td>INC/</td>
<td>VPE</td>
<td>DPAR</td>
<td>FMT</td>
<td>CPAR</td>
<td>RMR</td>
</tr>
</tbody>
</table>

Bit: 15  Name: Correctable Data Error/CRC Error (COR/CRC)
Function: PE mode—set on a tape character. Therefore, PE error
 correction logic was able to correct the data on-the-fly
and good data was transferred to memory.

NRZ mode—set when the CRC character generated
from read back data does not agree with the CRC read
from tape. Cleared by drive clear or INIT. Read only.

Bit: 14  Name: Unsafe (UNS)
Function: Set if the GO bit in the MTCS1 register is set, the MOL
bit in the MTDS register is reset, and a command code
other than drive clear is issued. It is set if the TM02
detects an imminent power fail condition (AC LO as-
serted, DC LO not asserted).

If UNS is caused by GO = 1 while MOL = 0, it is cleared
by CLR or DRIVE CLEAR. If UNS is caused by a tran-
sient voltage-low condition, it can be cleared by INIT
or drive clear when voltage returns to an acceptable
level. If UNS is caused by a permanent voltage-low
condition, it cannot be cleared. Read only.

Bit: 13  Name: Operation Incomplete (OPI)
Function: A read or space operation indicates that a tape record
has not been detected within 7 seconds from command
initiation. A write operation indicates that a read-after-
write tape record has not been detected within 0.7 sec-
onds from command initiation. Can also indicate that
NSG < 0.08 inches. Cleared by INIT or drive clear.
Read only.

Bit: 12  Name: Drive Timing Error (DTE)
**Function:** Set during a write operation if WCLK was not received from the controller in time to provide a valid tape character, or when a data transfer is attempted when the bus is already occupied (OCC = 1). Cleared by INIT or drive clear. When DTE is asserted, the drive also asserts EBL and EXC and aborts the command. Read only.

**Bit: 11  Name:** Non-Executable Function (NEF)  
**Function:** Set when:
- a write operation is attempted on a write-protect transport  
- a space reverse, read reverse, or write check reverse is attempted when the tape is at BOT  
- the DEN 2 bit in the tape control register does not agree with the PES status bit (i.e., selected drive not capable of selected density)  
- a space or write operation is attempted when FCS = 0 in the tape control register  
- a read or write operation is attempted with DEN2 = 0 in the tape control register and the twos complement of a number less than 13 is in the frame count register  
- if tape speed control modules do not agree with the drive type register, indicating that the controller/slave system is not operating at the same tape speed.

Cleared by drive clear or INIT. Read only.

**Bit: 10  Name:** Correctable Skew/Illegal Tape Mark  
**Function:** In PE mode, this bit is set when excessive but correctable skew is detected in data read back from the tape. It is a warning only, and does not indicate that bad data was read from the tape.

In NRZ mode, this bit is set when a bit pattern is detected on tape which has the general characteristics of an NRZ filemark (specifically two single character spaces) but which does not contain the exact data expected in a NRZ filemark. Cleared by drive clear or INIT. Read only.

**Bit: 9  Name:** Frame Count Error (FCE)  
**Function:** Set when a space operation has terminated and the frame counter is not cleared. Also set when the con-
troller fails to negate RUN when the TM02 asserts EBL. Cleared by drive clear or INIT. Read only.

**Bit: 8**  
**Name:** Non Standard Gap (NSG)  
**Function:** Set after a data transfer operation whenever any tape characters are read while the read head is scanning the first half of the inter-record gap. Cleared by drive clear or INIT. Read only.

**Bit: 7**  
**Name:** PE Format Error/LRC (PEF/LRC)  
**Function:** Set in PE mode when an invalid preamble or postamble is detected. Set in NRZ mode when the LRC character generated from read-back data does not match the LRC character read from tape. Cleared by drive clear or INIT. Read only.

**Bit: 6**  
**Name:** Incorrectable Data/Vertical Parity Error (INC/VPE)  
**Function:** During PE read operation, this indicates that one of the following has occurred:
- multiple dead tracks
- parity errors without dead tracks
- skew overflow
  
  During a NRZ read operation, this indicates that a vertical parity error has occurred or that data has occurred after the skew delay is over. Cleared by drive clear or INIT. Read only.

**Bit: 5**  
**Name:** Data Bus Parity Error (DPAR)  
**Function:** Set when a parity error is detected on the data lines during a write operation. Cleared by drive clear or INIT. Read only.

**Bit: 4**  
**Name:** Format Error (FMT)  
**Function:** Set when a data transfer is attempted with an incorrect format code (i.e., the tape format code loaded in the MTTC register is not implemented on that TM02). Cleared by drive clear or INIT. Read only.

**Bit: 3**  
**Name:** Control Bus Parity Error (CPAR)  
**Function:** Set when a parity error is detected on the control lines during a control bus write operation. Cleared by drive clear or INIT. Read only.

**Bit: 2**  
**Name:** Register Modification Refused (RMR)  
**Function:** Set when the controller attempts to write into any im-
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implemented TU16 register (except the maintenance register or the attention summary register) while the GO bit is asserted. If RMR occurs, the addressed register is not modified. Cleared by drive clear or INIT. Read only.

Bit: 1  
Name: Illegal Register (ILR)
Function: Set when a read or write from a non-existent register is attempted. Cleared by drive clear or INIT. Read only.

Bit: 0  
Name: Illegal Function (ILF)
Function: Set when the GO bit is asserted and a function code not implemented by the TM02/TU16 is attempted. Cleared by drive clear or INIT. Read only.

Attention Summary Register (MTAS) 772 456

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
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</tr>
</tbody>
</table>

NOT USED

Bit: 7-0  
Name: ATA 7-0
Function: Each bit sets when the corresponding drive asserts its ATA bit. All bits are cleared by UNIBUS A INIT, drive clear or controller clear. Individual bits are cleared by loading a function code with the GO bit in the corresponding drive or by writing a 1 in the ATA bit positions of this register. Writing a 0 has no effect. Read/write.

Character Check Register (MTCC) 772 460

NRZ FORMAT

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
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<tr>
<td>0</td>
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<td>CRC</td>
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</tr>
</tbody>
</table>

NOT USED

CRC CHARACTER

PE FORMAT

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>DTP</td>
<td>DTP</td>
<td>DTE</td>
<td>DTE</td>
<td>DT5</td>
<td>DT4</td>
<td>DT3</td>
<td>DT2</td>
<td>DT1</td>
<td>DT0</td>
</tr>
</tbody>
</table>

NOT USED  DEAD TRACK

Bit: 8-0  
Name: Check Character/Dead Track (CCD)
Function: Contains the CRC character and parity bit in NRZ mode or the dead track register in PE mode. Read only.
Data Buffer Register (MTDB) 774 262

Data Buffer (MTDB) Register (772462)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
DB 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Bit: 15-0  Name: Data Buffer (DB 15-0)
Function: When read, the contents of OBUF (internal register) are delivered. Upon completion of the read, the next sequential word in the Silo will be clocked into OBUF. When written, data is loaded into IBUF (internal register) and allowed to sequence into the Silo if space is available. Used by the program for diagnostic purposes. Read/write.

Maintenance Register (MTMR) 772 464

The maintenance register is a 16-bit read/write register for diagnostic testing.

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
MDF 8 MDF 7 MDF 6 MDF 5 MDF 4 MDF 3 MDF 2 MDF 1 ZOO BPI CLK MC MDF 3 MDF 2 MDF 1 MDF 0

Drive Type Register (MTDT) 772 466

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
NSA TAP MOH TCH DRQ SPR NOT USED DT 08 DT 07 DT 06 DT 05 DT 04 DT 03 DT 02 DT 01 DT 00

Bit: 15-14  Name:
Function: Always a 1.

Bit: 13  Name: Moving Head (MOH)
Function: Always a 0. Read only.

Bit: 12  Name: 7 Channel (7CH)
Function: Always a 0. Read only.

Bit: 11  Name: Drive Request Required (DRQ)
Function: Always a 0. Read only.
Bit: 10  Name: Slave Present (SPR)  
Function: Asserted when a transport is powered up and has been assigned the selection code contained in the MTTC tape control register. Read only.

Bit: 8-0  Name: Drive Type (DT 8-0)  
Function: Contains the drive type number for the selected slave. If no slave is assigned in bit 0-2 of the MTTC tape control register, the drive type code readback is 50(sub)8. Drive clear or INIT do not affect these bits. Read only.

Serial Number Register (MTSN) 772 470  
The serial number register is a 16-bit, read-only register which contains a BCD representation of the four least significant digits of the transport serial number.

Bit: 15-12  Name: (SN15-SN12)  
Function: Most significant BCD digit (10(**)3) of slave serial number. Read only.

Bit: 11-8  Name: (SN11-SN08)  
Function: 10(**)2 digit of slave serial number. Read only.

Bit: 7-4  Name: (SN07-SN04)  
Function: 10(**)1 digit of slave serial number. Read only.

Bit: 3-0  Name: (SN03-SN00)  
Function: Least significant BCD digit of slave serial number. Read only.

Tape Control Register (MTTC) 772 472

Bit: 15  Name: Acceleration (ACCL)
**Function:** Set when the transport is not actively reading or writing data. ACCL is not affected by drive clear or INIT. Read only.

**Bit: 14**

**Name:** Frame Count Status (FCS)

**Function:** Normally set at the end of a write into the frame count register. Cleared when frame count register overflows. Cleared by drive clear or INIT.

Loading a space or write command with the GO bit asserted and FCS equal to 0 will cause a nonexecutable function (NEF-bit 11 of drive status register) to be asserted and will cause the command to be aborted. No tape motion will occur. Read only.

**Bit: 13**

**Name:** Slave Address Change (SAC)

**Function:** This bit notes that a new slave has been selected. SAC will be asserted whenever the slave select bits of the TC Register are changed. The bit will stay asserted until the newly selected slave is issued a drive set pulse, initiating a command to that slave.

Set when a control bus write operation to the tape control register is performed. Cleared by the initiation of any command requiring tape motion.

TCW is used by the TM02 to determine whether or not to wait for the completion of the settled down process (SDWN-bit 4 of the drive status register). If TCW is asserted, SDWN should be negated before issuing a new command to the selected slave. Read only.

**Bit: 12**

**Name:** Enable Abort On Data Transfer Errors (EAODTE)

**Function:** This bit, when written to a 1, will cause a data transfer operation to be aborted as soon as one of the following errors is deleted:

- DPAR-bit 5 of MTER register
- COR/CRC-bit 15 of MTER register
- FMT/LRC-bit 7 of MTER register
- INC/VPE-bit 6 of MTER register

Read/write.

**Bit: 10-8**

**Name:** Density Select (DEN2-DEN0)

**Function:** Specifies the tape character density during read or write operations.
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<table>
<thead>
<tr>
<th>DEN 2</th>
<th>DEN 1</th>
<th>DEN 0</th>
<th>bpi</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>556</td>
</tr>
<tr>
<td>NRZ</td>
<td>0</td>
<td>1</td>
<td>0 or 1</td>
</tr>
<tr>
<td>800</td>
<td>1</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1600</td>
<td>PE</td>
<td></td>
</tr>
</tbody>
</table>

Drive clear and INIT do not affect the density select bits.

Density select bits are looked at only in a write operation. During a read operation, the auto density feature of the controller selects the density of the slave. During a write operation, when DEN2 = 1/600 bpi, when DEN2 = 0 the controller defaults to 800 bpi.

Bit: 7-4  Name: Format Select (FMT SEL 3-0)
Function: Specifies I/O bus-to-tape character formatting during a write operation or tape character-to-I/O bus formatting during a read operation.

If the RMT SEL bits specify a format not implemented on a TM02/TU16 system and a valid data transfer command is loaded in the MTCS1 register with the GO bit asserted, the format error bit (FMT-bit 4 of the MTER register) will be asserted and the operation will abort. Read/write.

Bit: 3  Name: Even Parity (EV PAR)
Function: If this bit is set in NRZ mode, even parity will be written on tape and will be expected on readback. If this bit is reset, odd parity will be written on tape and will be expected on readback. When the TM02 is operating in NRZ with EV PAR set, it will not allow an all zeros character to be written on tape. If an all zeros character is presented to the TM02, the TM02 will invert binary bit 4 and the parity bit before writing the character on tape. This converts 000(sub)8 to 020(sub)8.

In EP, this bit will cause parity errors. The controller will always write odd parity data, but the read circuitry is expecting even parity data.

Bit: 2-0  Name: Slave Select (SS2-0)
Function: Specifies the unit number of the transport to be used. Drive clear or INIT does not affect SS2-0. Read/write.
**SPECIFICATIONS FOR TAPE AND CONTROL**

**Main Specifications**
- **Storage medium**: ½ inch wide magnetic tape (industry standard)
- **Capacity/tape reel**: 32 million characters (at 1600 bpi)
- **Data transfer speed**: 72,000 characters/sec., max.
- **Drives/control**: 8 max.

**Data Organization**
- **Number of tracks**: 9
- **Recording density**: 800 or 1600 bits/inch, program selectable
- **Interrecord gap**: 0.50 inches, min.; 0.60 inches, nom.
- **Recording method**: NRZ1 for 800 bpi, phase encoded for 1600 bpi

**Tape Motion**
- **Read/write speed**: 45 inches/sec.
- **Rewind speed**: 150 inches/sec.
- **Rewind time**: 3 minutes, typical

**Tape Characteristics**
- **Length**: 2,400 feet, max.
- **Type**: Mylar base, iron-oxide coated
- **Reel diameter**: 10½ inches, max.
- **Handling**: Direct-drive reel motors, servo-controlled single capstan, vacuum tape buffer columns with constant tape winding tension

**Mechanical**
- **Mounting**: Tape drive and master tape electronics mount in a standard PDP-11 cabinet (supplied); control unit is 2 system units (mounts in a separate assembly)

**Size**
- **31-inch front panel height for drive and master electronics**

**Weight**
- **500 lbs. (including cabinet)**

**Cable length**
- **80 feet (max.) for total tape system (control unit to furthest drive)**

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TE16

Power
Tape drive current  8A at 115 Vac
Surge current  85A at 115 Vac
Current for control  16A at +5V; 0.6A at −15V
Heat dissipation  900W

Environment
Operating temperature  15°C to 32°C
Relative humidity  20% to 80%, max. wet bulb 25°C

Miscellaneous
BOT, EOT detection  Photoelectric sensing of reflective strip, industry compatible
Skew control  Deskewing electronics included in tape transport to eliminate static skew
Write protection  Write-protect ring sensing on tape transport
Data checking  Read-after-write parity checking of characters; Longitudinal Parity Check, and Cyclic Redundancy Check at 800 bpi

Testing
Off-line exerciser included in tape drive electronics; on-line check of control data paths accomplished by diagnostics

Reading
Data can be read in forward or reverse direction

Error correction
(Phase-encoding only), on-the-fly error correction for a single-track dropout

Magnetic head
Dual-gap, read-after-write

SPECIFICATIONS FOR TAPE DRIVE (TE16)

Mechanical
Mounting  Mounts in a standard PDP-11 cabinet (supplied)
Size  26-inch front panel height
FEATURES
- high reliability
- low cost
- small size
- low power consumption

DESCRIPTION
The TS03 is a low-cost, 9-track magnetic tape system that uses industry-standard 800-bpi NRZI recording format. The basic system consists of a master tape drive, a controller and a power supply. A second tape drive can be added for only the cost of the tape drive since the second drive (slave) uses the master drive’s controller and power supply.

Cost saving results from small size because the TS03 frequently fits into existing cabinets. The TS03 with controller can fit into a processor cabinet with spare room left over for another subsystem.

Small size also means lower power consumption because:
MAGNETIC TAPES

TS03

- there is no vacuum motor.
- the TS03 uses very low standby power—about the same as a medium-sized light bulb.
- less power is required to drive the TS03's seven-inch diameter reels.
- lower power consumption means a smaller load if back-up generator or batteries are used.
- heat dissipation is so low that no cooling fans are needed.

The TS03 is a 9-track, 800 bpi magnetic tape drive. Each tape drive is a self-contained unit including read and write electronics, low inertia friction capstan and two linear-drive reel servos. The reel servos use mechanical servo arms for controlling the tape storage loops. Magnetic arm transducers are employed to sense the arm position and control tape tension. The linear servos provide gentle tape handling to prolong tape life.

The recording head assembly includes an open-loop tape path with single edge guiding, tape cleaner, EOT/BOT station and a 9-track read-after-write head. The recorder has a transparent plastic door enclosing the tape path and recording area to allow viewing while still excluding airborne dust.

The 7-inch diameter tape reel is mounted on a quick-release tape hub. A fixed tape-up hub is provided and does not require a separate tape reel.

The master drive is mounted on slides and occupies 10 1/2-inches of panel height in a standard DIGITAL cabinet.

The master drive includes portions of controller circuitry (adapted on a printed circuit board) mounted beneath the drive mechanism enclosure. The board is hinged to facilitate access for servicing and maintenance.

Reliability
The TS03 is designed to read and write data to industry standards with high reliability. The calculated MTBF (Mean Time Between Failures) is 5,080 hours for the tape drive.

A unique feature of the TS03 eliminates the writing of hard errors on tape. If an error is detected in the read-after-write check, programming can cause the entire record to be rewritten. Hardware within the TS03 automatically senses that this is a re-try and the read-checking margins are tightened up to ensure distinguishing between a transient error and a bad tape area. If the data passes
on a second (or subsequent) try, the written data is guaranteed to exceed the read thresholds. If there was a bad section of tape, faulty record can be erased, then recorded correctly further down the tape.

**Master Controller Functions**
The TS03 master controller performs the following tasks:

**Tape Format**
A Cyclic Redundancy Check character is generated on write data passing to the TS03 and is strobed onto tape. This CRC character is generated in accordance with the ANSI standard for 800-bpi NRZI recording. A Longitudinal Redundancy Check character is also written on the tape.

An industry-compatible tape mark is generated when a write Tape Mark instruction (also known as write EOF or Write File Mark) command is in progress.

**Record Detection**
Once tape motion has been initiated on a tape transport, motion will not be halted until either a valid record is detected or the initialize signal is given.

**Data Checking**
A vertical parity bit is attached to each data character written. Whenever the TS03 is moving at tape read/write speed, it checks data for correct vertical parity and a correct Longitudinal Redundancy Check character for each record read.

The TS03 also contains logic for detecting industry compatible tape marks (END-OF-FILE mark).

**REGISTERS**
**Status Register (MTS) 772 520**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>Illegal Command</td>
<td>Set by any of the following illegal commands.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Any DATO or DATOB to the Command Register MTC during the tape operation period</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A write, write EOF, or write with extended IRG operation when the FILE PROTECT bit is a 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A command to a tape unit whose SELECT REMOTE bit is a 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The SELECT REMOTE (SELR) bit becoming a 0 during an operation</td>
</tr>
</tbody>
</table>

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In error conditions 1 through 3, the command is loaded into the MTC, but the GO pulse to the tape unit is not generated. In addition the CU ready bit remains set.

**Bit: 14  Name:** End of File (EOF)

**Function:** Set when an EOF character is detected during a read, space forward or space reverse operation. During the read or space forward operation, the EOF bit is set when the LPC (longitudinal parity check) character following the EOF character is read. During a space reverse operation, the EOF bit is set when the EOF character following its LPC character is read. The ERR bit sets when the LPC character strobe is generated with the FILE MARK signal upon EOF detection.

**Bit: 13  Name:** Cyclical Redundancy Error (CRE)

**Function:** Detected only during a read operation. It compares the CRC character read from tape with that regenerated during the same read operation. If they are not the same, CRC ERROR from the tape unit becomes a 1 until the LPC character is detected.

**Bit: 12  Name:** Parity Error (PAE)

**Function:** The OR of the lateral and longitudinal parity errors. A lateral parity error is indicated on any character in the record while a longitudinal parity error occurs only when the LPC character is detected.

A parity error does not affect the transfer of data; that is, in a write operation, the entire record is transferred
to tape and in a read operation, the entire record is written into memory.

For all parity errors, the ERR bit sets only when the LPC character is detected. Both lateral and longitudinal parity errors are detected during a read, write, write EOF, and write with extended IRG operations. The entire record is checked, including the CRC and LPC characters. Longitudinal parity error occurs when an odd number of ones is detected on any track in the record. A lateral parity error occurs when an even number of ones is detected on any character when PEVN is a 0, or an odd number of ones is detected on any character when PEVN is a 1.

Bit: 11  Name: Bus Grant Late (BGL)

Function: Set when the control unit, after issuing a request for the bus, does not receive a bus grant before the control unit receives the bus request for the following tape character. The condition is tested only for NPR (non-processor request) operations. The ERR bit sets simultaneously with BGL, thus terminating the operation. If the BGL occurred during a write or write with extended IRG operation, the control unit does not send the signal WDS to the master, while the master writes the CRC character (if required) and LPC character onto the tape, terminating the record.

Bit: 10  Name: End of Tape (EOT)

Function: Set when the EOT marker is read while the tape is moving in the forward direction. The bit is cleared as soon as the same point is read while the tape is moving in the reverse direction. The ERR bit, as a result of the EOT bit at a 1, sets only in the tape forward direction and coincidentally with the reading of an LPC character.

Bit: 9  Name: Record Length Error (RLE)

Function: Detected only during a read operation. It occurs for long records and is indicated as soon as MTBRC increments beyond 0, at which time both data transfer into memory, and incrementing of the MTCMA and MTBRC stop. However, the control unit reads the entire record and sets the ERR bit when the LPC character is read. CU ready remains at 0 until the LPC character is read.
Bit: 8  Name: Bad Tape Error (BTE)
Function: Sets when a character is detected (RDS pulse) during the gap shut-down or settling down period for all operation (except rewind). When BTE is detected, the ERR bit is set immediately, and if INT ENB is set, an interrupt sequence is started.

Bit: 7  Name: Non-Existent Memory (NXM)
Function: Set during NPR operations when the control unit is bus master and is performing data transfers into and out of the bus when the control unit does not receive a slave SYNC signal within 10 microseconds after it has issued a master sync signal. The operations which occur when the error is detected are identical to those indicated for the BGL error.

Bit: 6  Name: Select Remote (SELR)
Function: Cleared when the tape unit addressed does not exist, is off-line, or has its power turned off.

Bit: 5  Name: Beginning 0f Tape (BOT)
Function: Set when the BOT marker is read, and cleared when the BOT marker is not read. BOT at a 1 does not produce a 1 in the ERR bit.

Bit: 4  Name: Seven Channel (7 CH)
Function: Set to indicate a 7-channel tape unit; cleared to indicate a 9-channel unit.

Bit: 3  Name: Tape Settle Down (SDWN)
Function: Set whenever the tape unit is slowing down. The master will accept and execute a new command during the SDWN period, unless the new command is to the same tape unit as the one issuing SDWN and if the direction implied in the new command is opposite to the present direction.

Bit: 2  Name: Write Lock (WRL)
Function: Set to prevent the control unit from writing information on tape. Controlled by the presence or absence of the write protect ring on the tape reel.

Bit: 1  Name: Rewind Status (RWS)
Function: Set by the master as soon as it receives a rewind command from the control unit. Cleared by the master as soon as the tape arrives at the BOT marker in the
forward direction. (It overshoots BOT in the reverse direction.)

Bit: 0  Name: Tape Unit Ready (TUR)
Function: Set when the selected tape unit is stopped and when
the SELECT REMOTE is false. Cleared when the pro-
cessor sets the GO bit and the operation defined by
the function bit occurs.

Command Register (MTC) 772 522

```
  15 14 13 12 11  10  9  8  7  6  5  4  3  2  1  0

   ERROR       DENSITY
   POWER CLEAR  LATERAL PARITY
   UNIT SELECT  C U READY
   INTERRUPT ENABLE
   ADDRESS BITS
   FUNCTION
   GO
```

Bit: 15  Name: Error (ERR)
Function: Set as a function of bits 7-15 of the Status Register
MTS. Cleared on INIT or on the GO command to the
tape unit.

Bit: 14-13  Name: Density (DEN 8, DEN 5)
Function: Cleared on INIT.

<table>
<thead>
<tr>
<th>Bit 14</th>
<th>Bit 13</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>200 bpi</td>
</tr>
<tr>
<td>0</td>
<td>556 bpi</td>
</tr>
<tr>
<td>1</td>
<td>800 bpi</td>
</tr>
<tr>
<td>1</td>
<td>800 bpi</td>
</tr>
</tbody>
</table>

Bit: 12  Name: Power Clear (PCLR)
Function: Provides the means for the processor to clear the con-
trol unit and tape units without clearing any other de-
vice in the system. The PCLR bit is always read back
by the processor as 0.

Bit: 11  Name: Lateral Parity (PEVN)
Function: Set for even parity. Cleared for odd parity. A search
for parity error is made in all tape moving operations
except space forward, space reverse, and rewind.

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**Bit: 10-8**  **Name:** Unit Select  
**Function:** Specifies one of the eight possible magnetic tape units. All operations defined in the MTC and all status conditions defined in the MTS pertain to the unit indicated by these bits. Cleared on INIT.

**Bit: 7**  **Name:** CU Ready (CUR)  
**Function:** Cleared at start of a tape operation and set at end of tape operation. The control unit accepts as legal all commands it receives while the CU Ready bit is 1.

**Bit: 6**  **Name:** Interrupt Enable (INT ENB)  
**Function:** When set, an interrupt occurs whenever either the CU Ready bit or the ERR bit change from 0 to 1 or whenever a tape unit that was set into rewind has arrived at the beginning of tape. In addition, an interrupt occurs on an instruction that changes the INT ENB from 0 to 1 and does not set the GO bit (i.e., CU READY or ERROR = 1).

**Bit: 5-4**  **Name:** Address Bits  
**Function:** Extended memory bits for an 18-bit bus address. Bit 5 corresponds to XBA17, and bit 4 to XBA16. They are an extension of the MTCMA, and increment during a tape operation if there is a carry out of MTCMA.

**Bit: 3-1**  **Name:** Functions Bits  
**Function:** Selects 1 of 8 functions (programmable commands).

<table>
<thead>
<tr>
<th>BIT 3</th>
<th>BIT 2</th>
<th>BIT 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off line</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Read</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Write</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Write EOF</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Space Forward</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Space Reverse</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Write with Extended</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Interrecord Gap</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Rewind</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Bit: 0  Name: Go
Function: When set, begins the operation defined by the function bits.

Byte Record Counter (MTBRC) 772 524
The MTBBRC is a 16-bit binary counter which is used to count bytes in a read, write, or write with extended IRG operation, or records in a space forward or space reverse operation. When used in a write or write with extended IRG operation, the MTBRC is initially set by the program to the twos complement of the number of bytes to be written on tape. The MTBRC becomes 0 after the last byte of the record has been read from memory. Thus, when the next WDS (Write Data Strobe) signal occurs from the master, the control unit will not send the WDR (Write Data Request) to the master indicating that there are no more data characters in the record.

When the MTBRC is used in a read operation, it is set to a number equal to or greater than the twos complement of the number of words to be loaded into memory. A record length error (RLE) occurs for long records only, and is indicated when a read pulse for data (RDS occurring when CRCS or LPCS does not occur) occurs when the MTBRC is 0. The MTBRC increments by 1 immediately after each memory access.

When the MTBRC is used in a space forward of space reverse operation, it is set to the twos complement of the number of records to be spaced. It is incremented by a 1 at LPC time, whether the tape is moving in the forward or reverse direction. A new GO pulse is sent to the tape unit during the SDWN time if the MTBRC is not 0 during that time. When the tape unit is moving in reverse, the LPC character is detected before SDWN, but before the entire record has been traversed. Thus, both SDWN and LPC characters appear to be in different positions on tape from those when the tape unit is moving forward.

Current Memory Address Register (MTCMA) 772 526
The MTCMA contains 16 of the possible 18 memory address bits. It is used in NPR operations to provide the memory address for data transfers in read, write, and write with extended IRG operations. Prior to issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a read operation, or from which the first byte is read in a write or write extended IRG operation. The MTCMA is incremented by 1 immediately after each memory access. Thus, at any instant of time, the MTCMA points to the next higher address than the one which
had most recently been accessed. When the entire record has been transferred, the MTCMA contains the address plus 1 of the last character in the record. In the error conditions Bus Grant Late (BGL) and Non-Existent Memory (NXM), the MTCMA contains the address of the location in which the failure occurred.

The MTCMA is available to the processor on a DATI, except bit 0 which always reads as a zero under program control. Bit 0 can be asserted during NPRs to determine the selected byte. The bits are set or cleared on a processor DATO. INIT clears all bits in the MTCMA.

**Data Buffer (MTD) 772 530**
The data buffer is an 8-bit register which is used during a read, write, or write with extended IRG operation. In a read operation, the data buffer is a temporary storage register for characters read from tape before being stored into memory. In a processor read, all nine bits are stored into memory. Bits 0 through 7 in memory correspond to channels 7 through 0 respectively from tape, and bit 8 corresponds to the parity bit. In an NPR operation, only the data bits are read into memory and are alternately stored into the low and high bytes. In a write or write with extended ERG operation, the data buffer is a temporary storage register for characters read from core memory before they are written on tape. The polarity of the parity bit is determined by the PEVN bit in the MTC.

In a read operation, the LPC character enters the data buffer when bit 14 or MTRD is a 1, and inhibited from doing so when 14 is a 0. Thus, after reading a nine-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the CRC character when bit 14 is a 0. After reading a seven-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the last data character when bit 14 is a 0. After reading an EOF character, the date buffer contains all zeros when bit 14 is a 1 and the LPC character when bit 10 is 0. The MTD is available to the processor on a DATI. Bits 9 through 15 read identically to bits 1 through 7 respectively. Bits 0 through 7 are set or cleared on a processor DATO. Bits 8 through 15 are not affected by the processor DATO. INIT clears all bits in the MTD.

**TE10 Read Lines (MTRD) 772 532**
The memory locations allocated for the TE10 read lines are:

- Bits 0-7 for the channels 7-0 respectively.
- Bit 8 for the parity bit.
- Bit 12 for the gap shutdown bit.
Bit 13 for the BTE error generation.
Bit 14 for the CRC, LPC character selector.
Bit 15 for the timer.

For correct longitudinal parity, bits 0-8 are 0 after writing a record or reading a record from tape. For a longitudinal parity error, one or more of the bits 0-8 remains at a 1; the bit(s) at a 1 indicating the channel(s) containing the error which sets the CU Ready bit. Thus, if the pulse is set during a tape operation, CU Ready sets prematurely, thus producing the gap shutdown period when characters are still being read. Bits 0-8 are set and cleared by the tape unit. Bit 13 is a pulse generated by the processor. Bit 14 is set and cleared by the processor and cleared by INIT. Bit 15 is uniquely controlled by the 100- microsecond timer. The MTRD is available to the processor on a DATI except that bit 13 reads back as a 0.

**Timer**
TIMER is a 10 KHz signal with a 50% duty cycle. The signal is used for diagnostic purposes in measuring the time duration of the tape operations. The timer is read as bit 15 in the MTRD.

**SPECIFICATIONS FOR TS03 DRIVE**
**Main Specifications**
Storage medium
1/2-inch wide magnetic tape (industry compatible)
Capacity/tape reel
5 million characters
Data transfer speed
10,000 char/sec
Drives/control, max
2

**Data Organization**
Number of tracks
9
Recording density
800 bits/inch
Inter-record gap
0.5 inches, min
Recording method
NRZI

**Tape Motion**
Read/write speed
12 1/2-inches/sec
Rewind time
1 minute, max
Tape drive
Single capstan
Reel braking
Dynamic servo control
Speed variation
3% instantaneous, 1% long term

261
<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Start/stop distance</strong></td>
<td>0.19 inch</td>
</tr>
<tr>
<td><strong>Start/stop time</strong></td>
<td>30 msec</td>
</tr>
<tr>
<td><strong>Tape Characteristics</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Length</strong></td>
<td>600 ft.</td>
</tr>
<tr>
<td><strong>Type</strong></td>
<td>Mylar base, iron-oxide coated</td>
</tr>
<tr>
<td><strong>Reel diameter</strong></td>
<td>7 inches</td>
</tr>
<tr>
<td><strong>Mechanical</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Mounting</strong></td>
<td>Mounts on slides in a standard 19-inch cabinet</td>
</tr>
<tr>
<td><strong>Size</strong></td>
<td>10 1/2-inch front panel height</td>
</tr>
<tr>
<td><strong>Weight</strong></td>
<td>34 lbs.</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Input current</strong></td>
<td>1A at 90 to 132Vac, or 0.5A at 180 to 240Vac</td>
</tr>
<tr>
<td><strong>Heat dissipation</strong></td>
<td>100W</td>
</tr>
<tr>
<td><strong>Environmental</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Operating temperature</strong></td>
<td>15°C to 32°C</td>
</tr>
<tr>
<td><strong>Relative humidity</strong></td>
<td>20% to 80%, with max wet bulb 25°C and min dew point 2°C</td>
</tr>
<tr>
<td><strong>Altitude</strong></td>
<td>10,000 feet</td>
</tr>
<tr>
<td><strong>Miscellaneous</strong></td>
<td></td>
</tr>
<tr>
<td><strong>BOT, EOT detection</strong></td>
<td>Photoelectric sensing of reflective strip, industry compatible</td>
</tr>
<tr>
<td><strong>Magnetic head</strong></td>
<td>Dual gap, read after write, 0.15-inch gap</td>
</tr>
<tr>
<td><strong>SPECIFICATIONS FOR CONTROL</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Main Specifications</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Storage medium</strong></td>
<td>1/2” wide magnetic tape (industry compatible)</td>
</tr>
<tr>
<td><strong>Capacity/tape reel</strong></td>
<td>5 to 20 million characters</td>
</tr>
<tr>
<td><strong>Data transfer speed</strong></td>
<td>36,000 char/sec</td>
</tr>
<tr>
<td><strong>Drives/control, max</strong></td>
<td>8</td>
</tr>
<tr>
<td><strong>Data Organization</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Number of tracks</strong></td>
<td>7 or 9</td>
</tr>
<tr>
<td></td>
<td>262</td>
</tr>
</tbody>
</table>
MAGNETIC TAPES

Recording density
7-track—200, 556, or 800 bits/inch; program selectable
9-track—800 bits/inch

Interrecord gap
7-track—0.75 inches, min.
9-track—0.50 inches, min.

Recording method
NRZI

Tape Motion
Read/write speed
45 inches/sec
Rewind speed
150 inches/sec.
Rewind time
3 minutes, typ

Tape Characteristics
Length
2,400 ft.
Type
Mylar base, iron-oxide coated
Reel diameter
10 1/2 inches
Handling
Direct-drive reel motors, servo-controlled single capstan, vacuum tape buffer changers with constant type winding tension.

Register Addresses
Status
772 520
Command
772 522
Byte Record Counter
772 524
Current Memory Address
772 526
Data Buffer
772 730
Read Lines
772 532

UNIBUS Interface
Interrupt vector address
224
Priority level
BR5
Data transfer
NPR
Bus loading
1 bus load

Mounting
1 System Unit (SU)

Power
5A at +5V
DESCRIPTION
The TU45 tape system is a MASSBUS compatible versatile tape drive system consisting of a tape controller and the TU45 tape transport. The subsystem records and reads digital data in industry standard PE or NRZI mode at a maximum data transfer rate of 120,000 tape characters per second. Tape density and tape character format are program selectable. Forward/reverse tape speed is 75 in/sec, while rewind is performed at 250 in/sec.

The TJU45 master tape system includes a control unit, the master tape control electronics, and the first tape drive, all supplied in a standard cabinet. The system is used with the PDP 11/34-11/60 series. The controller consists of two system units. One control unit can handle up to eight tape drives.

The TWU45 master tape system like the TJU45 includes a control unit plus the master tape control electronics, and the first tape drive. It is specifically designed for use with one PDP-11/70. The control unit is housed in prewired module slots in the PDP-11/70 backplane. The controller can handle up to eight tape drives. Except for the control units, the TJU45 and the TWU45 are identical.

Data Organization
Each vertical frame of the 9-track tape represents one character and contains eight data bits plus one parity bit. Since the 16-bit PDP-11 word contains two 8-bit bytes, one byte corresponds to one tape character for efficient data storage.

Groups of characters form a record. The industry standard has 18 to 2048 characters in a single record. Each record block is separated by an Interrecord Gap (IRG) that is minimum distance of one-half inch.

Parity is checked character-by-character when reading and writing on tape to verify the accuracy of the data transfer. With NRZI, there is also a Cyclic Redundancy Check (CRC) character generated or checked at the end of each record, plus a Longitudinal Parity Check (LPC) character. If an error is detected, and error indication is made.

Operation
Reading can be performed while tape is moving in the forward or reverse direction, but writing occurs only in the forward direction. The control unit can move the tape to new positions in forward or reverse and also monitors tape operation. Interrupts are generated when processor attention is required, or when an error occurs.
Tape motion is controlled by a vacuum column and a servo capstan. The half-inch Mylar-base is coated on one side with an iron oxide composition. The load and end points of the tape are marked by reflective strips which are detected by photo diodes. Approximately 10 feet of blank tape are wound on a reel, preceding the Beginning of Tape (BOT) and End of Tape (EOT) strips. A gap of about three inches is left from the load point before writing can begin, with NRZI. With PE, an identification burst (IDB) is written in this gap.

The tape drive can be controlled locally by the control panel. Local (off-line) controls are: On-Line/Off Line, Rewind, Unit Select, and Load. When on-line, program commands accepted by the transport are: Rewind and Unload, Read Forward, Read Reverse, Write, Write Tape Mark, Space Forward, Space Reverse, Erase, and Rewind to BOT.

There is provision to prevent accidental writing on a particular tape reel. An industry-standard, write-protect ring on the reel is sensed by the tape drive.

**Reliability**

Data reliability of the TU45 tape system is enhanced by the 1600 bits per inch, phase-ending, self-clocking feature which is not dependent on precise tape skew control. In addition, the 800 bits per inch NRZI mode includes an immediate read-after-write check. The written data is checked to ensure that it far surpasses the minimum allowable reading level.

Bad tape error problems are minimized by a “runaway timer” which allows the system to recover from bad tape sections on the reel. If no reading of writing is performed within a tape distance of approximately 25 feet, tape movement will stop and an error will be indicated. Data will not be acknowledged as comprising a data block unless there are at least 12 characters in the block.

**Controller**

The MASSBUS controller, in conjunction with the tape system, provides a fast and reliable mass storage system that can be employed in timesharing or real-time data storage applications. The following major functions are performed by the controller:

- interfaces with one or two UNIBUS cables and signals
- communicates directly with the main memory to fetch and store data
MAGNETIC TAPES

TU45

- communicates with the central processor to receive commands, provides error and status information, and generates interrupts
- interfaces with one to eight tape controllers

The control is divided into two major functional groups: the register access control path, and the DMA (direct memory access) data path. The register access control path allows the program to read from or write into any register contained in the controller or in the selected tape drive. There are a total of four registers in the MASSBUS controller, nine registers in each tape controller, and one shared register.

The DMA data path functionally consists of a 66-word by 18-bit first-in, first-out memory and associated control logic. The major function of this memory, referred to as the Silo, is to buffer data to compensate for fluctuations in NPR latency time on the UNIBUS.

Figure 6-1 TU45 System
Register Access Control Path
When a PDP-11 instruction address the MASSBUS controller to read or write any device register in the controller or in the drive, a UNIBUS cycle is initiated and this data is routed to or from the controller. If the register to be addressed is local (contained within the controller), the register control logic immediately gates the data to or from the appropriate register.

REGISTERS
Fourteen 16-bit registers are used to interface the MASSBUS controller to the TU45 tape subsystem. These registers are loaded and read under program control via UNIBUS A, figure X-X, the control part of the MASSBUS controller. Data may be transferred over a second UNIBUS, (UNIBUS B). The tape system is monitored by status and error indicators in these registers. Four of the fourteen registers are located entirely in the MASSBUS controller, nine are located in the tape drive controller. The fourteenth register is shared by both controllers.

Control and Status Register (MTCSI) 772 440
This read/write register is used to store tape commands and operational status.

![Diagram of the Control and Status Register](image)

### Bit: 15  Name: Special condition 15  
**Function:** (SC)  
Read only  
Set by TRE, ATTN, or MASSBUS control parity error. Cleared by UNIBUS INIT, controller clear, or by removing the ATTN condition.

### Bit: 14  Name: Transfer error (TRE)  
**Function:** Set by DLT, WCE, PE, NED, NEM, PGE, MXF, MDPE, or a drive error during a data transfer. Cleared by
UNIBUS INIT, controller clear, controller error clear, or by loading a data transfer command with GO set.

**Bit: 13**  
**Name:** MASSBUS control bus parity error (MCPE)  
Read only  
**Function:** Parity errors that occur on the MASSBUS control bus while writing a drive register are detected by the drive and cause the PAR error (MTER register, bit 3) to set.

**Bit: 12**  
**Name:** Not used.  
**Function:** Always read as a 0.

**Bit: 11**  
**Name:** Drive available (DVA)  
Read only  
**Function:** Used in dual port drive applications.

**Bit: 10**  
**Name:** Not used  
**Function:** Always read as a 0.

**Bit: 9**  
**Name:** A17  
**Function:**

**Bit: 8**  
**Name:** A16  
UNIBUS Address  
Read/write  
**Function:** Upper extension bit of the MTBA register. Cleared by UNIBUS INIT, controller clear or by writing 0s in these bit positions.

**Bit: 7**  
**Name:** Ready (RDY)  
Read only  
**Function:** Indicates controller status. When set, the controller will accept any command. When cleared, the controller is performing a data transfer command and will allow only non-data transfer commands to be executed.

**Bit: 6**  
**Name:** Interrupt enable (IE)  
Read/write  
**Function:** A program-controlled interrupt may occur by writing is into IE and RDY at the same time. This bit can be set/cleared through the MTCS2 register.

**Bit: 5**  
**Name:** F4—F0 and GO bit  
Read/write  
**Function:** F4—F0 are function (command) code control bits that determine the action to be performed.
### Magnet Tapes

<table>
<thead>
<tr>
<th>F4</th>
<th>F3</th>
<th>F2</th>
<th>F1</th>
<th>F0</th>
<th>GO</th>
<th>Function</th>
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<tbody>
<tr>
<td>01</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>03</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>07</td>
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<td>1</td>
<td>1</td>
<td>1</td>
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<td>1</td>
</tr>
</tbody>
</table>

**Bit:** Name: The Go bit (MTCS1, bit 0) must be set to cause the controller or drive to respond to a command. The GO bit is reset by the drive at the end of the operation. Cleared by UNIBUS INIT or controller clear (will about command execution in all drives).

**Word Count Register**  772 422

**Bit: 15-0** Name: Word count (WC)

**Function:** Set by the program to specify the number of words to be transferred (2’s complement form). This register is cleared only by writing 0s into it. Incremented for each word transferred to or from memory.

Read/write

**Bus Address Register**  774 444

**Bit: 15-1** Name: BA 15-1

01 Bus address

Read/write

**Function:** Loaded by the program to specify the starting memory address to a transfer. Cleared by UNIBUS INIT or by controller clear.

The MTBA register is incremented or decremented by 4 for each double data word transferred to or from memory. For single-word operation, the register is incremented or decremented by 2.

**Bit: 0** Name: Not used.

**Function:** Always read as a 0.
Frame Count Register  772 446
The frame count register is a 16-bit, read/write register that counts tape events. During a data transfer operation (read/write), this register is incremented each time a tape character is transferred to or from the tape. However, during a space operation, this register is incremented each time a record is detected. The register output may be read by the controller at any time, but the controller can only write into this register when the transport is not performing a space or data transfer (GO negated).

Bit: 15-0  Name: FC 15-0 Frame count
Read/write

Function:  Cleared by writing 0s in the bit locations.
Designates in 2's complement from the number of records to be spaced over, characters to be written, or characters that have been read. Initiating a write or space command when the frame count register is loaded with zeros implies a count of 1(∗)16.

Control and Status 2 Register  722 450
This register indicates The Status of the Controller; and contains the drive unit number. The unit number specified in bits 2 through 0, indicates which drive is responding when registers are addressed that are located in a drive.

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATA LATE</td>
<td>WRITE CHECK ERROR</td>
<td>UNIBUS PARITY ERROR</td>
<td>NON-EXISTANT DRIVE</td>
<td>NON-EXISTANT MEMORY</td>
<td>PROGRAM ERROR</td>
<td>MISSED TRANSFER</td>
<td>MASSBUS DATA BUS</td>
<td>OUTPUT READY</td>
<td>INPUT READY</td>
<td>CONTROLLER CLEAR</td>
<td>PARITY TEST</td>
<td>UNIBUS ADDRESS</td>
<td>UNIBUS SELECT</td>
<td></td>
</tr>
</tbody>
</table>

Bit: 15  Name: Data late (DLT)

Functions: Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write-check operation at the time the drive demands a transfer.

Read only
Bit: 14  Name: Write check error (WCE)
Function: Set when the controller is performing a write-check operation and a word on the tape does not match the corresponding word in memory.
          Read only

Bit: 13  Name: Parity error (PE)
Function: Set is a data parity error from memory is detected while the controller is performing a write or write-check command.
          Read/write

Bit: 13  Name: Non-existent drive (NED)
Function: Set when the program reads or writes a drive register.
          Read only

Bit: 11  Name: Non-existent memory (NEM)
Function: Set when the controller is performing a data transfer and the memory address specified in MTBA and MTBAE is non-existent.
          Read only

Bit: 10  Name: Program Error (PGE)
Function: Set when the program attempts to initiate a data transfer operation while the controller is currently performing one.
          Read only

Bit:  9  Name: Missed transfer (MXF)
Function: Set if the drive does not respond to a data transfer command within 650 us. Read/write

Bit:  8  Name: MASSBUS data bus parity error (MDPE)
Function: Set when a parity error occurs on the MASSBUS data bus while doing a read or write-check operation.
          Read only.

Bit:  7  Name: Output ready (OR)
Function: Set when a word is present in the MTDB register and can be read by the program. Serves as a status indicator for diagnostic check of the data buffer. Read only

Bit:  6  Name: Input ready (IR)
Function: Set when a word is written in the MTDB register by
the program. Serves as a status indicator for diagnostic check of the data buffer.
Read only

**Bit: 5**  
**Name:** Controller clear (CLR)  
**Function:** When a 1 is written into this bit, the controller and all drives are initialized.

**Bit: 4**  
**Name:** Parity test (PAT)  
**Function:** While PAT is set, the controller generates even parity on both the control bus and data bus of the MASS-BUS. When clear, old parity is generated. Read/write

**Bit: 3**  
**Name:** Unibus address incremented inhibit (BAI)  
**Function:** When set during a data transfer, all data words are read from or written into the same memory location. Read/write

**Bit: 2-0**  
**Name:** Unit select  
**Function:** These bits are written by the program to select a drive. Read/write

**Drive Status Register  772 452**  
This register contains the various status indications of the selected drive. The status indicators displayed are those of the type drive specified by the unit select bits of the MTCS2 register. This is a read only register.

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
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<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
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</thead>
<tbody>
<tr>
<td>CORRECTABLE DATA</td>
<td>CRC ERROR</td>
<td>UNSAFE</td>
<td>OPERATION INCOMPLETE</td>
<td>DRIVE TIMING ERROR</td>
<td>NON EXECUTABLE FUNCTION</td>
<td>CORRECTABLE SKEW ILLEGAL TAPE MARK</td>
<td>FRAME COUNT ERROR</td>
<td>NON STANDARD GAPS</td>
<td>PE FORMAT LRC</td>
<td>INCORRECTABLE DATA VERTICAL PARITY ERROR</td>
<td>DATA BUS PARITY ERROR</td>
<td>FORMAT ERROR</td>
<td>CONTROL BUS PARITY</td>
<td>REGISTER MODIFICATION REFUSED</td>
<td>ILLEGAL REGISTER</td>
</tr>
</tbody>
</table>

**Bit: 15**  
**Name:** Attention active (ATA)  
**Function:** Set by the drive when there is an attention condition in that drive.
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Read only

Bit: 14  Name: Error summary (ERR)
Function: This bit is the logical OR of all the bits in the MTER register. This bit is not cleared by loading a command other than drive clear. While ERR is asserted, commands other than drive clear are not accepted by the drive.
Read only

Bit: 13  Name: Positioning in progress (PIP)
Function: Set by the drive while the space or rewind command is under way. Cleared at the completion of the operation.
Read only

Bit: 12  Name: Medium on-line (MOL)
Function: Indicates selected slave is ready for immediate use. Any change in status of MOL will set ATA.
Read only

Bit: 11  Name: Write locked (WRL)
Function: Set whenever a reel of tape without a write enable ring is loaded on the selected slave. Indicates that the selected slave transport is write protected.
Read only

Bit: 10  Name: End of tape (EOT)
Function: Set when the EOT marker is recognized during forward tape motion. Cleared when the EOT marker is passed over during reverse tape motion.
Read only

Bit: 9  Name: Not used

Function: Check on

Bit: 8  Name: Drive present (DPR)
Function: This bit is a hardwired 1.
Read only

Bit: 7  Name: Drive ready (DRY)
Function: Indicates that the drive is on-line and prepared to accept a command. It does not necessarily indicate that the slave is ready to accept a command.
Read only

Bit: 6  Name: Slave Status change (SSC)
Function: Set when any slave transport requires attention due to one of the following conditions: completion of a rewind, power failure, coming on-line, going off-line.
Read only

Bit: 5 Name: Phase encoded status (PES)
Function: Reflects the format mode in which the formatter is operating.
Read only

Bit: 4 Name: Slowing down (SDWN)
Function: Set during the period when tape motion is stopping.
Read only

Bit: 3 Name: Identification burst (IDB)
Function: In the forward direction, the bit remains set through the reading, writing, or spacing operation.
Read only

Bit: 2 Name: Tape mark (TM)
Function: Indicates detection of tape mark. The phase encoded tape mark written by the TU45 consists of 40 characters with zeros in physical tracks 1, 2, 4, 5, and 8 with tracks 3, 6, 7, 9 dc erased.
Read only

Bit: 1 Name: Beginning of tape (BOT)
Function: Set when the selected slave detects the BOT marker.
Read only

Bit: 0 Name: Slave attention (SLA)
Function: Set by a selected slave which requires attention due to coming on-line.
Read only

Error Register (MTER) 772 454
There are 16 different error conditions that can be detected in the TU45 tape subsystem. The error register is a read only register that stores all of the tape system error indications.

Errors are characterized as class A and class B. Class B will terminate an in-progress data transfer; a class A error will not. However, the MASSBUS controller is notified of any error during a data transfer by the immediate assertion of EXCH on the MASSBUS. If the tape subsystem is not performing any operation, or is performing a rewind (i.e., to GO bit is clear), the controller
is immediately notified of an error condition by the assertion of ATTN H on the MASSBUS.

Bit: 15  Name: Correctable data error/CRC error (COR/CRC)
Function: PE mode—set on a tape character. Therefore, PE error correction logic was able to correct the data on-the-fly and good data was transferred to memory.

NRZI mode—set when the CRC character generated from read back data does not agree with the CRC read from tape. Cleared by drive clear or INIT.

Bit: 14  Name: Unsafe (UNS)
Function: Set if the GO bit in the MTCS1 register is set, the MOL bit in the MTDS register is reset, and a command code other than drive clear is issued.

Bit: 13  Name: Operation incomplete (OPI)
Function: A read or space operation indicates that a tape record has not been detected within 4.3 sec from command initiation. A write operation indicates that a read-after-write tape record has not been detected within 0.43 sec from command initiation. Can also indicate the NSG 0.8 inches.

Bit: 12  Name: Drive timing error (DTE)
Function Set during a write operation if WCLK was not received from the controller in time to provide a valid tape character, or when a data transfer is attempted when the bus of the MASSBUS is already.
Bit: 11  Name: Non-executable function (NEF)

Function: Set when:

A write operation is attempted on a write-protect transport.

A space reverse, read reverse, or write check reverse is attempted when the tape is at BOT.

The DEN 2 bit in the tape control register does not agree with the PES status bit.

A space or write operation is attempted when FCS = 0 in the tape control register.

A read or write operation is attempted with DEN2 = 0 in the tape control register and the 2’s complement of a number less than 13 is in the frame count register.

Bit: 10  Name: Correctable skew/illegal tape mark (CS/ITM)

Function: In PE mode, this bit is set when excessive but correctable skew is detected in data read back from tape. It is a warning only, and does not indicate that bad data was read from tape.

In NRZI mode, this bit is set when a bit pattern is detected on tape which has the general characteristics of an NRZI filemark (specifically, two single characters separated by seven blank character spaces) but which does not contain the exact data expected in an NRZI filmark.

Bit: 9   Name: Frame count error (FCE)

Function: Set when a space operation has terminated and the frame counter is not cleared.

Bit: 8   Name: Non standard gap (NSG)

Function: Set after a data transfer operation whenever any tape characters are read while the read head is scanning the first half of the interrecord gap.

Bit: 7   Name: PE format error/LRC (PEF/LRC)

Function: Set in PE mode when an invalid preamble or postamble is detected. Set in NRZI mode when the LRC character generated from readback data does not match the LRC character read from tape.

Bit: 6   Name: Incorrectable data/vertical parity error (INC/VPE)

Function: A PE read operation indicates that one of the following has occurred: multiple dead tracks, parity errors
without dead tracks, skew overflow, during an NRZI 
read operation, indicates that a vertical parity error 
has occurred or that data has occurred after the skew 
delay is over.

Bit: 5 Name: Data bus parity error (DPAR)
Function: Set when a parity error is detected on the MASSBUS 
data lines during a write operation.

Bit: 4 Name: Format error (FMT)
Function: Set when a data transfer is attempted with an incor-
rect format code.

Bit: 3 Name: Control bus parity error (CPAR)
Function: Set when a parity error is detected on the MASSBUS 
control lines during a control bus write operation.

Bit: 2 Name: Register modification refused (RMR)
Function: Set when the controller attempts to write into any im-
plemented TU45 register except the maintenance reg-
ister or the attention summary register while the GO 
bit is asserted. If RMR occurs, the address register is 
not modified.

Bit: 1 Name: Illegal register (ILR)
Function: Set when a read or write from a non-existent register 
is attempted.

Bit: 0 Name: Illegal function (ILF)
Function: Set when the GO bit is asserted and a function code 
not implemented by the system is attempted.

Attention Summary (MTAS) Register 772 456
The attention summary register is read/write "pseudo-register," 
which consists of from one to eight bits depending on the num-
ber of controllers in the system. The term "psuedo-register" re-
fers to the fact that only one register bit position is physically 
contained in each controller. This bit position reflects the state 
of the ATA status bit for that TM02. Hence, bit position 0 of the 
attention summary register is generated by the ATA bit of the 
controller, bit position 1 is generated by the ATA bit of the con-
troller, and so on to bit 7. Bits 8 through 15 are not used.

Bit: 15-8 Name: Not used
Function:

Bit: 7-0 Name: ATA 07-00
Read/write
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**Function:** Each bit sets when the corresponding drive asserts its ATA bit. All bits are cleared by UNIBUS INIT, drive clear, or controller clear. Individual bits are cleared by loading a function code with the GO bit in the corresponding drive or by writing a 1 in the ATA bit positions of this register.

**Character Check (MTCC) Register 772 460**
The check character register is a nine-bit, read-only register that permits you to check the validity of a data transfer. At the end of an NRZI read operation, this register contains the CRC character for that operation. Hence, you can determine if the CRCC generator logic is functioning properly. At the end of a PE read operation, however, this register contains a dead track indication (DT = 1) of any track which may have dropped one or more bits during the operation.

**Bit:** 15-9  **Name:** Not used.

**Function:**

**Bit:** 8-0  **Name:** Check character read track (CCD)

**Function:** Contains the CRC character and parity bit in NRZI mode or the dead track register in PE mode.

**Data Buffer (MTDB) Register 772 462**
This register provides a maintenance tool to check the data buffer in the controller. A total of eight words is accepted before the data buffer becomes full. Successive reads from data buffer will read out words in the same order in which they were entered into the data buffer.

The MTDB register can be read and written only as an entire word. Any attempt to write a byte will cause an entire word to be written. Reading the DB register is a “destructive read-out” operation: the top data word in the data buffer is removed by the action of reading DB, and a new data word (if present) replaces it a short time later. Conversely, the action of writing the DB register does not destroy the “contents” of DB; it merely causes one more data word to be inserted into the data buffer.

**Bit:** 15-0  **Name:** Data buffer (DB 15-00)

**Function:** Used by the program for diagnostic purposes. When the register is written into, IR is cleared until the DB is ready to accept a new word. When the register is read, it will cause OR to be cleared until a new word is ready. During a write-check error condition, the data
word read from tape which did not compare with the corresponding word in memory is frozen in MTDB for examination by the program.

**Maintenance (MTMR) Register 772 464**
The maintenance register is a 16-bit read/write register which performs the following functions: provides data wraparound paths for checking the formatting logic in the controller, provides a means for testing error detection circuitry within the controller, acts as a storage buffer for the longitudinal parity check (LRC) character when operating in NRZI mode and performing a forward read or forward write operation.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-7</td>
<td>Maintenance data field (MDF 8-10)</td>
<td>These bits buffer the data generated during wraparound operations. At the end of normal NRZI transfers (except read reverse), these bits contain the LRC of the last record. MDF 0 contains the parity bit for the maintenance data character. MDF 1 contains the LSB of the maintenance data character and the remain bits are contained in order in MDF 2 through MDF 8. Read/write</td>
</tr>
<tr>
<td>6</td>
<td>Two-hundred BPI clock (BPICLK)</td>
<td>Displays a clock signal derived from the crystal oscillator in the selected slave. The clock frequency is dependent on the read/write speed of the selected slave and is equal to the frequency at which at continuous succession of characters is written on tape when operating at 200 characters per inch density. Read only</td>
</tr>
<tr>
<td>5</td>
<td>Maintenance clock (MC)</td>
<td>This bit controls the sequencing of data through the controller data paths when operating in maintenance mode. Read/write</td>
</tr>
</tbody>
</table>
Bit: 4-1  Name: (Cont)

Function:

Bit: 0  Name: Maintenance mode (MM)

Function: Must be set to a 1 when any maintenance mode function is desired. Setting the MM bit to 1 does not initiate any action on the part of the drive but alters the manner in which the drive executes various commands. The manner in which the command execution is altered depends on the maintenance of code in bits 4 through 1 of this register.

Read/write

Drive Type (MTDT) Register 772 466
The drive type register is a read-only register, the content of which identifies the particular type of storage device (transport) being used. Bits 0 through 8 (DT 0-8) of the drive type register identify the type and status of the selected transport. If a non-existent transport is selected or if the selected transport is not powered up, DT 0-8 will contain 010₈. If the selected transport is powered up, but is not a TU45, DT 0-8 will contain 011₈ or 013₈ to 017₈, depending on the type of transport. If the selected transport is a TU45 and is powered up, these bit positions will contain 012₈.

Bit: 15  Name: Not sector addresses (NSA)

Function: Always set to indicate that the device is not sector addressable.

Read only

Bit: 14  Name: Tape (TAP)

Function: Always set to indicate that the device is a tape transport.

Read only

Bit: 13  Name: Moving head (MOH)

Function: Always negated to indicate that the device is not a moving head unit.

Read only

Bit: 12  Name: 7 Channel (7CH)

Function: Asserted if the selected transport is a 7-channel unit. Always negated if the selected transport is a TU45.

Read only

Bit: 11  Name: Drive request required (DRQ)
Function: Always negated to indicate that the device is a single-port device.
    Read only
Bit: 10  Name: Slave present (SPR)
Function: Asserted when a transport is powered up and have been assigned the selection code contained in the MTTC tape control register.
    Read only
Bit: 9   Name: Not used
Function:
Bit: 8-0 Name: Drive tape (DT8-0)
Function: Contains the drive type number for the selected slave (11_8 for the TU45). If no slave is assigned in bits 0-2 of the MTTC type control register, the drive code readback is 010_8. If a slave has been assigned a select code in bits 0-2 of this register, the drive type code will be a code from 11_8 to 17_8.
    Read only

Serial Number (MTSN) Register 772 470
The Serial Number Register is a read only register that contains a BCD representation of the four least significant digits of the transport serial number.

Bit: 15-12 Name: SN15-SN12
Function: Most significant BCD digit (10(**)3) of slave serial number.
    Read only
Bit: 11-08 Name: SN11-SN08
Function: 10(**)2 digit of slave serial number.
Bit: 7-4   Name: SN07-SN04
Function: 10(**)1 digit of slave serial number
Bit: 3-0   Name: SN03-SN00
Function: Least significant BCD digit of slave serial number.
    Read only

Tape Control (MTTC) Register 772 472
The Tape Control Register is a read/write register that selects an existing transport, the data format, and the density.

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Bit: 15  Name: Acceleration (ACCL)
Function: Set when the transport is not actively reading or writing data.
          Read only

Bit: 14  Name: Frame count status (FCS)
Function: Normally set at the end of a write into the frame count register. Cleared when frame count register overflows.
          Read only

Bit: 13  Name: Tape control write (TCW)
Function: Set when a control bus write operation to the tape control register is performed. Cleared by the initiation of any command requiring tape motion.
          Read only

Bit: 12  Name: Enable abort on data transfer errors (EAODTE)
Function: This bit, when written to a 1, will cause a data transfer operation to aborted as soon as the error is deleted.
          Read/write

Bit: 11  Name: Not used
Function:

Bit: 10-8 Name: Density select (DEN2-DENO)
Function: Specifies the tape character density during read or write operations:

<table>
<thead>
<tr>
<th>DEN2</th>
<th>DEN1</th>
<th>DEN0</th>
<th>Density (bpi)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>800 NRZ</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>800 PE</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1600</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Drive clear and INIT do not affect the density select bits.

Bit: 7-14  Name: Format select (FMT SEL 3-0)
Function: Specifies MASSBUS-to-tape character formatting during a write operation, or tape character-to-MASSBUS formatting during a read operation.
Read/write

Bit: 3  Name: Even parity (EV PAR)
Function: If this bit is set in NRZI mode, even parity will be written on tape and even parity is expected on read-back. If this bit is reset, odd parity will be written on tape and will be expected on read-back.
Read/write

Bit: 2-0  Name: Slave select (SS2-0)
Function: Specifies the unit number of the transport to be used.

Bus Address External (MTBAE) Register 772 474
The MTBAE register contains the upper 6 bits of the memory address and combine with the lower 16 bits located in MTBA to form the complete 22 bit address. This register should be loaded by the program in conjunction with the MTBA register to specify the starting memory address of a data transfer operation. The six bit field is incremented (decremented for specific function codes) each time a carry (borrow) occurs from the MTBA register during memory transfers.

Bit: 15-6  Name: Not Used
Function: Always read as a 0.

Bit: 15-0  Name: Bus Address (A21:16)
Function: Loaded by the program to specify the starting memory address of a data transfer operation. The MTBAE register is incremented (or decremented) each time a carry out (borrow out) of MTBA occurs. A16 and A17 can also be set or cleared through the MTCS1 register.

Control and Status 3 (MTCS3) Register 772 476
The MTCS3 register contains parity error information associated with the memory bus. Bit position 13 of the MTCS2, (PE) indicates that a parity error occur during the memory transfer. Bits 15 through 13 of MTCS3 further localize the error for diagnostic maintenance. In addition, bits 3 through 0 provide the diagnostic program the ability to invert the sense of parity check and thereby verify correct operation of the parity circuits.
An Interrupt Enable bit in the MTCS3 register allows the program to enable interrupts without writing into a drive register as previously described. This bit also appears in the MTCS1 register for program compatibility and can be set or cleared by writing into either register.

**Bit: 15**  **Name:** Address Parity Error (APE)
**Function:** Set if the address parity error line indicates that the memory detected a parity error on address and control information during a memory transfer.
Read only

**Bit: 14, 13**  **Name:** Data Parity Error Odd Word, Even Word (DEP, OW, EW)
**Function:** Set if a parity error is detected on data from memory when the controller is performing a Write or Write Check command.
Read only

**Bit: 12, 11**  **Name:** Write Check Error Odd Word, Even Word (WCE, OW, EW)
**Function:** Set when data fails to compare between memory and the drive.
Read only

**Bit: 10**  **Name:** Double word (DBL)
**Function:** Set if the last memory transfer was a double word operation. Cleared by UNIBUS INIT, Controller Clear or loading a data transfer command with GO set.
Read only

**Bit: 9-7**  **Name:** Not Used
**Function:** Always read as a 0.

**Bit: 6**  **Name:** Interrupt Enable (IE)
**Function:** IE is a control bit which can be set under program control. When IE = 1, an interrupt may occur due to RDY or SC being asserted. Cleared by UNIBUS INIT, Controller Clear, or automatically cleared when an interrupt is recognized by the CPU.
Read/write

**Bit: 5-4**  **Name:** Not Used
**Function:** Always read as a 0.

**Bit: 3-0**  **Name:** Invert Parity Check (IPCK 3:0)

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Function: These bits are written by the program to control the data parity detection logic. When set inverse parity is checked with data during memory transfers of Write and Write Check operations.

SPECIFICATIONS
Main Specifications
Storage medium 1/2-in. wide magnetic tape (industry std)
Capacity/tape reel 32 million characters (at 1600 bpi, nominal)
Data transfer speed 120,000 characters per sec., max.
Drives/control 8, max.
Number of tracks 9
Recording density 800 or 1600 bpi program selectable
Interrecord gap 0.50 in. min.
Recording method NRZI for 800 bpi phase-encoded for 1600 bpi

Tape Motion
Read/write speed 75 in./sec.
Rewind speed 250 in./sec.
Rewind time 115 sec. (typical)

Tape Characteristics
Length 2400 ft. max.
Type Mylar base, iron-oxide coated
Reel diameter 10-1/2 in., max.
Handling Direct-drive reel motors, servo-controlled single capstan, filtered positive pressurized tape compartment, vacuum type tape cleaner.

Mechanical
Mounting Tape drive and master electronics mount in a H950 or H9502 cabinet (supplied)

Cabinet size (with covers closed) 72 in.h; 27.5 in.w; 32 in.d

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MAGNETIC TAPES

TU45

H9502
TJU45 Control unit (RH11) 60.5 in.h; 27.5 in.w; 32 in.d
TWU45 (Control unit (RH70) 2 system units (mounts in a separate assembly)
Weight
Cable length
MOUNTS IN PDP-11/70 BACKPLANE
APPROX. 500 LBS (INCLUDING CABINET)
100 FT. MAX., FOR TOTAL TAPE SYSTEM (CONTROL UNIT TO FURTHEST DRIVE)
STANDARD LENGTHS:
MASSBUS-10FT.
SLAVEBUS-10 FT.

Power
Current for TJU45, TWU45 master 7.5 A (average at 115 Vac)
Current for tape control
Current for MASSBUS control
Heat dissipation

Environment
Operating temperature
Relative humidity

15° TO 35°C (NON-CONDENSING)
30% TO 89% MAX. WET BULB 25°C

Miscellaneous
BOT, EOT detection
Skew control
Write protection
Data checking
Write-protect ring sensing on tape transport
Read-after-write parity checking of characters: Longitudinal Parity check, and Cyclic Redundancy check

Testing
Self-test of control with tape transport off-line; on-line check control data paths

Error correction
(Phase-encoding only), "On-the-fly" error correction for a single-track dropout

Magnetic head
DUAL-GAP, READ-AFTER-WRITE

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DECTAPE
DECTape II, TU58, is a low cost mass memory device offering random access on block-formatted, pocket-size cartridge media. DECTape II is ideal for small system mass storage, diagnostic loading, and software update distribution. A dual drive DECTape II offers 0.5 megabyte of storage space, making it one of the lowest cost tape subsystems available.

FEATURES
- capacity of 262,144 bytes per formatted cartridge
- random access to 512 blocks of 512 bytes each
- 10 second average access time
- 60 inch per second bidirectional search speed
- reliable 30 inch per second read/write tape speed
- up to two drives per controller
- offered as an OEM component product and as an integrated subsystem
- rugged pocket sized media
- easy to load—just insert

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DESCRIPTION
DECTape II is a random-type access, mass memory tape subsystem capable of reading and writing 256K bytes/per drive of data on block-addressable, preformatted cartridges at 800 bits per inch. DECTape II is a magnetic tape transport subsystem for auxiliary data storage. Low cost, low maintenance, and high reliability are assured by the simply designed transport mechanisms. Each transport has a high quality read/write head with full erase-gap for reliable recording. The system stores information at fixed positions on magnetic tape as in magnetic disk or floppy disk storage devices, rather than at unknown or variable positions as in conventional magnetic tape systems. This feature allows replacement of blocks of data on tape in a random fashion, without disturbing information recorded previously. In particular, during the writing of information on tape, the system reads a format from the tape, and uses this information to determine the exact position to record the information to be written. Similarly, in reading, the same format is used to locate data to be played back from the tape.

Data Organization
DECTape II is divided on two tracks into 2048 128-byte blocks. These blocks are interleaved to maximize motor life. Interleaved data (placing corresponding blocks of data in alternate blocks) prolongs the motor life by minimizing the stop-and-go action common to most tape subsystems. The blocks permit data to be partitioned into groups of words that are integrated, while greatly reducing the amount of storage area that would be needed for addressing individual words. A simple example of such a group of words is a program. A program can be stored and retrieved from magnetic tape in a single block format because it is not necessary to be able to retrieve only a single word from the program. However, it is necessary to be able to retrieve different programs that may not be related in any way. Thus, each program can be stored in a different block on the tape.

Operation
Since DECTape II is a fixed-address system, the host computer need not know where the tape has stopped. To locate a specific point on tape, the host computer requests to read or write a numbered block. The address of the block currently passing over the head is read by the DECTape II microprocessor, which calculates the tape motion necessary to find the requested location and accomplish the requested task. This built-in function makes software interfacing to the DECTape II much simpler, and significantly decreases overhead of the host computer.
Data Integrity
DECTape II employs a 16 BIT CHECKSUM to ensure accurate data recording and retrieval. The DECTape II microprocessor automatically generates a CHECKSUM when a block of data is written, and similarly checks the character when the block is read. If an error is found, the device rereads the tape up to eight times before a hard error is indicated. This feature eliminates the host computer overhead normally associated with rereading soft errors.

A Light-emitting diode (LED) is also provided in the rack mounted option, that indicates if the cartridge is in motion. This visible indicator helps prevent a user from inadvertently removing a tape while the DECTape II is in operation.

Data integrity is further ensured by a write-protect feature. Implementation of a plastic write-lockout allows the user to choose write-protection of tapes for short- or long-term operation. The lockout can be completely removed for long-term write protection or can be easily “switched” when short-term write protection is desired.

To maximize data integrity, a high quality magnetic head has been used with a full track width erase head to insure complete block erasure. An optional write-verify mode backs the tape up after writing and reads (with increased threshold) the data. The CHECKSUM is tested by the microprocessor and verified.

Perfomatted Medium
The DECTape II medium is an oxide-coated tape with header marks to indicate Beginning of Tape (BOT) and End of Tape (EOT) to the microprocessor. Adjacent files are separated by perfomatted Inter Record Marks (IRMs). The servo circuit includes a “runaway timer” that is used to protect tape cartridges from being unspooled, in event of a processor failure or a read chain failure. The microprocessor must acknowledge seeing each Inter Record Mark during tape motion. If no acknowledgment occurs in a predetermined time, tape motion is stopped.

Component Level
DECTape II mechanisms and the subsystem printed circuit module are offered separately for integration by the OEM. Each mechanism occupies 64 cubic inches of space allowing 256 bytes of storage in a compact package. The TU58 offers such features as random-access block addressing, low power consumption, and serial baud rates ranging from 150 to 38.4K baud, making it one of the most versatile storage mediums available. Power require-
ments of the component-level product are very low at $+5V @ 600mA$ and $+12V @ 1.2A$ peak, $600mA$ steady state running, $50mA$ idle.

**Rack-Mounted**
In its rack-mounted integration level, the TU58 is a dual drive configuration featuring media storage space and activity lights. The modular design of the TU58 allows all maintenance to be performed from the front of the unit, which reduces the mean time to repair.

**Intelligent Terminals**
Dual DECTape II cartridge tapes are integrated into DIGITAL's intelligent terminals, the PDT-11/130, allowing 512K bytes of block addressable mass storage. System files and data files can be stored locally, and captured data can be stored for later transmission. DECTape II provides an easy, quickly accessible storage medium, making program distribution inexpensive and easy.

**Logical Format**
Data are recorded on two tracks. Each track contains 1024 records of 128 bytes. Both tracks are recorded in the forward direction. Special marks are recorded during tape formatting that indicate the beginning and the end of the tape and the beginning of each record.

**Software Interface**
The TU58 is controlled by a high level command set that frees the host from device related operations such as tape positioning. The TU58 host interface is an asynchronous serial line compatible with the DLII or DLVII. The serial line uses a protocol designed to provide low cost systems with control and 8-bit binary data transfers over one full duplex line.

**REGISTERS**
The interface between the data bus and the DLII or DLVII is via four device registers: the Receiver Status Register, The Receiver Data Buffer, The Transmitter Status Register, and The Transmitter Data Buffer Register.
The Receiver Status Register (RCSR) 77X XXO

**DESCRIPTION AND OPERATION**

**Bits:** 15-8 and 5-0 are unused

**Bit: 7**  
- **Name:** Receiver Done  
- **Read only**  
- **Function:** This bit when set indicates that there is a character available in the receive buffer.

**Bit: 6**  
- **Name:** Receiver Interrupt Enable  
- **Read/write**  
- **Function:** This bit, when set, causes an interrupt request to be generated each time bit 7 in RCSR is set.

**Receiver Data Buffer Register (RBUF) 77X XX2**

**Bit: 15**  
- **Name:** Error  
- **Read only**  
- **Function:** This bit is set if bit 14, 13, or 12 (or any combination of these bits) in RBUF is set.

**Bit: 14**  
- **Name:** Overrun  
- **Read only**
Function: This bit is set if bit 7 in RCSR (Receiver Done) is not cleared before the UART attempts to present a new character to RBUF, i.e., if the UART attempts to set bit 7 in RCSR, and it is already set. The previous character in RBUF is lost, and the new character replaces it.

Bit: 13 Name: Framing Error
Read only
Function: This may indicate an open input line, "BREAK" signal, or excessive distortion of the received character.

Bit: 12 Name: Receive Data Parity Error
Read only
Function: This bit is always zero if the "no parity check" option is specified. Bits 14, 13, or 12 are updated each time a character is received.

Bit: 7-0 Name: Received Data
Read only
Function: These bits contain the last complete character assembled. The unused high order bits will contain 0.

Transmitter Status Register (XCSR) 77X XX4

Transmitter Status Register (XCSR) 77XXX4

Bit: 15-8 Name: Unused
Bit: 7 Name: Transmitter Ready
Read only
Function: This bit is cleared when a data character is loaded into XBUF. This bit is set, not cleared, by INIT.

Bit: 6 Name: Transmitter Interrupt Enable
Read/write
Function: This bit, when set, will cause an interrupt request to be generated whenever bit 7 in XCSR is set.

Bit: 5, 4, 3  Name: Unused
Bit: 2        Name: Maintenance
Read/write

Function: This bit, when set, causes data emitted at the serial output of the transmitter section to appear at the serial input of the receiver section. It is cleared by INIT, and by the program.

Bit: 1  Name: Unused
Bit: 0  Name: BREAK

Function: The transmitter will appear to the program to function normally if characters are presented to XBPF. This bit is cleared by INIT, and by the program.

Transmitter Data Buffer Register (XBUF) 77X XX6

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bit: 7-0  Name: Transmitted Data
Write only

Function: These bits contain the data character to be transmitted by the UART. If the data character contains fewer than 8 data bits, the character must be right justified when loaded into XBUF.

Clock Register (LKS)

Bit: 15-8  Name: Unused
Bit: 7      Name: LINE CLOCK MONITOR
Read/clear

Function: Set only by the line frequency clock signal and cleared only by the program.

Bit: 6      Name: LINE CLOCK INTERRUPT ENABLE
Read/write

Function: When set, starts an interrupt sequence if Line Clock monitor is also set.

Bit: 5-0    Name: Unused
MAGNETIC TAPES

TU58

DL11 SPECIFICATIONS
Function: Provides an interface between the PDP-11 UNIBUS and a single asynchronous bit serial communications channel.

Mechanical: The DL11 consists of one quad module and a connecting cable terminated in a plug appropriate to the data communications equipment to be connected.

Operating Mode: Full or half duplex under program control.

TU58 SPECIFICATIONS
Temperature
TU58 operating (External) 15°C (58°F) to 32°C (90°F) ambient
TU58 non-operating -30°F to 140°F
Media operating 10°C (50°F) to 52°C (125.6°F)
Maximum Temperature Gradient between system ambient and TU58 ambient 18°C (32.4°F)

Relative Humidity
TU58 operating
Maximum wet bulb 25°C (77°F)
Minimum dew point 2°C (36°F)
Relative humidity 20% to 80% RH
TU58 non-operating 5% to 98% RH
Media operating 10% to 80% RH

Electrical
Power consumption +5V @ 1A
+12V @ 1.2A peak,
+.64A average running, 0.5A static

Interface levels
Serial Interface In accordance with RS-423 compatible with RS-232 or RS-422
DESCRIPTION
The TU60 Magnetic Tape, TA11 System is a reliable, inexpensive, dual-drive, reel-to-reel unit designed to replace paper tape. Its two drives run nonsimultaneously using proprietary Digital Equipment Corporation Philips-Type cassettes. Engineered to provide users with optimum price/performance, the system offers the following features:

• 1 MIL TAPE. Heavy mylar backing eliminates edge damage and resultant tape failure.

• REEL-TO-REEL DRIVE. Increases tape life. Only two driving elements. No pinch rollers, capstans, brakes, clutches, pulleys, or belts.

• SINGLE TRACK RECORDING. Differentially balanced head eliminates external noise sensitivity. Low density and wide track recording ensure reliability.

• DC MOTORS. Linear servos provide precise, gentle tape acceleration and deceleration. Eliminates stretching and guarantees gap spacing.

• SOLID-CASTING DRIVE. All elements needed to control tape position, skew, and motion are mounted on precision solid casting.

• MODIFIED HUB. Optimizes data capacity, simplifies loading.

• LEADER DETECTION. Optical, foolproof, failsafe.

• CASSETTES INTERCHANGEABLE. Assured by precision construction and frequency-independent read electronics.

• ERROR CHECKING CIRCUITS. 16-bit cyclic redundancy check.
MAGNETIC TAPES

TU60

- PHASE-ENCODED RECORDING. Read by sensitive, noise-immune peak detection circuits and phase lock loop.
- SERVICEABLE. Electronics, drives, and power supply are easily accessible plug-in subassemblies.

The TA11 includes a Control Unit and a Dual Tape Transport.

Data Organization
In the TA11 Cassette System, data is recorded on tape in a single bit-serial track of data. Since there is no prerecorded timing or format track (such as in DECTape), data must be sequentially recorded and retrieved as in conventional magnetic tapes systems.

The cassette medium is an oxide-coated tape with sections of clear leader (no oxide) appended to both ends. Data can not be recorded in these clear leader sections, but they identify BOT (beginning of tape) and EOT (end of tape). Placement of data onto the recordable region of the cassette tape is organized into units called files. Adjacent files are separated by file gaps, which are generated under soft control. Each file consists of one or more blocks separated by block gaps. Block gaps are generated automatically. Each block consists of one or more bytes of data and two cyclic redundancy check (CRC) bytes. Under program control, the CRC bytes are appended when a block is written and checked when a block is read. Each byte consists of eight bits (no parity). The number of files, blocks per file, and bytes per block is unrestricted, except for tape capacity. Tape capacity is 92,000 bytes, minimum. That is reduced by 300 bytes per file gap and 46 bytes per block gap.

REGISTERS
Control and Status Register (TACS) 777 500

```
   15 14 13 12 11 10  9  8  7  6  5  4  3  1  0
ERROR BLOCK CHECK CLEAR LEADER WRITE LOCK FILE GAP TIMING ERROR OFF LINE UNIT SELECT TRANSFER REQUEST INTERRUPT ENABLE READY ILBS FUNCTION GO
```
Effect of the Initialize (INIT) signal: clear bits 8 to 6, 4 to 1; set bit 5.

Read only: bit 15 through 9, 7, and 5

Write only: bit 0

**Bit: 15**  
**Name:** Error  
**Function:** Set to indicate an error condition determined by the current status indicators of TACS, bits 14 through 9, and by the current function, bits 3 through 1. Error bit is valid only when ready is set.

**Bit: 14**  
**Name:** Block Check  
**Function:** Set to indicate a CRC error for READ and SFB. During a READ function, Block Check sets Error. During an SFB function, the bit is normally expected and does not set Error. Cleared when the next function is successfully initiated.

**Bit: 13**  
**Name:** Clear Leader  
**Function:** Set when the currently selected cassette is at EOT or BOT. The bit sets Error for all functions except REWIND.

**Bit: 12**  
**Name:** Write Lock  
**Function:** Set to indicate that the currently selected cassette is write-protected if and only if the current function bits are set for WRITE or WFG. The bit sets Error.

**Bit: 11**  
**Name:** File Gap  
**Function:** Set when a file gap has been entered during a READ, SFB, SRF or SFF function. The bit sets Error only on READ and SFB. Cleared when the next function is successfully initiated.

**Bit: 10**  
**Name:** Timing Error  
**Function:** Set when the program's response to Transfer Request was not quick enough and signifies loss of data during Read or Write function. The bit sets Error. Cleared when the next function is successfully initiated.

**Bit: 9**  
**Name:** Off Line  
**Function:** Set when the currently selected cassette is not present or when there is no power in the cassette transport. The bit sets Error on all functions.

**Bit: 8**  
**Name:** Unit Select
**MAGNETIC TAPES**

**TU60**

**Function:** Specifies which transport is under program control 0 for left (unit 0); 1 for right (unit 1).

**Bit: 7**  **Name:** Transfer Request

**Function:** Set when data is available in Data Buffer, TADB, during READ, or request for data during WRITE. Cleared when TADB is addressed. The bit is held clear by ILBS. It inhibits Ready from setting and must be serviced prior to Ready.

**Bit: 6**  **Name:** Interrupt Enable

**Function:** Set to enable Ready or Transfer Request = 1 to cause an interrupt.

**Bit: 5**  **Name:** Ready

**Function:** Set when the cassette is ready to accept and execute a command. It is cleared when a function is initiated and set when the function is completed as long as Transfer Request is clear.

**Bit: 4**  **Name:** ILBS

**Function:** Initiate Last Byte Sequence. Set to terminate WRITE function by causing the transport to write the CRC bytes, and to terminate READ function by causing the transport to read and check the next two bytes on tape as CRC characters. For an n-byte block, ILBS is set in response to the n + 1 Transfer Request. The bit holds Transfer Request clear.

**Bit: 3-1**  **Name:** Function

**Function:** Indicates function to be performed.

<table>
<thead>
<tr>
<th>BIT</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>WRITE</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>READ</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>SPACE REV. FILE</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>SPACE REV. BLOCK</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>SPACE FWD. FILE</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>SPACE FWD. BLOCK</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>REWIND</td>
</tr>
</tbody>
</table>

**Bit: 0**  **Name:** Go

**Function:** Set to initiate the function specified by bits 3 to 1.

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Data Buffer Register (TADB) 777 502

The TADB register serves a dual function and actually comprises two separate registers in the control. One register is loaded with 8-bit data from the Cassette during the read function and this data can be retrieved by reading TADB. The other register is loaded from the UNIBUS and presented to the Cassette during the write function.

SPECIFICATIONS

Main Specifications
Storage medium 0.150" wide magnetic tape (in a DECassette)
Capacity/cassette 92,000 bytes
Data transfer speed 562 bytes/sec, max
Drives/control 2 (1 dual unit)

Data Organization
Number of tracks 1 (full width)
Bytes/block 1 to 92,000
Bits/byte 8
Recording method phase encoding
Recording density 350 to 700 bits/inch

Tape Motion
Read/write speed 9.6 inches/sec, avg
Search speed 22 inches/sec, avg
Start/stop time 20 msec, max
Rewind time 20 sec, typ (100 to 150 in/sec) 30 sec, max
Handling reel-to-reel drive

Tape Characteristics
Length 150 ft
Type computer-grade, 100% certified
1 mil thick, mylar substrate

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## Register Addresses
- Command and Status (TACS) 777 500  
- Data Buffer (TADB) 777 502

## UNIBUS Interface
- Interrupt vector address 260 
- Priority level BR6 
- Bus Loading 1 bus load

## Mechanical
- Mounting 1 panel-mounted unit + 1 SPC slot 
- Size 5 1/4” front panel height + quad module 
- Cable 15 ft, supplied; 25 ft, max

## Power
- Input current 1 A at 115 Vac  
- 1.5 A at + 5 V 
- Heat Dissipation 120 W

## Environmental
- Operating temperature 10°C to 40°C 
- Relative humidity 20% to 80%

## Models
- TA11-AA Dual cassette unit and control,  
  115 Vac, 60 Hz 
- TA11-AB Dual cassette unit and control,  
  230 Vac, 50 Hz 
- TU60-K Cassette with 150 ft of certified tape

## Miscellaneous
- Error control 16-bit cyclic redundancy check (CRC), hardware-generated and appended to data at time of writing. Tested during read by hardware via program command. 
- Read electronics Peak detection/phase lock loop (low threshold read).
CHAPTER 7
PAPER TAPE

PC11

DESCRIPTION
The PC11 high-speed reader and punch system consists of a paper tape reader, punch and control. The system reads eight-hole unoiled perforated tape at 50 characters per second. A unit containing a reader only (PR11) is also available.

Operation
In reading the tape, a set of photodiodes translates the presence or absence of holes in the tape to logic levels representing ones and zeros, to the presence or absence of holes in the tape. All information read or punched is parallel-transferred through the controller. When an address is placed on the UNIBUS, the controller decodes the address and determines if the reader or the punch has been selected. If one of the four device register addresses has been selected, the controller determines whether an input or an output operation should be performed. An input operation from the reader is initiated when the processor transmits a command to the Paper Tape Reader Status Register. An output operation is initiated when the processor transfers a byte to the Paper Tape Punch Buffer Register.

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The controller enables the PDP-11 system to control the reading or punching of paper tape in a flexible manner. The reader can be operated independently of the punch. Either device can operate under direct program control or can operate without direct supervision, using interrupts to maintain continuous operation.

REGISTERS
Paper Tape Reader Status Register (PRS) 777 750

Effect of the Initialize (INIT) signal: clear bits 11, 7, and 6.
Read only: bits 15, 11, and 7
Write only: bit 0

Bit: 15  Name: Error
Function: Set when an error occurs: no tape in reader, reader is off-line, or reader has no power.

Bit: 11  Name: Busy
Function: Set when a character is being read. It is set when Reader Enable is set and cleared when the present operation is complete (when Done is set).

Bit: 7  Name: Done
Function: Set when a character is available in the Reader Data Buffer. It is cleared by any program reference to the Reader Data Buffer or by setting Reader Enable.

Bit: 6 Name: Interrupt Enable
Function: Set to allow Error or Done = 1 to cause an interrupt.
Bit: 0 Name: Reader Enable
Function: Set to allow the Reader to fetch one character. The setting of this bit clears Done, sets Busy, and clears the Reader Buffer (PRB). Operation of this bit is disabled if Error = 1; attempting to set it then will cause an immediate interrupt if Interrupt Enable = 1.

Paper Tape Reader Buffer (PRB) 777 552

Bits 7 through 0 hold the coded data for the character read. The bits are cleared when Reader Enable, bit 0 of PRS, is set. To the processor, the data is read only.

Any program reference to PRB (777 552 or 777 553) as a word or byte will clear Done, bit 7 of PRS.

Paper Tape Punch Status (PPS) 777 554

Effect of the Initialize (INIT) signal: clear bit 6, set bit 7.
Read only: bits 15 and 7

Bit: 15 Name: Error
Function: Set when an error occurs: no tape in punch, or punch has no power.

Bit: 7 Name: Ready
Function: Set when ready to punch a character. It is cleared
PAPER TAPE DEVICES

PC11

when the Punch Buffer is loaded and set when punching is done.

Bit: 6  Name: Interrupt Enable
Function: Set to allow Error or Ready = 1 to cause an interrupt.

Paper Tape Punch Buffer Register (PPB) 777 556

Bits 7 through 0 hold the coded data for the character to be punched. To the processor, the data is write only.

An instruction that could modify PPB as a word or byte clears Ready (bit 7 of PPS) and initiates punching. An immediate interrupt will occur when punching is initiated if Error = 1 and Interrupt Enable = 1.

SPECIFICATIONS

Main Specifications
Storage medium 8-hole paper tape, unoiled
Reader speed 300 char/sec
Punch speed 50 char/sec
Paper tape Fanfold
Data format 8-bit characters

Register Addresses
Reader Status (PRS) 777 550
Reader Buffer (PRB) 777 552
Punch Status (PPS) 777 554
Punch Buffer (PPB) 777 556

UNIBUS Interface
Interrupt vector address 70 (for reader); 74 (for punch)
Priority level BR4 (reader has precedence over punch)
Bus loading 1 bus load

Mechanical
Mounting 1 panel mounted unit + 1 SPC slot

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PC11

Size  
10 1/2" front panel height + quad module

Weight  
50 lb

Power  
Input current  
3A at 115Vac; 1.5A at +5V
Heat dissipation  
350 W

Environment  
Operating temperature  
10°C to 40°C
Relative humidity  
10% to 90%

Models  
PC11: Reader/punch and control, 115Vac, 60 Hz
PC11-A: Reader/punch and control, 230Vac, 50 Hz
PR11: Reader and control
H722: Transformer-1sp (required for 230Vac, 50 Hz operation of PC11-A or PR11)
AA11-K

The AA11-K includes four digital-to-analog converters (DACs) and an associated display control.

FEATURES
• 4-channel independently buffered 12-bit digital-to-analog converter
• oscilloscope control logic for the four digital-to-analog channels
• 4096 × 4096 dot matrix capabilities
• oscilloscope control signals available for controlling a variety of oscilloscopes, charts, and X/Y recorders
• bipolar output ranges of ±5V, ±10V, ±0.5V
• quad-sized module that interfaces directly to the PDP-11 UNIBUS
• status register control of intensity, write-through, nonstore, and erase functions to provide flexibility for oscilloscope or other device control

DESCRIPTION
The AA11-K display control permits you to display data in the form of a 4096 × 4096 dot array. Under program control, a dot may be produced at any point in this array, and a series of these dots may be programmed sequentially to produce graphical output.

The display control may output to chart or X/Y recorder or CRT display unit. Normal configuration calls for its use with a VR17 CRT Display Monitor. However, it is capable of operating with other equipment, such as the Tektronix 602, 604 display oscilloscopes and 611, 613 storage oscilloscopes.

The AA11-K has four 12-bit DACs, each driven from a 12-bit buffer register, and circuitry that provides all controls necessary to output the analog signals to an external oscilloscope. Digital-to-analog (D/A) output is nominally ±5V; however, this can be set to ±0.5V or ±10V. Outputs are capable of driving up to 5000 pF of load.

Output operations are accomplished by loading the display status register and the D/A buffer registers. Through use of display status register bits, the user can intensify the contents of the D/A buffer registers; provide delays necessary for some oscilloscope applications; provide erase, write-through, and non-store control functions for storage oscilloscope applications; and enable interrupt on completion of oscilloscope intensification, erase, and ex-
ternal delay. The display control offers four program-controlled nodes in which the oscilloscope can intensify a point. Jumpers provide additional display control flexibility by allowing you to select the desired delay, intensification pulse polarity, magnitude, and duration.

**STANDARD* REGISTER ADDRESSES**

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Status</td>
<td>770416</td>
</tr>
<tr>
<td>X-D/A0</td>
<td>770420</td>
</tr>
<tr>
<td>Y-D/A1</td>
<td>770422</td>
</tr>
<tr>
<td>D/A2</td>
<td>770424</td>
</tr>
<tr>
<td>D/A3</td>
<td>770426</td>
</tr>
</tbody>
</table>

* The register address is switch-selected in increments of 40 locations. However, the relative location of the various registers will remain the same.

**VECTOR ADDRESSES* AND PRIORITY LEVELS**

<table>
<thead>
<tr>
<th>Address</th>
<th>BR Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>360</td>
<td>4</td>
</tr>
</tbody>
</table>

**REGISTERS**

Programming the AA11-K is accomplished through the display status register and the D/A data registers. One hardware interrupt vector is associated with the display control.

**Display Status Register** 770416

```
  15 13 12 11 10  9  8  7  6  5  4  3  2  1  0
     NOT USED              MODE

ERASE STORAGE SCOPE
WRITE THRU STORAGE SCOPE
STORE STORAGE SCOPE
BIT 9
NOT USED
READY FLAG
INTERUPT ENABLE
NOT USED
EXTERNAL DELAY
FAST INTENSIFY
INTENSIFY
```

**Bit: 15-13 Name:** Unused

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Bit: 12  Name: Erase
Function: Bit 12 = 1, erase data in the storage oscilloscope. Write only.

Bit: 11  Name: Write Thru
Function: Bit 11 = 1, an intensified point will not be stored even though the user is in the store operation. (Works with WRITE THRU input of the oscilloscope.) Write only.

Bit: 10  Name: Store
Function: Bit 10 = 1, all intensified points will be stored. INTENSIFY pulse width increased from 2 to 6 \( \mu s \). Read/write.

Bit: 9   Name: Bit 9
Function: A digital signal available to the I/O connector. Read/write.

Bit: 8   Name: Unused

Bit: 07  Name: Ready Flag
Function: Bit 7 = 0, the oscilloscope is not ready, do not load or intensify points. Bit 7 = 1, the oscilloscope is ready. Read only.

Bit: 6   Name: Interrupt Enable
Function: Bit 6 = 1 and bit 7 in transition from a 0 to a 1 will cause an interrupt. Read/write.

Bit: 5   Name: Unused

Bit: 4   Name: EXT DELAY
Function: When bit 04 = 1, all internal timing stops and READY signal at the I/O connector goes low. When the external device (oscilloscope or XY recorder) returns a DELAY RET signal, an intensify pulse will be generated and the Ready flag will be set. Read/write.

Bit: 3-2 Name: Mode
Function: 00 Normal Intensification with bit 00 in SR
01 X Mode Intensification on loading X D/A (D/A 0)
10 Y Mode Intensification on loading Y D/A (D/A 1)
11 XY Mode Intensification on loading X or Y D/A. Read/write.

Bit: 1   Name: Fast Intensify Enable
Function: Bit 1 = 0, all oscilloscope settling delays are as defined for each oscilloscope. Bit 1 = 1, settling delay is 3 \( \mu \text{s} \). Read/write.

Bit: 0 Name: Intensify

Function: Bit 0 = 1, generates an intensify pulse in mode 00. Write only.

Interrupts occur when bit 06, Interrupt Enable, is set and bit 7, Ready Flag, sets. Bit 7 sets when an INTENSIFY pulse occurs or when an erase operation is complete. The Ready flag notifies the user that all delays (including EXTERNAL DELAYS) and operations are complete.

A point may be intensified in any of four control modes, selected by bits 2 and 3. In mode 0, a point is intensified by setting bit 0. Mode 1 intensifies a point upon loading the X D/A register; mode 2 intensifies a point upon loading the Y D/A register; mode 3 intensifies upon loading either the X or Y D/A register.

DATA REGISTERS
The D/A data registers are read/write registers and they are word operable.

```
15 12 11   DATA 0
NOT USED
```

D/A Data Registers Format

OSCILLOSCOPE CONTROL DESCRIPTION
Point plotting on an oscilloscope or X-Y recorder is done by providing the desired voltage to the X and Y inputs, setting the beam or the pen in the desired spot.

After allowing time for the X-Y amplifiers to settle, an INTENSIFY (Z) pulse intensifies the positioned beam or a digital signal lowers the pen to plot a point.

By repeating the process or position/intensify, alphanumeric and graphic information can be plotted.

The AA11-K controls the oscilloscope with the ERASE, WRITE THRU, STORE, READY and BIT 9 open-collected TTL signals provided at the I/O connector.
D/A CONVERTERS
The four DACs have 12 bits straight binary or 2's complement input and a bipolar output normally set to ±5V. The outputs can be jumpered to provide ±10V or ±0.5V if needed. If voltages other than those provided are required, use the attenuator in the oscilloscope (or plotter).

SPECIFICATIONS (±5V RANGE)

Number of DACs: 4
Digital Input: 12 bits bipolar, straight binary; jumperable to 2's complement
Digital Storage: Read-write, word operable, single buffered
Output Voltage: ±5V; ±10V, ±0.5V jumperable
Resolution: 1 part in 4096 of full range
Warmup Time: 5 minutes minimum
Gain Accuracy: Adjustable
Gain Drift: 10 ppm/o C maximum
Offset Accuracy: Adjustable
Offset Drift: 20 ppm of F.S./o C maximum
Linearity: ±1/2 LSB maximum
Differential Linearity: ±1/2 LSB maximum, monotonic
Output Impedance: 1 ohms maximum at D/A output
BC08R-08 Cable Impedance: 4 ohms maximum
Drive Capability: ±5 mA maximum per DAC
Slew Speed: 5V/μs
Rise and Settling Time to 0.1% of final value: 4 μs, 8 μs with 5000 pF load in parallel with 1K ohm

Intensify
INTENSIFY Pulse Width: 2 μs; 6 μs in store mode
INTENSIFY Pulse Magnitude: 3.3V; 1.4V jumperable
INTENSIFY Pulse Polarity: Jumperable (negative normally)
Intensification Delay: 1. 3 μs in fast intensify mode
2. 20 μs; 20 μs jumperable
3. Externally determined by DELAY RETURN L

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The AD11-K is a 12-bit analog to digital converter that accepts analog data at specified rates and stores the equivalent digital value for software processing.

FEATURES
- real-time data acquisition
- low cost
- flexibility

DESCRIPTION
The basic AD11-K subsystem consists of an input multiplexer (switch selectable between 16 channel single ended or 8 channel differential), sample and hold circuitry, and a 12-bit A/D converter. Simply changing the jumpers can change the analog inputs from bipolar to unipolar. Inputs are over-voltage protected on all ranges.

The AD11-K is a 12-bit successive approximation converter in which data is right justified in offset binary. It is controlled by the A/D status register. A/D conversion can be initiated in any one of three ways: under program control, on overflow from a real-time clock, or on an external input. This system flexibility enables the AD11-K to serve in most applications that require data acquisition.

You can select single ended or differential mode by switch operation. In single ended mode, up to 16 single ended or pseudo differential channels of analog input can be selected. The input channel is selected by the status register. Input voltage can be changed from the standard setup of +−5V to +−5.12V, +−10V, +−10.24V, 0 to 10V or 0 to 10.24 simply by configuring jumpers on the module.

Once an A/D conversion is completed, a flag is set, and if the A/D interrupt is enabled, the processor will interrupt (vector) to the proper subroutine for data processing. The program can be run in interrupt mode or can be set to wait for the A/D done flag.

The multichannel throughput rate is 50 kHz. Since the converted value is held in a buffer register, a second conversion can be started before the results of the first conversion are read, achieving a high throughput rate.

The AD11-K includes an 8-bit D/A converter, which is normally used for maintenance to test the A/D converter but is also available to the user.
AD11-K

The digital-to-analog converter has no control logic, so software must provide the proper settling delay (approximately 30 μsec). The D/A output range is \(+\text{ }-2V\).

REGISTER AND VECTOR ADDRESSING
The AD11-K has a floating address to allow the use of more than one AD11-K in a system, or to avoid any device address conflict with other options. The standard register addresses selected for the AD11-K are:

170400          R/W—status register
170402          Write—loads D/A buffer register
                Read—reads A/D buffer register

REGISTERS

Status Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>Error Flag</td>
<td>This bit sets when:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1. A second A/D conversion ends before data from the previous A/D conversion is read.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. A second A/D start is initiated before the first version is complete. Read/write.</td>
</tr>
<tr>
<td>13-8</td>
<td>Mux Channel</td>
<td>Defines which A/D input channel of the multiplexer is to be sampled. Read/write.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Six-bit address field selects one of 64 channels, of which 16 are located in the AD11-K and 48 are located in the optional AM11-K expander.</td>
</tr>
<tr>
<td>7</td>
<td>Done Flag</td>
<td>Sets upon completion of an A/D conversion. Cleared by hardware when the A/D interrupt bus cycle is complete or when the buffer register is read. Read only.</td>
</tr>
<tr>
<td>6</td>
<td>Interrupt Enable</td>
<td>When a conversion is completed, the done flag will cause an interrupt if this bit is set. Read/write.</td>
</tr>
<tr>
<td>5</td>
<td>Overflow Enable</td>
<td>Permits overflow from KW11-K real-time clock to cause an A/D start. This allows channel sampling at precisely timed intervals independent of software. Data may then be read by testing the A/D done flag or by enabling the interrupt. Read/write.</td>
</tr>
</tbody>
</table>
Bit: 4  Name:  External Start Enable
Function: Permits an external event to initiate an A/D conversion.
           Read/write.

Bit: 0  Name:  A/D Start
Function: Starts an A/D conversion. Cleared at end of conversion.
           Read/write.

A/D Buffer Register
The A/D buffer register is a read-only register. It furnishes the
12-bit converted value, formatted in 12-bit right, justifies offset
binary after an A/D conversion is completed.

D/A Buffer
The D/A Buffer is a write-only register. It is an 8-bit register that
holds the digital value to be converted to an analog signal.

8-BIT INPUT                                         OUTPUT
(OCTAL)                                             RANGE
  000377                                             +1.870V
  000200                                             0V
  000000                                             −1.875V
RESOLUTION                                          14.64mV

SPECIFICATIONS
General
12-bit A/D converter with sample-and-hold
Accuracy at 25°C                                    0.025% of full scale range
Number of channels                                   16 (single-ended or pseudo-
                                                       differential)
                                                       8 true differential

SPC—Quad module
Pin-compatible with AR11 at Berg connector (H854)
Uses H322 panel
Uses same wrap-around module
Expansion capabilities (via AM11-K)
64 (single ended or pseudo-
   differential)
32 (true differential)
Control
Controlled by programmed instructions, clock counter over-
   flow, or external input
**SENSOR I/O DEVICES**

**AD11-K**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Format</td>
<td>Parallel, 12-bit, right justified, offset binary, double buffered</td>
</tr>
<tr>
<td>Warm-up time</td>
<td>Five minutes</td>
</tr>
<tr>
<td>Power</td>
<td>+5 Vdc at 3.5 A (max)</td>
</tr>
<tr>
<td><strong>Accuracy</strong></td>
<td></td>
</tr>
<tr>
<td>Relative accuracy (linearity)</td>
<td>0.025% of full scale range</td>
</tr>
<tr>
<td>Differential linearity</td>
<td>No skipped states, no states wider than 2 LSB</td>
</tr>
<tr>
<td></td>
<td>99% of states $\pm$ 1/2 LSB</td>
</tr>
<tr>
<td><strong>Stability</strong></td>
<td></td>
</tr>
<tr>
<td>Gain temperature coefficient</td>
<td>12 ppb/$^\circ$C, 20$^\circ$C/LSB at full scale</td>
</tr>
<tr>
<td>Linearity temperature coefficient</td>
<td>3 ppm of F.S./$^\circ$C, 81$^\circ$C/LSB</td>
</tr>
<tr>
<td>Offset temperature coefficient</td>
<td>10 ppm of F.S./$^\circ$C, 25$^\circ$C/LSB</td>
</tr>
<tr>
<td>Recommended calibration interval (two adjustments)</td>
<td>6 months</td>
</tr>
<tr>
<td><strong>Repeatability</strong></td>
<td></td>
</tr>
<tr>
<td>rms Noise (0)</td>
<td>1/2 LSB (max)</td>
</tr>
<tr>
<td><strong>Inputs</strong></td>
<td></td>
</tr>
<tr>
<td>Bias current</td>
<td>10 na (max)</td>
</tr>
<tr>
<td>Input impedance</td>
<td>10 megohms (min)</td>
</tr>
<tr>
<td></td>
<td>10pF (max) OFF channel</td>
</tr>
<tr>
<td></td>
<td>100 pF (max) ON channel</td>
</tr>
<tr>
<td><strong>Input Voltage Range</strong></td>
<td>Standard Setup: $\pm$5V</td>
</tr>
<tr>
<td></td>
<td>Optional Setup: $\pm$0.12V, ±10</td>
</tr>
<tr>
<td></td>
<td>10V, $\pm$10.24V, 0 to 10V or 0 to 10.24V</td>
</tr>
<tr>
<td>Resolution</td>
<td>12 bits (1 part in 4096)</td>
</tr>
<tr>
<td><strong>Signal Dynamics</strong></td>
<td></td>
</tr>
<tr>
<td>Throughput time</td>
<td>20 $\mu$sec (includes interchannel settling and A/D conversion)</td>
</tr>
<tr>
<td>Inter-channel settling error</td>
<td>1 LSB (max)</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>80 dB down at 1 kHz</td>
</tr>
<tr>
<td></td>
<td>(15 OFF channels into one ON channel)</td>
</tr>
<tr>
<td>Differential CMRR</td>
<td>70 dB (dc to 1 kHz)</td>
</tr>
<tr>
<td>Small signal bandwidth</td>
<td>500 kHz typical</td>
</tr>
</tbody>
</table>

317
<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slew rate limit</td>
<td>7 V/μsec</td>
</tr>
<tr>
<td>Sample-and-hold aperture</td>
<td>200 nsec typ, delay from external start</td>
</tr>
<tr>
<td></td>
<td>165 nsec typ, delay from clock overflow</td>
</tr>
<tr>
<td></td>
<td>20 nsec max, delay uncertainty</td>
</tr>
</tbody>
</table>
The AM11-K is an expansion multiplexer used to expand the number of analog input channels of the AD11-K.

FEATURES

- low-cost input multiplexer expansion of the AD11-K A/D converter to 64 single-ended (32 differential) input channels
- 48 (24) channels of analog input expansion
- single-ended or differential inputs can be jumper-selected independently in groups of 16 (8) channels
- screw terminal distribution panel included
- panel-mounted option requiring no small peripheral controller (SPC) or system unit (SU) mounting space (cable connection to AD11-K)

NOTE

Numbers in parentheses mean differential channels. Other numbers mean single-ended or pseudodifferential, i.e., "16 (8) channels" mean 16 single-ended or pseudodifferential or 8 differential channels.

DESCRIPTION

The AM11-K is a multiplexer expander that supplements the 16 channel single-ended (8 differential) analog input multiplexer in the AD11-K analog-to-digital (A/D) converter.

The expansion is done in three independent groups on the AM11-K. Each group can be set to 16 single-ended or pseudodifferential or 8 differential input channels; each group can have a gain of 1, 4, 5, 16, 50, or 64 assigned to it by a switch set in the amplifier.

If the three independent multiplexer expander groups in the AM11-K are set for gains of 4, 16, and 64, respectively, and the multiplexer group in the AD11-K is set at unity gain, a programmable gain data acquisition system can be configured by connecting the same groups in the AM11-K and the AD11-K. The result is a programmable gain data acquisition system with 8 differential (or 16 single-ended) channels. The AM11-K assembly provides screw terminals for the customer's wiring. A BC11-T cable connects the AM11-K to the AD11-K and provides the power and communication link between them.
The processor communicates via the UNIBUS with the AD11-K only. When a channel in the range 20-77 is called for, the AD11-K will activate that channel in the AM11-K.

The throughput rate for channels 20-77 in the AM11-K is 25 kHz, versus a 50 kHz rate for the AD11-K, because longer settling time is allotted to the gain amplifier in the AM11-K.

The AM11-K uses the built-in self-test circuitry in the AD11-K. The ±8V ramp generator and ±2V (8-bit) digital-to-analog (D/A) converter, in conjunction with the G5036 wraparound module, test the functionality of the AM11-K and AD11-K.

**PROGRAMMING**

All communication to the AM11-K is handled by the AD11-K. An input channel in the AM11-K is selected by loading the proper word into the status register of the AD11-K. The AD11-K, in turn, activates the desired channel in the AM11-K.

**SPECIFICATIONS**

**AD11-K Input voltage range**

Jumper-Selectable

±5V, ±5.12V,

±10V, ±10.24V,

0V to +10V

0V to +10.24V

**AD11-K Standard voltage range**

±5V

**AM11-K Gain (Switch-Selectable in groups of 16 (8) channels**

1, 4, 5, 16, 50, 64

**AM11-K Standard Gain**

1

**AD11-K Resolution**

12 bits (1 part in 4096 of input range)

**Single channel throughput to memory using a PDP-11/34 under optimum programming and external A/D start**

40 kHz

**AM11-K number of channels**

48 (channels of single-ended, or pseudodifferential)

24 (channels of differential)

**Input impedance**

100 megohms

**Input bias current**

50
Temperature stability

Gain 25 ppm/°C
Offset: Gain = 1, 50 ppm of F.S.R./°C
Gain = 64, 1.5 ppm of F.S.R./°C

GENERAL SPECIFICATIONS
Mechanical
19" x 5.19" panel
Operating Temperature
10°C (50°F) to 40°C (104°F)
Relative Humidity
10% to 90%
(no condensation)
FEATURES

- low cost
- compact
- convenient interfacing and mounting
- capabilities include:
  A/D converter—auto zeroing technique (patented)
  16-channel multiplexer, with sample and hold
  Programmable clock
  Scope display control with 2 D/A converters
  UNIBUS interface logic

DESCRIPTION

The AR11 is a compact analog real-time subsystem for use with the PDP-11 family of computers. Included in the subsystem are a 10-bit analog/digital converter, two 10-bit digital/analog converters, a crystal controlled clock, scope control, a 16-channel multiplexer, and a sample and hold circuit. Operation and selection of functions are under software control.

A/D Converter System

The 10-bit A/D converter samples analog data at specified rates and allows the program to store the equivalent digital value for subsequent processing. Sample and hold circuitry ensures accu-
rate conversions, even on rapidly changing signals, by holding the input voltage constant until the process is completed. The maximum throughput rate for a single channel is approximately 35 kHz. A 16-channel single-ended multiplexer is included. The input voltage range is program-selectable for unipolar (0V to +5V), or bipolar (−2.5V to +2.5V) operation.

Display Control
The control displays data in the form of a 1024 by 1024 dot array. Under program control, a bright dot may be produced at any point in this array. A series of these dots may be programmed to produce graphical output. The display can drive an X-Y analog recorder, and offers four program-controlled modes in which the scope can intensify a point. There are two 10-bit D/A converters with either a ±5V or a ±0.5V full scale output and all the necessary circuitry for scope control.

Programmable Clock
The programmable clock offers several methods for accurately measuring and counting time intervals or events. It can be used to synchronize the central processor to external events, count external events, measure intervals of time between events, or provide interrupts at programmable intervals. It can be used to start the A/D converter at predetermined intervals or from an external logic input.

The clock operates in one of two program modes: single interval or repeated interval. There are seven programmable frequencies: 1 MHz to 100 Hz, an external input, and an auxiliary input (on the backplane wiring).

An 8-bit counter can be preset for a number of time pulses or events to occur before an interrupt (or A/D counter start) is initiated. This counter can be read from the processor at any time to determine timing status.

PACKAGING
The complete AR11 subsystem electronics are contained on one single hex module that can mount in either of the two center slots of a DD11-B system unit, or within the CPU mainframe assembly. All external connections are made via a Berg connector (supplied with mating plug) which is mounted on an outside corner of the module.

No external analog supply voltages are required. A unique dc to dc converter without transformer uses the +5V logic power to
generate the high-quality positive and negative voltages needed by the AR11.

PROGRAMMING
There are 8 registers used for control and data. The address of the first register is selectable in increments of 20, between 770 000 and 777 760. With a starting address of 770 400, the arrangement is:

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/D Status</td>
<td>770 400</td>
</tr>
<tr>
<td>A/D Buffer</td>
<td>770 402</td>
</tr>
<tr>
<td>Clock Status</td>
<td>770 404</td>
</tr>
<tr>
<td>Clock Buffer</td>
<td>770 406</td>
</tr>
<tr>
<td>Display Status</td>
<td>770 410</td>
</tr>
<tr>
<td>X Buffer</td>
<td>770 412</td>
</tr>
<tr>
<td>Y Buffer</td>
<td>770 414</td>
</tr>
<tr>
<td>Clock Counter</td>
<td>770 416</td>
</tr>
</tbody>
</table>

There are three interrupt vectors with the address of the first vector selectable in increments of 20. If the first vector is at 300, the arrangement is:

<table>
<thead>
<tr>
<th>Vector</th>
<th>Address</th>
<th>Priority Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/D</td>
<td>300</td>
<td>BR6</td>
</tr>
<tr>
<td>Clock</td>
<td>304</td>
<td>BR6</td>
</tr>
<tr>
<td>Scope Control</td>
<td>310</td>
<td>BR4</td>
</tr>
</tbody>
</table>

SPECIFICATIONS
A/D Converter System
Input voltage range
0 to +5V, or −2.5V to +2.5V, program-selectable
Resolution
10 bits (1 part in 1024)
Accuracy at 25°C
±0.1% of full scale
Linearity
1/2 LSB
Conversion time
22 to 24 μsec
Number of input channels
16
Input impedance
10M ohms, minimum
Settling time (MUX plus S & H)
8 μsec, max. (5-volt step)

Scope Control
D/A output voltage range
−5V to +5V, or −0.5V to +0.5V, jumper-selectable (2 D/As)
Resolution
Accuracy at 25°C

Programmable Clock
Clock rates

Operating modes
Counter size
Preset register size
Accuracy
External input
Auxiliary frequency input

Mechanical
Mounting
User interface

Power
4A at +5V

10 bits
±0.1% of 10V full scale, or
±2% of 1V full scale

1 MHz, 100 kHz, 10 kHz, 100 Hz all crystal controlled; external logic input; auxiliary frequency input

Single interval, repeated interval
8 bits
8 bits
±0.005%
TTL logic
TTL logic, accessible on backplane

1 hex module slot
Berg connector on the module

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DESCRIPTION
The DR11-B is a general purpose direct memory access (DMA) interface to the UNIBUS. The DR11-B, rather than using program-controlled data transfers, operates directly to or from memory, moving data between the UNIBUS and the user device.

The interface consists of four registers: command and status, word count, bus address, and data. Operation is initialized under program control by loading word count with the twos complement of the number of transfers, specifying the initial memory or bus address where the block transfer is to begin, and by loading the command/status register with function bits. The user device recognizes these function bits and responds by setting up the control inputs. If the user device requests data from memory of a UNIBUS device, the DR11-B performs a UNIBUS Data In transfer (DATI) and loads its data register with the information held at the referenced bus address. The outputs of this register are available to the user device; this output data is buffered. If the user device requests data to be written into memory, the DR11-B performs a UNIBUS Data Out transfer (DATO), moving data from the user device to the referenced bus address; this input data is not buffered. Transfers normally continue at a user-defined rate until the specified number of words is transferred.

The user is given a number of control lines allowing for flexible operation. Burst modes, read-modify-restore operations and byte addressing are possible with the control structure.

The DR11-B is packaged in one standard System Unit allowing convenient incorporation into a PDP-11 system. A UNIBUS jumper module is supplied with the unit.

REGISTERS

NOTE
The INIT signal is held asserted internal to the DR11-B whenever an interlock error occurs (M9680 test board neither in slots ABO2 for normal operation nor in CDO4 for maintenance mode).

Word Count Register (DRWC) 772 410
DRWC is a 16-bit read/write register. It is initially loaded with the twos complement of the number of transfers to be made and normally increments up toward zero after each bus cycle. When overflow occurs (all ones to zeros), the READY bit of DRST is set
and bus cycles stop. DRWC is a word register; therefore do not use byte instructions when loading it. Cleared by INIT.

**Bus Address Register (DRBA) 772 412**
DRBA is a 15-bit read/write register. Bit 0, corresponding to address line A00, is provided by the user device. Along with XBA16 and 17 in DRST, DRBA is used to specify BUS A<17:01> in direct bus access. The register is normally incremented by 2 after each cycle, advancing the address to the next sequential word location on the bus. If DRBA (corresponding to A<15:01>) overflows (all ones to all zeros), the ERROR bit in DRST is set. This error condition (BAOF) is cleared by loading DRBA or INIT. Incrementation can be inhibited by the user device, refer to the BA INC ENB user signal. With this control signal and A00 provided externally, DRBA can be used to address sequential bytes. This is a word register; therefore do not use byte instructions when loading it. Cleared by INIT.

**Status and Command Register (DRST) 772 414**
The DRST is used to give commands to the user device and to provide status indicators of the DR11-B control and the user device.
Bit: 15  Name: Error
Function: Set to indicate an error condition: either NEX (bit 14), ATTN (bit 13), interlock error (test board is neither in slots AB02 nor CD04), or bus address overflow (BAOF: DRBA incremented from all ones to zeros). Sets READY (bit 7) and causes interrupt if IE (bit 6) is set. ERROR is cleared by removing all four possible error conditions: interlock error is removed by inserting test board in CD04 for diagnostic tests or in AB02 for normal operation. Bus address overflow is cleared by loading DRBA, NEX is cleared by loading bit 14 with a zero, and ATTN is cleared by user device. Read only.

Bit: 14  Name: Nonexistent Memory (NEX)
Function: Set to indicate that as UNIBUS master, the DR11-B did not receive a SSYN response 20 µsec after asserting MSYN. Cleared by INIT or loading with a zero; can not be loaded with a one. Sets ERROR. Read only.

Bit: 13  Name: Attention (ATTN)
Function: Attention bit that reads the state of the ATTN user signal. Sets ERROR. (Used for device-initiated interrupt.) Set and cleared by user control only. Read only.

Bit: 12  Name: Maintenance
Function: Maintenance bit used with diagnostic programs. Cleared by INIT. Read/write.

Bit: 11-9  Name: Device Status (DSTAT A, B, C)
Function: Device status bits that read the state of the DSTAT A, B, and C user signals. (Not tied to interrupt.) Set and cleared by user control only. Read only.

Bit: 8  Name: Cycle
Function: CYCLE is used to prime bus cycles. If set when GO is issued, an immediate bus cycle occurs. Cleared when bus cycle begins; cleared by INIT. Read/write.

Bit: 7  Name: Ready
Function: Set to indicate that the DR11-B is able to accept a new command. Set by INIT or ERROR, cleared by GO; set on word count overflow. Causes interrupt if bit 6 is set. Forces DR11-B to release control of the UNIBUS and prevents further DMA cycles. Read only.

Bit: 6  Name: Interrupt Enable (IE)
Function: Set to allow ERROR or READY = 1 to cause an interrupt. Cleared by INIT. Read/write.
DR11-B

Bit: 5-4 Name: Extended Bus Address

Function: Extended bus address bits 17 and 16, in conjunction with DRBA, specify A(17:01) in direct memory transfers. Cleared by INIT. BA17 and 16 do not increment when DRBA overflows; instead ERROR is set. Read/write.

Bit: 3-1 Name: Function 3, 2, 1

Function: Three bits made available to the user device. User-defined. Cleared by INIT. Read/write.

Bit: 0 Name: Go

Function: Set to cause a pulse to be sent to the user device indicating a command has been issued. Clears READY. Always reads as a zero. Write only.

Data Buffer Register (DRDB) 772 416

The DRDB serves two functions. First, it is a 16-bit write-only register. The outputs of this register are available to the user device (refer to the DATA OUT signals). The register can be loaded under program control but is also used to buffer information when data is being transferred from the UNIBUS to the user device (when DR11-B does a DATI cycle). DRDB is a word register; therefore do not use byte instructions when loading it. Cleared by INIT.

Second, the DRDB functions as a 16-bit read-only register. Information to be read is provided by the user device on the DATA IN signal lines. These lines are not buffered and must be held until they are either read under program control or transferred directly to memory (DATO bus cycle).

Maintenance Mode

Checkout and test of the DR11-B is accomplished by using a MAINT bit in DRST along with a special maintenance module which simulates the user’s device. The maintenance module plugs directly into the two slots normally occupied by the cable boards and jumps the output and input signals. The maintenance module is included with the DR11-B.

SPECIFICATIONS

Usage:
Direct memory access (DMA) data transfer

Input/output levels (user interface):
Logic 1 = +3V
Logic 0 = 0V
Register Addresses

Word Count  (DRWC) 772 410
Bus Address  (DRBA) 772 412
Status and Command  (DRST) 772 414
Data Buffer  (DRDB) 772 416
2nd DR11-B  772 430 to 772 436
3rd DR11-B  772 450 to 772 456
4th DR11-B  772 470 to 772 476

UNIBUS Interface

Interrupt vector address  124 (1st DR11-B) (for other DR11-Bs, assigned by user)
Priority level  BR5
Data transfer  NPR
Bus loading  1 bus load

Mounting: 1 System Unit (SU)

Input Current: 3.3A at +5V (no current needed at −15V)
DESCRIPTION
The DR11-C is a general-purpose interface between the PDP-11 UNIBUS and a user's peripheral. The DR11-C provides the logic and buffer registers necessary for program-controlled parallel transfers of 16-bit data between a PDP-11 system and an external device. The interface also includes status and control bits that may be controlled by either the program or by the external device for command, monitoring, and interrupt functions.

The DR11-C interface consists of three functional sections:
• address section logic
• interrupt control logic
• device interface logic

The address selection logic determines: if the interface has been selected for use, which register is to be used, if a word or byte operation is to be performed, and, what type of transfer (input or output) is to be performed.
DR11-C

The interrupt control logic permits the interface to gain bus control and perform program interrupts to specific vector addresses. The interrupt enable bits are under program control; the interrupt bits are under control of the user’s device.

The DR11-C interface logic consists of three registers:

- control and status
- input buffer
- output buffer

Operation is initialized under program control by addressing the DR11-C to specify the register and the type of operation to be performed.

If an output operation is specified, information from the UNIBUS is stored in a 16-bit register. Once this register has been loaded under program control (e.g., MOV RO, OUTBUF), the outputs are available to the device until the register is loaded with new data from the bus. This register can also be read on the bus. When data has been transferred to the buffer register, a NEW DATA READY control signal is supplied to indicate to the user’s device that data has been loaded by means of a DATA or DATOB bus cycle and is read by means of a DATI or DATIP bus cycle.

When an input operation is specified, the DR11-C provides 16 lines of input to UNIBUS transmitters. This permits data from the user’s device to be read onto the bus. A control signal, DATA TRANSMITTED, informs the device that the input lines have been read. The input lines, which are not buffered, can be read by a DATI bus cycle (e.g., MOV INBUF, RO).

The control and status register provides six bits that can be used to control the monitor user functions. Two of these are interrupt enable (INT ENB) bits under control of the program. Two bits (REQ A and B) are under direct control of the user’s device and can only be read by the program. These bits can be used either to initiate interrupt requests or to provide flags that can be monitored by the program. The remaining two bits (CSR0 and CSR1) are read/write bits that can be controlled by the program to provide command or monitoring functions. In maintenance mode, they are also used to check interface operation.

A maintenance cable, which is supplied with the interface, permits checking of the DR11-C logic by loading the input buffer from the output buffer rather than from the user’s device. Thus, a word from the bus is loaded into the output register and the same word
DR11-C Interface, Block Diagram

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appears when reading the input buffer, if the interface is functioning properly.

The DR11-C can also be used as an interprocessor buffer (IPB) to allow two PDP-11 processors to transfer data between each other. In this case, one DR11-C is connected to each processor bus and the two DR11-Cs are cabled together, permitting the two processors to communicate.

**Physical Description**
The DR11-C interface is packaged on a single quad module that can be plugged into a small peripheral slot (SPC).

The module has two Berg connectors for all user input/output signals. Two M971 connector blocks, which are not supplied with each interface, can be used to bring all input/output lines to individual pins on a back panel via two H856 cables. Note that this cable is a mirror image rather than a straight one-to-one cable.

The following accessories are available for interfacing:

- BC08R (Berg-to-Berg) flat cable available in lengths of 1, 6, 8, 10, 12, 20, and 25 feet. When ordering, the dash number indicates the desired cable length; e.g., BC08R-1 or BC08R-25.
- M971 connector board. A single-height by 8½ in. board that brings the signals from one Berg connector to the module fingers.
- H856 Berg connector. Includes an H856 Berg connector and 40 pins.

**REGISTERS**

![Register Diagram]

The register addresses can be changed by altering the jumpers on the address selection logic. However, if the jumpers are
changed, any programs or other software referring to these addresses must also be modified accordingly.

**Control and Status Register (DRCSR) 767 770**
The Control and Status Register is used to enable interrupt logic and to provide user-defined command and status functions for the external device.

Two REQUEST bits, which are under device control, may be used to provide device status indications. When used with the associated INT ENB (interrupt enable) bits that are under program control, they may be used to initiate interrupts. Two other bits (CSR0 and CSR1) are controlled from the UNIBUS and serve as command bits.

Although the REQUEST and CSR bits can be used for any function the user desires, standard PDP-11 interface conventions attempt to allocate bit 15 for error conditions and bit 7 for ready indications. Both of these bits can generate interrupt requests. Bit 0 is normally used for start or go commands.

**Bit: 15**
**Name:** REQUEST B

**Function:** This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program.

When used as an interrupt request, it is set by the internal device and initiates an interrupt provided the INT ENB B bit (bit 5) is also set.

When used as a flag, this bit can be read by the program to monitor external device status.

When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 (bit 1). This permits checking interface operation by loading a 0 or 1 into CSR1 and then verifying that REQUEST B is the same value.

A read-only bit, cleared by INIT when in maintenance mode.

**Bit: 7**
**Name:** REQUEST A

**Function:** Performs the same function as REQUEST B (bit 15) except that an interrupt is generated only if INT ENB A (bit 6) is also set.

When the maintenance cable is used, the state of REQUEST A is identical to that of CSR0 (bit 0).
A read-only bit, cleared by INIT when in maintenance mode.

Bit: 6  Name: INT ENB A
Function: Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST A (bit 7) becomes set.
Can be loaded or read by the program (read/write). Cleared by INIT.

Bit: 5  Name: INT ENB B
Function: Interrupt enable bit. When set, allows an interrupt sequence to be initiated provided REQUEST B (bit 15) becomes set.
Can be loaded or read by the program (read/write). Cleared by INIT.

Bit: 1  Name: CSR1
Function: This bit can be loaded or read (under program control) from the UNIBUS and can be used for a user-defined command to the device. It appears only on Connector No. 1.

When the maintenance cable is used, setting or clearing this bit causes an identical state in bit 15 (REQUEST B). This permits checking operation of bit 15 which cannot be loaded by the program.
A read/write bit (can be loaded or read by the program), cleared by INIT.

Bit: 0  Name: CSR0
Function: Performs the same functions as CSR1 (bit 1) but appears only on Connector No. 2.
When the maintenance cable is used, the state of this bit controls the state of bit 7 (REQUEST A).
A read/write bit, cleared by INIT.

Output Buffer Register (DROUTBUF) 767 772
The output buffer is a 16-bit read/write register that may be read or loaded from the UNIBUS. Information from the bus is loaded into this register under program control. At the time of loading, a pulsed signal (NEW DATA READY) is generated to inform the user's device that the register has been loaded. The trailing edge of the positive pulse should be used to allow the data to be loaded and to settle on the user's input lines. Data from the buffer is
transmitted to the user's device on the data OUT lines by means of a DATO or DATOB bus cycle.

The contents of the output buffer register may be read at any time by means of a DATI or DATIP bus cycle. During the read operation, the output of the buffer is fed directly to the bus data lines.

Whenever the maintenance cable is used, the data from the output buffer is also applied to the input buffer register. This permits checking operations of the interface logic.

The DROUTBUF is cleared by INIT.

**Input Buffer Register (DRINBUF) 767 774**
The input buffer is a 16-bit read-only register that receives data from the user's device for transmission to the UNIBUS. Information to be read is provided by the user's device on the data IN signal lines. Because the input buffer consists of gating logic rather than a flip-flop register, the data IN lines must be held until read onto the bus. The register is read by a DATI sequence and the data is transmitted on the UNIBUS for transfer to the processor or some other device. When the input lines are read during a DATI sequence, a pulsed signal (DATA TRANSMITTED) is sent to the user's device to inform it that the transfer has been completed. The trailing edge of the positive-going pulse indicates that this transfer is completed.

Whenever the maintenance cable is used, the input buffer register receives data from the output buffer register rather than from the user's device. This permits checking of the interface logic by loading a word from the bus into the output register and verifying that the same word appears in the input buffer.

**SPECIFICATIONS**

**Usage**
Priority interrupt interface control.

**Input/Output Levels**
(User interface)
logic 1 = +3 V
logic 0 = 0 V

**Register Addresses**
Control and Status (DRCSR) 767 770
Output Buffer (DROUTBUF) 767 772

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DR11-C

Input Buffer (DRINBUF) 767 774
2nd DR11-C 767 760 to 767 764
3rd DR11-C 767 750 to 767 754

UNIBUS Interface
Interrupt vector addresses Floating (see Appendix A)
(2 needed for each DR11-C)
Priority level BR5 (may be changed)
Bus loading 1 bus load

Mechanical
Mounting 1 SPC slot
Size Quad module

Input Current
.5A at +5V
(No current needed at −15V)

Miscellaneous
Inputs
One standard TTL unit load; diode protection clamps to ground and +5V.

Outputs
TTL levels capable of driving 8 unit loads except for the following:
NEW DATA READY = 30 unit loads
DATA TRANSMITTED = 30 unit loads
INIT (initialize) = common signal on both connectors driven by one 30-unit load driver.
Signals: NEW DATA READY—drives 30 units, positive pulse, 400ns wide unless width changed by an external capacitor.
DATA TRANSMITTED—drives 30 unit loads, positive pulse, 400ns wide unless width changed by an external capacitor.
INIT (initialize)—common signal on both connectors driven by one 30-unit load driver.
Data inputs

16-bit word from the external device.

Data outputs

16-bit word from the UNIBUS. Either a full word or an 8-bit byte (either high or low) may be loaded from the bus.

Maintenance Mode

A MAINT cable (supplied with basic system) jumpers the DROUTBUF outputs to the DRINBUF inputs and forces bits 15 and 7 to read as CSR1 and CSR0, respectively.
The DR11-K is a general purpose input/output interface capable of parallel transfer of up to 16 bits of data between a UNIBUS and an external device (or another DR11-K).

**FEATURES**
- 16 bits input and output
- Each input line can generate an interrupt
- recoverable over-voltage protection
- low cost

**DESCRIPTION**
The DR11-K General Device Interface is an integral logic module which forms a self-contained digital input-output interface between the PDP-11 UNIBUS and a user's peripheral. The DR11-K performs the tasks necessary to communicate with the PDP-11, so that the user's devices can be interfaced easily.

Under program control, the DR11-K permits bidirectional parallel transfer of up to 16 bits of information between a PDP-11 UNIBUS and a user's device or another DR11-K. All interfacing lines to and from the DR11-K are fused and have over-voltage protection.

Various options, which are hardware-selected by the user, are available for data input. Data can be read off a user's device either directly onto the UNIBUS or through the input register. The input register bits are transitionally set by its respective input line. Each of the input register bits can be hardware-selected to generate an interrupt to the UNIBUS.

The DR11-K can be used as an interprocessor buffer to allow two PDP-11 UNIBUS processors to exchange data.

The output lines are driven from a 16-bit output register. Information from the UNIBUS can be loaded into the output register in byte or word format. Following an exchange of control signals, the outputs are made available to the user's device. Once the external device accepts the data, a new transfer can be initiated. The output register can also be read to the UNIBUS.

The DR11-K also provides 16 lines of input for a transfer onto the UNIBUS. These signals can be hardware-selected to be read directly from the input lines or via the input buffer register. When going through the input buffer register each input line can be selected individually to interrupt the UNIBUS by simply presetting a
micro switch mounted on the interface. The four most significant bits (15-12) have additional input buffer-setting capabilities. Hardware-selectable, these buffer bits can be set by a negative input transition, a positive input transition, or by either a positive or a negative transition. The bidirectional transition setting allows an interrupt to occur on an input change. This added feature of bits 12 through 15 was specifically designed for interfacing to devices such as the Coulter Model “S” Blood Counter.

To transfer a word of data to the DR11-K, the external device places data on the input lines. The device, after allowing sufficient time for settling of transients, sends a pulse on the External Data Ready line. If the input interrupt enable (status register bit 06) is set, the External Data Ready pulse will generate an interrupt to the UNIBUS. When the input lines are read by the software, a control signal is generated by DR11-K, called Internal Data Accept. Once the external device receives this signal, new data can be transferred by repeating this operation. This method of interrupting is logically OR’d with the output of a circuit that allows for individual line interrupts.

After the data is loaded into the output register, a control signal is generated called Internal Data Ready High or Internal Data Ready Low, corresponding to a high- or low-byte transfer of data. If a full 16-bit word transfer is required, either line can be used. When the external device accepts the data, a control signal is sent back to the DR11-K, called External Data Accept. This then causes an interrupt to the UNIBUS if the output interrupt enable (status register bit 14) is set.

Input and output interrupts provide the ability to make vectored interrupt requests to the PDP-11 processor through two unique vector addresses. Interrupt enable/disable circuits are controlled by bits 14 and 6 of the addressable DR11-K status register.

The address selection logic determines if the interface has been selected for use, which register is to be used, when a word or byte operation is to be performed, and what type of transfer (input or output) is to be performed.

The interrupt control logic permits the interface to gain bus control and perform program interrupts to specific vector addresses. Interrupt enable bits are under program control; interrupt bits are under control of the external device.

The DR11-K interface logic consists of three registers: status register, input register, and output register. Operation is initialized
DR11-K

under program control by addressing the DR11-K to specify the register and the type of operation to be performed.

REGISTERS

Input Register
The input register is a 16-bit register that receives data from an external device for transmission to the UNIBUS. The external device places the data onto the DR11-K data input lines, where it is read by a DATI sequence either directly off the input lines or from the buffer register, depending on the option selected. There are two methods of interrupting: either by the control lines or by the buffer register bits (through their respective interrupt switches). If the control lines are used, the interrupt to the UNIBUS for a DATI sequence is produced by the External Data Ready line. When the data is read, the DR11-K notifies the external device on the Internal Data Accepted line. If the buffer register bits are used for interrupting, the interrupt to the UNIBUS for a DATI sequence is produced by presenting the correct transition on the input line that corresponds to the bit selected to interrupt. The input buffer register is bit-cleared by performing a write to the register with the bits to be cleared. In order to interrupt the UNIBUS, the input enable bit of the status register must be set; the bit is cleared when the UNIBUS accepts the interrupt. Any unused input line will read as a logical 0.

When the maintenance cable is used, the input register receives data from the output register rather than from the external device. This permits checking of the interface logic by loading a word from the bus into the output register and verifying that the same word appears in the input register.

Output Register
The output buffer is a 16-bit read/write register that may be read or loaded from the UNIBUS. Data can be loaded into this register under program control in either byte or word format. After the data is loaded, a pulsed signal (Internal High Data Ready or Internal Low Data Ready) permits the external transfer of data to either or both of two 8-bit devices. The output of the buffer is fed directly to the bus data lines. If 16-bit transfer is desired, either line can be used. When the external device has accepted the data, it sends back a pulsed signal (External Data Accepted), which causes an interrupt to the UNIBUS if the output interrupt enable bit (status register bit 14) is set. When the interrupt is accepted by the UNIBUS, the bit is cleared. The contents of the output register may be read at any time by means of a DATI.

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When the maintenance cable is used, the data from the output register are applied to the input buffer register, making it possible to check the operation of the interface logic.

**Status Register**
The status register is a 16-bit register, of which six bits are used for control and monitor functions. Two of these are flags that reflect the status of the DR11-K with respect to the external device, two are interrupt enable bits that interact with the UNIBUS of an interrupting condition, and two are used solely for maintenance to generate an interrupt to the UNIBUS.

The status register is used to enable interrupt logic, cause maintenance interrupts, and provide defined status functions from the external device. Input and output flags react to signals from the external device, two enable bits permit interrupts to occur when external signals are received, and two maintenance bits activate the interrupt logic.

- **Bit: 15**  
  **Name:** Output Flag  
  **Function:** This bit sets when External Data Accepted has been received from an external device.

- **Bit: 14**  
  **Name:** Output Interrupt Enable  
  **Function:** This bit enables an interrupt to occur when an External Data Accepted has been received. It is cleared when the interrupt is accepted by the UNIBUS.

- **Bit: 13**  
  **Name:** Set Interrupt Out  
  **Function:** This bit is used for maintenance only. When the DR11-K receives this bit, an output interrupt to the UNIBUS is generated.

- **Bit: 7**  
  **Name:** Input Flag  
  **Function:** This bit sets when an External Data Ready has been received from an external device.

- **Bit: 6**  
  **Name:** Input Interrupt Enable  
  **Function:** This bit enables an interrupt to occur when an external data ready has been received. It is cleared when the interrupt is accepted by the UNIBUS.

- **Bit: 5**  
  **Name:** Set Interrupt In  
  **Function:** This bit is used for maintenance only. When the DR11-K receives this bit, an input interrupt to the UNIBUS is generated.

All other bits are unused.
ADDRESSES
The DR11-K has floating addresses to allow the use of more than one DR11-K in a system, or to avoid device address conflict with other options.

DR11-K Address Assignments

<table>
<thead>
<tr>
<th>No. of DR11-Ks</th>
<th>Register Addresses</th>
<th>Vector Addresses</th>
</tr>
</thead>
<tbody>
<tr>
<td>DR11-K No. 0</td>
<td>16774-16770</td>
<td>300.304</td>
</tr>
<tr>
<td>DR11-K No. 1</td>
<td>167764-167760</td>
<td>310.314</td>
</tr>
<tr>
<td>DR11-K No. 2</td>
<td>167754-167750</td>
<td>320,324</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DR11-K No. 7</td>
<td>167704-167700</td>
<td>370,374</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DR11-K No. 15</td>
<td>167604-167600</td>
<td>470,474</td>
</tr>
</tbody>
</table>

SPECIFICATIONS

Input/Output Levels
logic 1 = 0V (less than 1.0V)  
logic 0 = +4V

Inputs 15:12 only Optionally redefined

Mechanical
Mounting One SPC slot
Size Hex module

Input Current
2.5A (2A (static) @ +5V

Environment
Operating Temperature +5°C (41°F) to 43°C (110°F)
Relative Humidity 20% to 80%, noncondensing

Miscellaneous
Inputs TTL-compatible
Over-voltage protection from –10Vdc to +15Vdc by 47-ohm fusible resistors that open when current exceeds 250mA.
Hysteresis for both high and low thresholds.

Outputs All driven by open collector logic.
Over-voltage protected and current protected by fuses that open when
current exceeds 250mA when in a zero state.

16-bit word from user's device.

16-bit word for UNIBUS, either as full word or 8-bit byte (either high or low).

A maintenance cable supplied with the DR11-K jumpers the output to the input register for testing.
The DR11-L and DR11-M are general purpose I/O interfaces designed to transfer two 16-bit words between a user’s device and a PDP-11 UNIBUS processor.

FEATURES
• high noise immunity
• buffer registers for temporary storage
• easy interface to user’s equipment

DESCRIPTION
The DR11-L and DR11-M are general purpose I/O interfaces that transfer two 16-bit words between a user’s device and a PDP-11 UNIBUS processor. Both interfaces feature switch-programmable device addresses, interrupt vector addresses, and bus request (BR) priority levels. Each word of each interface has a separate control and status register (CSR) with identical bit assignments. Interfacing to a user’s device is accomplished through the use of a simple handshake routine and 40-pin connectors. The handshake signals may be used with interrupt control for each word, or program control; data transfers can be accomplished without the handshake. Both interfaces are quad-height, extended-length, single-width modules, which can easily be integrated into PDP-11 processors. The interfaces may be used singly, to form a two-word input or two-word output interface, or in pairs.

Input transfers in the DR11-L and the DR11-M occur when the user’s device places 16 data bits and data ready on the lines to the DR11-L. DRDY IN latches the 16 data bits into a data buffer register. Under program control, the CPU reads the 16 data bits. Data Accept Out (DACC out) now notifies the user’s device that the data has been read.

DR11-L
The DR11-L two-word input interface features high impedance input receivers with high noise immunity and clamp diodes to limit the input voltage to +5V and ground. Two 16-bit latch buffer registers on the inputs provide temporary storage for the input words, freeing the user’s input device before the input words are accepted by the CPU. Inputs to the DR11-L can be two parallel 16-bit words or four parallel 8-bit bytes.

The interrupt capability of the DR11-L module can be utilized to gain use of the UNIBUS rather than waiting for the CPU to read
the input data. Interrupts can occur when DRDY IN latches the 16 data bits into the data buffer register. The DR11-L requests use of the UNIBUS through the BUS CONTROL lines, becomes bus master, and interrupts the program running in the CPU. The DR11-L then places a vector address on the data lines to the processor to indicate the starting address of a subroutine which contains instructions to read the data at the DR11-L data buffer register. DACC out notifies the user’s device that the data has been read.

The DR11-M two-word output interface features two read/write data buffer registers that can transfer two parallel 16-bit words or four parallel 8-bit bytes to the user’s device. Output drives on the DR11-M are capable of driving high voltage (30V) or TTL logic levels to meet user needs.

Output transfers are accomplished via the DR11-M interface. Under program control, the PDP-11 processor asserts the proper output data buffer register address to the DR11-M and places 15 DATA BITS in one of the two DR11-M output buffers. The DR11-M now asserts Data Ready Out (DRDY OUT) to notify the user’s device that data is available. After reading the data, the user’s device asserts Data Accepted In (DACC IN).

Output word transfers can also occur through requests from the user’s device, rather than waiting for the processor, by using the interrupt capability of the DR11-M. When the user’s device asserts DACC IN, the DR11-M requests use of the UNIBUS through the BUS CONTROL lines (BR, BG, etc.) becomes bus master, and interrupts the program running in the PDP-11. The DR11-M then places a vector address on the data lines to the processor to indicate the starting address of a subroutine which contains instructions to write data to the DR11-M output data buffer register. DRDY OUT is now asserted and the user’s device reads the 16 DATA BITS.

REGISTERS

DR11-L Control and Status Registers
The DR11-L input interface module has two CSRs, (one for each input word). Each CSR is a 16-bit register with three read/write bits. The CSRs provide the means through which the CPU commands and monitors interface operations.
Figure 8-2  DR11-L, DR11-M Interface Diagram
### Bit: 0
**Name:** Data Accepted Enable (DAE)
**Function:** 1 enables Data Accepted Out. When set to a 1, and if bit 1 is a zero, Data Accepted Out is produced. 0 disables Data Accepted Out. Set by initialize (INIT). Read/write.

### Bit: 1
**Name:** Data Latch (DL)
**Function:** Latches data into the data buffer register. Set by Data Ready In. Read only.

### Bit: 2
**Name:** CSR I.D.
**Function:** Identifies the CSR. 0 = CSR A. 1 = CSR B. Read only.

### Bit: 3
**Name:** Data Ready (DR)
**Function:** Indicates the status of the Data Ready In signal. 1 = DRI low. 0 = DRI high. Read only.

### Bit: 4
**Name:** P0
**Function:** With bit 5, indicates the selected BR priority level. Read only.

### Bit: 5
**Name:** P1
**Function:** With bit 4, indicates the selected BR priority level. Read only.

### Bit: 6
**Name:** Request Enable (RQE)
**Function:** 1 enables interrupt requests. 0 disables interrupt requests. Cleared by INIT. Read/write.

### Bit: 7
**Name:** Request (RQ)
**Function:** 1 generates interrupt request. Set by Data Ready. Cleared during the interrupt cycle, or whenever the data buffer is read or by INIT. Read only.

### Bit: 8
**Name:** Status Out (SO)
**Function:** User-defined output. 1 = low. 0 = high. Read/write.
Bit: 9  Name: V3
Function: Represents bit 3 of the base vector address. Read only.
Bit: 10 Name: V4
Function: Represents bit 4 of the base vector address. Read only.
Bit: 11 Name: V5
Function: Represents bit 5 of the base vector address. Read only.
Bit: 12 Name: V6
Function: Represents bit 6 of the base vector address. Read only.
Bit: 13 Name: V7
Function: Represents bit 7 of the base vector address. Read only.
Bit: 14 Name: V8
Function: Represents bit 8 of the base vector address. Read only.
Bit: 15 Name: Status In (SI)
Function: User-defined input. 1 = low. 0 = high. Read only.

DR11-M Control and Status Registers
The DR-11M output interface module has two CSRs, one for each output word. Each CSR is a 16-bit register with four read/write bits. The CSRs are the means through which the CPU commands and monitors interface operations.

Bit: 0  Name: Data Ready Enable (DRE)
Function: 1 enables Data Ready Out. When set to a 1, and if bit 1 is a one, Data Ready Out is produced. 0 disables Data Ready Out. Set by initialize (INIT). Read/write.
Bit: 1  Name: Data Ready (DR)
Function: Set when data is written into the data buffer register. Cleared by Data Accepted or by INIT. Read only.
Bit: 2  Name: CSR I.D.
Function: Identifies the CSR. 0 = CSR A, 1 = CSR B. Read only.
**Bit: 3**  Name: Data Accepted (DA)  
Function: Indicates the status of the Data Accepted In signal.  
1 = DAI low. 0 = DAI high. Read only.

**Bit: 4**  Name: P0  
Function: With bit 5, indicates the selected BR priority level. Read only.

**Bit: 5**  Name: P1  
Function: With bit 4, indicates the selected BR priority level. Read only.

**Bit: 6**  Name: Request Enable (RQE)  
Function: 1 enables interrupt request. 0 disables interrupt requests. Cleared by INIT. Read/write.

**Bit: 7**  Name: Request (RQ)  
Function: 1 generates interrupt request. Set by data accepted. Cleared during the interrupt cycle, or whenever data is loaded into the data buffer register, or by INIT. Read only.

**Bit: 8**  Name: Status Out (SO)  
Function: User-defined output. 1 = low. 0 = high. Read/write.

**Bit: 9**  Name: V3  
Function: Represents bit 3 of the base vector address. Read only.

**Bit: 10**  Name: V4  
Function: Represents bit 4 of the base vector address. Read only.

**Bit: 11**  Name: V5  
Function: Represents bit 5 of the base vector address. Read only.

**Bit: 12**  Name: V6  
Function: Represents bit 6 of the base vector address. Read only.

**Bit: 13**  Name: V7  
Function: Represents bit 7 of the base vector address. Read only.

**Bit: 14**  Name: V8  
Function: Represents bit 8 of the base vector address. Read only.

**Bit: 15**  Name: Status In (SI)  
Function: User-defined input. 1 = low. 0 = high. Read only.

**SPECIFICATIONS**  
**DR11-L**  
Physical  
Quad-height, extended-length, single-width module  

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DR11-L, DR11-M

Dimensions
Length—8 1/2 in., 21.6 cm
Width—1/2 in., 1.27 cm
Height—10 1/2 in., 26.7 cm

Weight
12 oz, 341 g

User Input Connections
Separate 40-pin connectors for each data word

Mounting Requirements
Plugs directly into any slot of a system mounting panel.

Electrical
Logic Power Requirements
+5V ±5% @ 1.5 A (nominal)

UNIBUS Loading
Presents 1 UNIBUS load

User Loading
Input Data Lines
Two TTL unit loads each
HIGH = Logic one
LOW = Logic zero

Input Control Lines
Five TTL unit loads each with hysteresis the same as the data lines.
HIGH = Logic zero
LOW = Logic one

Output Control Lines
35 TTL unit loads each
HIGH = Logic zero
LOW = Logic one

Module Type
M7864

Operational
Transfer Mode
Program-controlled with interrupts

Data Transfer
Two 16-bit words.

Environmental
Temperature
Storage: −40° to 66°C (−40° to 150°F)
Operating: 5° to 59°C (41° to 122°F)

Relative Humidity 10% to 95%
noncondensing

DR11-M
Physical
Quad-height, extended-length, single-width module

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### Dimensions
- Length—8 1/2 in., 21.6 cm
- Height—10 1/2 in., 26.7 cm
- Width—1/2 in., 1.27 cm

### Weight
- 12 oz, 341 g

### User Output Connections
- Separate 40-pin connectors for each data word.

### Mounting Requirements
- DR11-M plugs directly into any slot of a system unit mounting panel.

### Electrical
- Logic Power Requirements
  - +5V ± @ 1.5 A (nominal)

### UNIBUS Loading
- Presents 1 UNIBUS load

### User Loading
- Output Data Lines
  - 20 TTL unit loads each
  - HIGH = Logic one
  - LOW = Logic zero
- Input Control Lines
  - 5 TTL unit loads each
  - HIGH = Logic zero
  - LOW = Logic one
- Output Control Lines
  - 20 TTL unit loads each
  - HIGH = Logic zero
  - LOW = Logic one

### Transfer Mode
- Program-controlled with interrupts

### Data Transfer
- Two 16-bit words. One word at a time is transferred to each DR11-M output register. The output registers are word- and byte-addressable.

### Environmental
- Storage: $-40^\circ$ to $66^\circ$C ($-40^\circ$ to $150^\circ$F)
- Operating: $5^\circ$ to $50^\circ$C ($41^\circ$ to $122^\circ$F)
- Relative Humidity
  - 10% to 95% noncondensing
The DRS11 and the DSS11 modules provide 48 digital inputs and outputs for PDP-11 systems.

FEATURES
- 48 optically isolated inputs plus one interrupt—DSS11
- 48 buffered outputs, TTL or open collector, plus one interrupt (DRS11)
- RC input filters (optional)
- optically isolated output drivers (optional)
- screw terminal panel (optional)

DESCRIPTION
The DRS11/DSS11 input-output system enables users of PDP-11 systems to control up to 48 digital inputs and 48 digital outputs.
The options consist of two basic modules that are compatible with the small peripheral controller (SPC) slot. The output module, DRS11 provides 48 buffered outputs plus one RC filtered interrupt input. Up to 16 DRS11 output modules can be implemented on a system.

The input module, DSS11 provides 48 optically isolated inputs plus one optically isolated interrupt input. Up to 16 DSS11 controllers can be used on one system. One interrupt input is also available on each DSS11 module. All DSS11 input signals are optically isolated for system protection.

In addition to the basic modules, optional signal conditioning I/O modules and screw terminal panels can be added to the basic modules, enabling the configuration to meet the requirements of small industrial data acquisition and control systems.

All I/O controls and signals fit SPC slots. A screw terminal panel is available that allows easy access to signals brought into the system's control modules.

**Interface Registers**
The diagnostic program exercises control over the system, obtaining information from four registers on each of the control modules.

<table>
<thead>
<tr>
<th>Module</th>
<th>Control and Status Register</th>
<th>1st Data Register Out</th>
<th>2d Data Register Out</th>
<th>3d Data Register Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRS11</td>
<td>CSR-DRS</td>
<td>RG1-DRS</td>
<td>RG2-DRS</td>
<td>RG3-DRS</td>
</tr>
<tr>
<td>DSS11</td>
<td>CSR-DSS</td>
<td>RG1-DSS</td>
<td>RG2-DSS</td>
<td>RG3-DSS</td>
</tr>
</tbody>
</table>

These registers can be assigned UNIBUS addresses using the module switches. The CSR for each module will represent the address chosen, with the data registers being the next three sequential addresses. For example, if the switches were set for CSR address of 77500, the data registers would be: 775002, 775004, and 775006.

**Control and Status Registers**
The control and status registers for both the DRS11 and the DSS11 are identical.
DRS11, DSS11

**Bit: 6**  Name: Interrupt Enable
**Function:** Allows an interrupt when CSR bit 7 is set. Read/write.

**Bit: 7**  Name: Request
**Function:** Set when an external request occurs. An interrupt will occur if bit 6 is set when Request becomes true. Read only.

**Bit: 8**  Name: Request In Maintenance Mode
**Function:** Used when checking modules in maintenance mode. Setting simulates an external request whose function is identical to that of bit 7.

All other bits are unused.

**PROGRAMMING**
Programming for the DRS11 and the DSS11 is very straightforward. The DRS11 output bits are enabled to the user connections after the data registers have been loaded. They remain enabled until cleared by the program or by a system reset.

The DSS11 inputs are available to be read by the program almost immediately after being set by the user equipment. It is suggested, however, that these inputs be read only when the user external interrupt is generated. This external interrupt should be used to signal when the data has settled.

**SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Description</th>
<th>DSS11-A</th>
<th>DSS11-B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>48 inputs (TTL) plus one interrupt</td>
<td>48 inputs (24Vdc) plus one interrupt</td>
</tr>
<tr>
<td>Input voltage Range (ON state)</td>
<td>4-7V</td>
<td>24V ± 15%</td>
</tr>
<tr>
<td>Input current</td>
<td>7-21mA</td>
<td>16mA (nominal)</td>
</tr>
<tr>
<td>Isolation voltage</td>
<td>500V</td>
<td>500V</td>
</tr>
<tr>
<td>Prerequisite</td>
<td>PDP-11</td>
<td>PDP-11</td>
</tr>
<tr>
<td>Mounting</td>
<td>1 SPC</td>
<td>1 SPC</td>
</tr>
<tr>
<td>UNIBUS loads</td>
<td>one</td>
<td>one</td>
</tr>
<tr>
<td>Amps @ +5V</td>
<td>1.6</td>
<td>1.6</td>
</tr>
</tbody>
</table>
### DRS11, DSS11

#### INPUT SIGNAL CONDITIONING (DSS11-M)

<table>
<thead>
<tr>
<th>Description</th>
<th>DSS11-MP</th>
<th>DSS11-MR</th>
<th>DSS11-MS</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC filtered</td>
<td>RC filtered</td>
<td>RC filtered</td>
<td></td>
</tr>
<tr>
<td>contact sense</td>
<td>voltage sense</td>
<td>voltage sense</td>
<td></td>
</tr>
<tr>
<td>RC time constant</td>
<td>2msec(nominal)</td>
<td>2msec(nominal)</td>
<td>2msec(nominal)</td>
</tr>
<tr>
<td>Input volt</td>
<td>24V±15%</td>
<td>25V±15%</td>
<td>48V±10%</td>
</tr>
<tr>
<td>range (ON state)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input current</td>
<td>user-supplied</td>
<td>13mA @ 24V</td>
<td>13mA @ 48V</td>
</tr>
<tr>
<td>Contact</td>
<td>15mA(nominal)</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Current</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Prerequisite</td>
<td>DSS11-A</td>
<td>DSS11-A</td>
<td>DSS11-B</td>
</tr>
<tr>
<td>UNIBUS loads</td>
<td>none</td>
<td>none</td>
<td>none</td>
</tr>
</tbody>
</table>

#### DIGITAL OUTPUTS (DRS11)

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>DRS11-A</th>
<th>DRS11-B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type output</td>
<td>TTL driver</td>
<td>open collector</td>
</tr>
<tr>
<td>Output voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>capability (OFF state)</td>
<td>TTL</td>
<td>30V max</td>
</tr>
<tr>
<td>(ON state)</td>
<td>compatible</td>
<td>.7V @ 40mA</td>
</tr>
<tr>
<td>Output current</td>
<td>16mA @ .4V</td>
<td>40mA @ .7V</td>
</tr>
<tr>
<td>limitation limitation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Prerequisite</td>
<td>PDP-11</td>
<td>PDP-11</td>
</tr>
<tr>
<td>Mounting</td>
<td>1 SPC</td>
<td>1 SPC</td>
</tr>
<tr>
<td>UNIBUS loads</td>
<td>one</td>
<td>one</td>
</tr>
<tr>
<td>Amps @ +5V</td>
<td>2.5</td>
<td>2.5</td>
</tr>
</tbody>
</table>

#### OUTPUT SIGNAL CONDITIONING (DRS11-MP)

| DESCRIPTION         | 48 optically isolated dc drivers— one interrupt input |
| Type output         | open collector |
| Output voltage      | |
| capability (OFF state) | 50V max |
| ON state            | 1.0V max @ 75mA |
## DRS11, DSS11

<table>
<thead>
<tr>
<th>Specification</th>
<th>DRS11, DSS11 Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output current limitation</td>
<td>75mA @ 1.0V</td>
</tr>
<tr>
<td>Isolation voltage</td>
<td>500V max</td>
</tr>
<tr>
<td>Prerequisite</td>
<td>DRS11-B</td>
</tr>
<tr>
<td>Mounting</td>
<td>1 SPC slot next to DRS11-B</td>
</tr>
<tr>
<td>UNIBUS loads</td>
<td>none</td>
</tr>
<tr>
<td>Amps @ +5V</td>
<td>1.5</td>
</tr>
<tr>
<td>CSS</td>
<td></td>
</tr>
</tbody>
</table>

358
The IB11 is the IEEE bus interface to the UNIBUS.

FEATURES

- PDP-11 software compatible
- board-mounted, userconfigured switches that allow easy device (register address) and interrupt vector address selection

On the IEEE bus side of the interface, features include:

- instrument bus compatible with IEEE Standard #488-1975
- supports cable length up to 20m (65.6 ft) total
- 15 instruments (maximum) can connect to the bus

DESCRIPTION

The IB11 module plugs directly into any UNIBUS system backplane. A connector on the module connects directly with the IEEE bus via the IEEE cable supplied with the module. Devices that connect to the IEEE bus function either as “talkers,” “listeners,” or “controllers” or as a combination of the three functions. An instrument sending a message (of ASCII characters) is a talker, an instrument receiving a message is a listener.

The IEEE bus always has a system controller. The IB11 must perform this function; it can control all instruments connected to the IEEE bus in that system. The controller is capable of controlling talkers and listeners connected to the bus. The IB11 is both controller and controller-in-charge, scheduling all device polling, commands, and data byte transfers.

REGISTERS

The IB11 communicates with instruments connected to the IEEE bus under control of the program being executed. All communication between the UNIBUS and the IB11 is via the Instrument Bus Status (IBS) and the Instrument Bus Data (IBD) registers.

Instrument Bus Status Register

The IBS register provides the means for controlling the IEEE bus signals and the IB11 signals relative to the UNIBUS. Bits 0-7 are set and cleared by the program. Bits 8-15 cannot be set or cleared by the program.
Bit: 0  **Name**: Take Control Synchronously (TCS)
**Function**: Set and cleared under program control to enable or disable the IB11 controller-in-charge function by taking control synchronously or by negating the attention (ATN) bus line. Read/write.

Bit: 1  **Name**: End or Poll (EOP)
**Function**: Set and cleared under program control to set or clear the end or identity bus line (EOI).

Bit: 2  **Name**: Remote On (REM)
**Function**: Set and cleared under program control to set or clear the remote enable (REN) bus line. Must be set for the IB11 to control instruments on the bus.

Bit: 3  **Name**: Interface Bus Clear (IBC)
**Function**: When set by the program the interface clear (IFC) bus line is set for 125 μs (approximately). TCS is automatically set and IBC is cleared. This clears EOP, REM, LON, TON, ACC, LNR, TKR, CMD. Read/write.

Bit: 4  **Name**: Listener On (LON)
**Function**: Set by the program to enable or disable the IB11 listener function. Read/write.

Bit: 5  **Name**: Talker On (TON)
**Function**: Set by the program to enable or disable the IB11 talker function. Read/write.

Bit: 6  **Name**: Interrupt Enable (IE)
**Function**: Set and cleared by the program to enable or disable IB11 interrupts. Read/write.

Bit: 7  **Name**: Accept Data (ACC)
**Function:** Set and cleared by the program. When ACC is clear, reading a data byte from the data buffer will automatically set the bus DAC line and clear the LNR bit (bit 8). When ACC is set, the program must clear the low byte of the IBD register in order to clear the LNR bit and set the DAC bus line. Setting ACC when TON, LON, and TCS are all set sets the NRFD line. Read/write.

**Bit: 8 Name:** Listener Ready (LNR)

**Function:** When set, LNR indicates that the IB11 has a data or command byte that is ready for reading from the low byte of the IBD. LNR is set when LON is set and the DAV line becomes asserted.

**Bit: 9 Name:** Talker Ready (TKR)

**Function:** When set, TKR indicates to the processor that the IB11 is ready for the next data byte to be transmitted to the bus lines via the low byte of the IBD register. TKR is used for message bytes. Read only.

**Bit: 10 Name:** Command Done (CMD)

**Function:** When set, CMD indicates that the IB11 is ready for a byte to be transmitted to the bus lines via the low byte of the IBD register. CMD is set after TSC is set to indicate that the ATN bus line was set and that a command byte may be transmitted over the IEEE bus. Read only.

**Bit: 11 Name:**

**Function:** Not used—read as 0.

**Bit: 12 Name:**

**Function:** Not used—read as 0.

**Bit: 13 Name:** Error 1 (ER1)

**Function:** Set whenever a conflict occurs between the instrument bus ATN, IFC, or REN lines and their control hardware. Read only.

**Bit: 14 Name:** Error 2 (ER2)

**Function:** Set when the IB11 tries to send a data or command byte while there is no active listener or command accepter on the instrument bus.

**Bit: 15 Name:** Service Request (SRQ)

**Function:** This bit always indicates the status of the IEEE bus SRQ line. It may be written (set and cleared) if the ER1 inhibit switch is set.
Instrument Bus Data Register

Bit: 15-8  Name: IEEE bus control line status
Function: The program can monitor the signal status of all eight control signals by reading this byte. Note that DAC (bit 08) and RFD (bit 10) are inverted with respect to the actual IEEE bus signal lines.

Bit: 7-0  Name: Instrument bus data input/output
Function: The program can read or write via this register byte to receive or transmit command or data bytes over the instrument bus. Bits 7-0 correspond to DIO bus lines 8-1.

SPECIFICATIONS

Power Requirements  +5 V ±5% 0.8 A typical (1.5 A maximum)

Mechanical
Height  13.2 cm (5.2 in.)
Length  22.8 cm (8.9 in.)
Width  1.27 cm (0.5 in.)

Environmental
Temperature
  Storage  −40° to 60° C (−40° to 140° F)
  Operating  50° to 50° C (41° to 122° F)
Relative Humidity  10% to 95% (no condensation)
The IEC11-A Bus controller is a hex card that plugs directly into a SPC slot in a PDP-11 UNIBUS computer backplane and produces a IEEE 488-1975 instrumentation bus.

**FEATURES**
- provides a simple means of interfacing instrumentation equipment to a PDP-11 UNIBUS computer
- designed to meet IEEE 488-1975 specifications
- Bus tester option is available

**DESCRIPTION**
In the past, interfacing instrumentation equipment to computers for measurement and test applications was complex and costly. Each instrument had its own interface, interface diagnostic, and, if an operating system was used, its own software handler.

The IEEE-Bus is a means of simplifying the interfacing of instrumentation equipment by providing a standard data bus to which a user can simply plug in up to 15 instruments of any type or manufacture (providing that the instruments have an IEEE-Bus interface connection).

The IEC11-A is a single hex card that plugs directly into an SPC slot in a PDP-11 computer backplane and produces an IEEE-Bus which meets the IEEE Standard 488-1975 specification.

A special adaptor cable is supplied, which connects to the IEC11-A and provides a standard IEEE-Bus connector (i.e., CINCH 57-10240) ready to connect to the first instrument to be interfaced. Other equipment is then simply connected to the bus in a “daisy chain” fashion when required.

![Figure 8-4](image)

The IEEE-Bus addition to the PDP-11 UNIBUS family makes computer power more easily attainable for the production engineers who cannot justify the expense of turnkey systems for specific projects, or who need more generalized test capabilities than the turnkey systems can offer.
Some specific uses:
- flexible production test systems for rapidly changing product lines
- computer control of test instrumentation to automate testing and to receive timely data and trend plotting
- automatic calibration and record keeping of test instrumentation
- in-process quality control product testing
- parametric testing of electrical components and assemblies for incoming QC where flexibility is essential

The growing availability of test stimulation data acquisition devices that are compatible with the IEEE standard is making a much easier situation for the system user. The concept of building computer-operated test systems out of instrument building blocks has become a reality now that the building blocks are compatible with each other and with the computer.

The IEC11-A interface allows scientific researchers to automate instrumentation easily in the laboratory. The IEC11-A offers a standard bus for interfacing the PDP-11 UNIBUS to a large variety of laboratory instruments.

Major instruments such as scanners, programmable power supplies, spectrum analyzers, function generators, and many others used for test and measurement now have the IEEE Standard Digital Interface option. The IEEE Standard Digital Interface standard bus
has to date been incorporated by at least fifty major instrument manufacturers and is recognized internationally.

The IEC11-A allows the full power of a general purpose computer running a high level programmable language to talk to laboratory instrumentation without complicated interface consideration.

The IEC11-A provides the following IEEE defined functions:

- system controller
- controller-in-charge
- talker
- listener

Each IEEE-Bus system must have one and only one system controller that is able to activate IFC (Interface Clear) and/or REN (Remote Enable) to the bus.

Asserting IFC forces the IEEE-Bus system to halt, thereby allowing an orderly start or restart.

An IEEE-Bus system may have several controllers. However, only one of them can be assigned as the controller in charge. When active, the controller in charge may issue commands and address bytes via the bus. The talker and the listener function may be activated by the controller in charge.

The IEC11-A is able to conduct parallel poll (PP) and may respond to or activate service request (SR). In addition, the interface may activate the functions Remote/Local (RL), Device Clear (DC) and Device Trigger (DT) in the devices connected to the IEEE-Bus.

The IEC11-A communicates with the PDP-11 by program control using program interrupts. UNIBUS address, interrupt vector and IEC device address are selectable by switches. Interrupt priority may be selected by a priority plug.

**SPECIFICATIONS**

**Mechanical**

<table>
<thead>
<tr>
<th>Description</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module</td>
<td>1 hex board</td>
</tr>
<tr>
<td>Mounting requirements</td>
<td>1 hex SPC slot in a system unit</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>0°C to 55°C</td>
</tr>
<tr>
<td>Relative humidity</td>
<td>95% (noncondensing)</td>
</tr>
<tr>
<td>Weight</td>
<td>1 kg</td>
</tr>
<tr>
<td>IEC cable length</td>
<td>Up to 20 meters</td>
</tr>
<tr>
<td>IEC adaptor cable</td>
<td>2.5m</td>
</tr>
</tbody>
</table>

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IEC11-A

**Electrical**
- Power consumption: 2.5A; +5V
- Logic levels: TTL
- UNIBUS loads: One
- IEEE-Bus loads: One
- Number of IEEE-devices: Up to 15

**Operational**
- Registers: Four 16 bit registers
- Operating mode: Program transfer with interrupt
- Interrupt level: 4...7 selectable
- IEEE interface functions (Subsets):
  - Talker (TL)
  - Listener (L1)
  - Acceptor Handshake (AH1)
  - Source Handshake (SH1)
  - Service Request (SR1)
  - Control (C1, 2, 3, 4, 5)

CSS
The KW11-K is a dual programmable real-time clock option used in PDP-11 UNIBUS computers.

FEATURES

Clock A
- 16-bit counter
- 16-bit programmable preset/buffer register
- four modes of operation
- two external inputs (Schmitt trigger)
- eight program-selectable clock rates
- five clock frequencies

Clock B
- 8-bit counter
- 8-bit programmable register
- one external input (Schmitt trigger)
- seven program-selectable clock rates
- five clock frequencies

DESCRIPTION

Clock A is a 16-bit programmable real-time clock that can accurately measure and count intervals of time and events. It can be used for processor synchronization to external events, to generate events, such as an A/D conversion at programmed intervals, and to generate events synchronized to an external event input. Clock A is controlled by the A status register which consists of enables, flags, and mode and rate selections.

Clock A operates in one of four programmable modes: single interval, repeated interval, external event timing, and external event timing from zero base. Clock A can be program-selected to operate at one of eight clock rates. The clock can operate from one of five crystal-controlled frequencies (1 MHz, 100 kHz, 10 kHz, 1 kHz and 100 Hz), an external (Schmitt Trigger One) input, line frequency or the overflow of Clock B (allowing a further dimension in Clock A input frequency selections).

Clock B is an 8-bit programmable real-time clock that can accurately time intervals or events. It can be used for generating interrupts at programmed intervals, for generating events (such as an A/D conversion) at programmed intervals, or for providing an input
SENSOR I/O DEVICES

KW11-K

frequency to Clock A. Clock B is controlled by the B status register which consists of flags, enables, and rate selections. Clock B operates in one mode: repeated interval mode. Clock B can be program-selected to operate at one of seven clock rates, one of five crystal-controlled frequencies (2 MHz, 100 kHz, 10 kHz, 1 kHz and 100 Hz), line frequency, or external (Schmitt Trigger Three) input. An eighth selection is used as a stop frequency.

The KW11-K has three Schmitt trigger inputs which have threshold and slope control.

The KW11-K, when used in conjunction with an A/D converter that provides for an external A/D start, has the ability to perform sampling on a high frequency repetitive analog signal at effective rates as high as 1 MHz.

REGISTERS
The KW11-K has a floating address to allow the use of more than one KW11-K in a system or to avoid any device address conflicts with other options. The register address is selected by switches on the module representing address lines A12 through A05. The standard register addresses selected for the KW11-K are:

Clock A:
A Status Register     R/W     770404
A Buffer Register     R/W     770406
A Counter Register   Read only 770430

Clock B:
B Status Register     R/W     770432
B Buffer Register     R/W     770434
B Counter Register   Read only 770436

Status Register A

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Bit: 15  Name: ST1 Flag
Function: This flag sets when a Schmitt Trigger one (ST1) event or a maintenance ST1 has occurred.

Bit: 14  Name: ST1 Interrupt Enable
Function: This status bit enables an interrupt to be generated if an ST1 event has occurred.

Bit: 13  Name: ST1 Enable Counter
Function: This status bit enables the Enable Counter A (status bit 00) to be set when an ST1 event has occurred.

Bit: 12  Name: Status
Function: For maintenance purposes, this status bit generates an ST1 event.

Bit: 11  Name: Status
Function: For maintenance purposes, this status bit generates a 1 MHz clock pulse in Clock A.

Bit: 10  Name: Status
Function: For maintenance purposes, this status bit generates an ST2 event.

Bit: 9-8  Name: Mode
Function: These mode bits select the mode of operation of Clock A.

0 0  Single Interval mode—Counter counts from preset value to overflow, sets mode flag, sets overflow flag, and stops. Overflow generates A event output.

0 1  Repeated Interval mode—Counter counts from preset value to overflow, sets mode flag, sets overflow flag, transfers buffer to counter register, and begins again. Overflow generates A event output.

1 0  External Event Time mode—The counter is free running at the selected rate and a pulse from Schmitt Trigger Two transfers contents of the counter register to the buffer regis-
SENSE I/O DEVICES

KW11-K

ter, sets mode flag, and continues counting.

1 1

External event time mode from zero base—The counter is free-running at the selected rate and a pulse from ST2 transfers contents of counter register to buffer register, sets mode flag, clears the counter, and continues counting from zero.

Bit: 7  Name: Mode Flag
Function: This status sets on overflow or when a counter to buffer transfer occurs.

Bit: 6  Name: Mode Flag Interrupt Enable
Function: This status bit enables an interrupt to be generated when the mode flag sets.

Bit: 5  Name: A Overflow Flag
Function: This status bit sets when an overflow from counter A occurs.

Bit: 3-1  Name: Rate
Function: These status bits select the rate at which Clock A operates:

<table>
<thead>
<tr>
<th>Clock A</th>
<th>03</th>
<th>02</th>
<th>01</th>
</tr>
</thead>
<tbody>
<tr>
<td>No rate or B Overflow</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1 MHz</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>100 kHz</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>10 kHz</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1 kHz</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>100 Hz</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>STP1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Line Frequency</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Bit: 0  Name: Enable Counter A
Function: When this status bit is set, Clock A is enabled to count at the selected rate. This bit is set by either the status register or by an ST1 event and ST1 Enable (bit 14).
Status Register B

Bit: 15-12 Name: Not used.

Bit: 11 Name: Maintenance
Function: This status bit disables the 1 MHz oscillator (Clock A) that is used to generate the other crystal-controlled frequencies of Clock A.

Bit: 10 Name: Maintenance
Function: For maintenance purposes this status bit generates a Clock A interrupt.

Bit: 9 Name: Maintenance
Function: For maintenance purposes this status bit generates a Clock B interrupt.

Bit: 7 Name: B Overflow Flag
Function: This status bit sets when an overflow from counter B occurs.

Bit: 6 Name: B Overflow Interrupt Enable
Function: This status bit enables an interrupt to be generated when a B overflow occurs.

Bit: 5 Name: Feed B to A
Function: If Clock A is selected for rate 0, the overflow of Clock B is used as the clocking frequency of Clock A.

Bit: 4 Name: Auto-Increment Mode
Function: When this status bit is set, buffer register A is decremented in 2's complement when an A overflow occurs. When an ST2 occurs, internal KW11-K clock timing is synchronized to it.

Bit: 3-1 Name: Rate
Function: These status bits enable the rate at which Clock B is to operate:
Clock B 03 02 01
No rate 0 0 0
1 MHz 0 0 1
100 kHz 0 1 0
10 kHz 0 1 1
1 kHz 1 0 0
100 Hz 1 0 1
STP 3 1 1 0
Line Frequency 1 1 1

Bit: 0  Name: Enable Counter B
Function: When this status bit is set, Clock B is enabled to count at the selected rate.

A and B Counters
The A counter is a 16-bit (word-oriented) counter. It is a read-only register, and can be read while in operation.

The B counter is an 8-bit (low byte) counter. It is a read-only register that can be read only when the counter is not enabled.

Preset/Buffer Register and B Preset Register
The A preset/buffer register is 16-bit (word-oriented) register that can be written into or read while Clock A is in operation.

The B preset register is an 8-bit (low-byte) register that can be written or read, but not while Clock B is in operation.

SPECIFICATIONS
Power Requirements ±5 Vdc at 3 A (max)
DESCRIPTION
The KW11-L Clock divides time into intervals of $16\frac{2}{3}$ msec or 20 msec, determined by the line frequency, 60 Hz or 50 Hz. The accuracy of the clock period is that of the frequency source.

There are two modes of operation:

**Interrupt Mode:** An interrupt is generated for each cycle of the line frequency.

**Non-Interrupt Mode:** The program checks a Monitor bit for timing information.

**Clock Status Register (LKS) 777 546**

![Clock Status Register Diagram]

Effect of the Initialize (INIT) signal: clear bit 16, set bit 7.

**Bit:** 7  **Name:** Monitor  
**Function:** Set by the line frequency clock signal and cleared by the program.

**Bit:** 6  **Name:** Interrupt Enable  
**Function:** Set to allow Monitor = 1 to cause an interrupt. Determines mode of operation; 1 = interrupt, 0 = noninterrupt.

SPECIFICATIONS

**Main Specifications**

<table>
<thead>
<tr>
<th>Time intervals</th>
<th>$16\frac{2}{3}$ msec at 60 Hz line frequency, 20 msec at 50 Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating modes</td>
<td>Interrupt, noninterrupt</td>
</tr>
<tr>
<td>Register address</td>
<td>(LKS) 777 546</td>
</tr>
</tbody>
</table>

**UNIBUS interface**

<table>
<thead>
<tr>
<th>Interrupt vector address</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Priority level</td>
<td>BR6</td>
</tr>
<tr>
<td>Bus loading</td>
<td>1 bus load</td>
</tr>
<tr>
<td></td>
<td>373</td>
</tr>
<tr>
<td><strong>Mechanical</strong></td>
<td></td>
</tr>
<tr>
<td>---------------</td>
<td>---</td>
</tr>
<tr>
<td>Mounting</td>
<td>Within main CPU assembly</td>
</tr>
<tr>
<td>Size</td>
<td>1 single height module</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>0.8 A at +5V</td>
</tr>
</tbody>
</table>
FEATURES
• four clock rates, program-selectable
• crystal-controlled clock for accuracy
• two external inputs
• three modes of operation
• interrupts at 50 or 60 Hz line frequency

DESCRIPTION
The KW11-P Clock provides programmed real-time interval interrupts and interval counting in three modes of operation. The major functional units of the Clock include:

16-bit Counter: Counts up or down at four selectable rates and can be read while operating. The interrupt sequence is initiated at zero (underflow) during a countdown from a preset interval count. The count-up mode is used to count external events; an interrupt is initiated at 177 777 (overflow).

16-Bit Count Set Buffer: Stores the preset interval count. At underflow, depending on the operating mode, the buffer automatically reloads the Counter or is cleared.

Control and Status Register: Provides various control and status signals related to the operation of the buffer and counter.

Clock: Provides 2 crystal-controlled signals of the 100 kHz and 10 kHz to clock the counter. Two external clock inputs are provided: 50/60 Hz line frequency and a TTL-compatible signal input.

MODES OF OPERATION
Single Interrupt Mode: A program-specified time interval is present and an interrupt is generated at the end of the interval. The time interval, represented as a specific count, is loaded into the counter. Countdown or count up is initiated at one of four selectable rates; at underflow or overflow an interrupt is generated, clocking is stopped, and the counter is reset to zero.

Repeat-Interrupt Mode: A program-specified time interval is present and repeated interrupts are generated at a rate corresponding to the time interval. Operation is similar to the Single-Interrupt Mode, except that after the interrupt is generated on underflow or overflow, the counter is automatically reloaded from the control-set buffer and clocking is restarted. At the next underflow or overflow, another interrupt is generated.

External Event Counter Mode: The external input is used to clock
the counter in the count-up or countdown mode. The counter may be read during operation to determine the number of events that have occurred.

REGISTERS
Control and Status Register 772 540

Bit: 15  Name: Error
Function: Set when, in repeat-interrupt mode, a second underflow or overflow occurs before the interrupt of the preceding one has been serviced. It is cleared when the Status Register is addressed and by internal gating. It is valid only during the first serviced interrupt after the error.

Bit: 7  Name: Done
Function: Set on underflow or overflow.

Bit: 6  Name: Interrupt Enable
Function: Set to allow Done = 1 to cause an interrupt.

Bit: 5  Name: Fix
Function: Set to cause single clocking of the counter as a maintenance aid.

Bit: 4  Name: Up/Down
Function: Selects either count-up or countdown for the counter; 1 = up, 0 = down.

Bit: 3  Name: Mode
Function: Selects interrupt mode of operation; 1 = Repeat Interrupt, 0 = Single Interrupt.

Bit: 2-1  Name: Rate Select
Function: Selects one of four available clock rates.
**SENSOR I/O DEVICES**

**KW11-P**

<table>
<thead>
<tr>
<th>Rate</th>
<th>Bit 2</th>
<th>Bit 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 kHz</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>10 kHz</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Line frequency</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>External</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Bit**: 0  **Name**: Run

**Function**: Set to allow the counter to count. Cleared on underflow in single-interrupt mode.

**Count Set Buffer Register 772 542**
This 16-bit register is used for storage of the interval count. It allows automatic reloading of the Counter in repeat-interrupt mode. The register is cleared by the INITIALIZE signal and by underflow or overflow in the single interrupt mode. The bits are write-only.

**Counter Register 772 544**
This 16-bit register is a binary up/down counter. It is cleared by the INIT (initialize) signal. The bits are read-only.

**PROGRAMMING**
Read the counter prior to stopping it. Stopping the counter might change its contents. If it is necessary to start the counter from a previous value, save the value which was read and reload if required. Do not loop on a counter-read command.

The latest version is equipped with a hardware synchronization feature which will add from zero up to one clock interval (of the selected rate), to the anticipated count time on the first interrupt after the run bit is asserted.

**SPECIFICATIONS**

**Main Specifications**

- **Clock rates**
  - 100 kHz, 10 kHz crystal-controlled, line frequency, external (Schmitt Trigger input), oscillator stability: ±0.01%

**Operating Modes**
- Single interrupt, repeated interrupt, external event counter, non-interrupt

**Register Addresses**

- **Control and Status** 772 540
- **Count Set Buffer** 772 542
- **Counter** 772 544

377
<table>
<thead>
<tr>
<th>UNIBUS Interface</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt vector address</td>
<td>104</td>
</tr>
<tr>
<td>Priority level</td>
<td>BR6</td>
</tr>
<tr>
<td>Bus Loading</td>
<td>1 bus load</td>
</tr>
</tbody>
</table>

**Mechanical**

| Mounting                  | 1 SPC slot (quad module) |

**Power**

| 0.5 A at +5V               |       |
The KW11-W is a general purpose watchdog timer that provides a monitoring facility for a PDP-11 UNIBUS system.

**FEATURES**
- three timers to monitor systems program
- automatic monitoring of power supply
- input and output facilities provided for users equipment

**DESCRIPTION**
The KW11-W is a general purpose watchdog timer that provides a PDP-11 UNIBUS system with a monitoring facility. The KW11-W includes three individual timers, designated T1, T2 and T3; all of these are reset each time the module is addressed by the systems program.

T1 specifies the minimum repetition rate at which the user program addresses the unit; T2 is known as a warning which indicates that T3 is about to time out; T3 is the actual watchdog timer which, upon timing out, operates an output relay, and causes an alarm signal to be generated.

The KW11-W can be configured to provide many possible applications. A simple application might be to use the KW11-W to monitor a computer's power supply. If computer power is lost, the relay contact outputs can be used to energize an external alarm.

In a dual processor configuration, two KW11-Ws can be connected back-to-back to facilitate failure detection and auto changeover. The alarm output of each unit is connected to the receive input of the other watchdog. If a failure of Processor A occurs, and its watchdog times out, the alarm output can be used to signal Processor B via its watchdog timer to perform a switch-over and assume system control.

The KW11-W’s three timers (one-shot multivibrators) are all reset simultaneously by a clock pulse which is produced each time the KW11-W control and status register is addressed by the system’s program. The time-out delays can be adjusted by the user by the selection of suitable timing components. In the normal mode of operation, T1 < T2 < T3.

**T1—Short Loop Timer**
This timer ensures that the KW11-W is not readdressed within
a defined period. If it is readdressed within that period, an error condition results which inhibits T2 from requesting an interrupt, and terminates T3, which in turn releases the watchdog relay (normally closed), causes a watchdog alarm to be generated, and also causes an interrupt to be produced (providing the interrupt is enabled).

T2—Second Chance Timer
T2 functions primarily as a software aid. Upon timing out, it causes an interrupt to be generated which indicates that the main watchdog (T3) is about to time out and should, therefore, be readdressed. Hence the unit may be addressed by a systems program in one of two ways:

a. By addressing the KW11-W regularly after a defined period has elapsed.

b. By addressing the KW11-W immediately after receiving an interrupt generated by T2’s timing out.

T3—Watchdog Timer
T3 is the main watchdog timer; if it times out, a systems error condition results which then releases the watchdog relay, and causes a watchdog alarm to be generated (providing that it is not inhibited externally).

Watchdog Alarm
A 5 ms pulse which is produced immediately following T3’s timing out or an error from T1 is called the watchdog alarm. This output can be utilized for:

• connection to receive input on a second KW11-W
• to trigger the user’s alarm circuitry

A watchdog relay is a single pole change over relay, whose contacts are available to the user. The relay is connected to the output of a latch circuit which ensures that the relay, once de-energized, remains in that condition until reset. In this way multi-error pulses occurring at its output are prevented. The relay is de-energized at power up, and whenever an error signal is generated (by a T1 error or by T3’s timing out), it can be re-energized under computer control, providing it is not inhibited by an external latch.

Its output can be utilized for:

• control of audible/visible alarm indication equipment

• automatic changeover from computer control to manual control of a system
Inputs
Signal conditioning (for either 6V, 24V, or 48V), optical isolation, contact bounce filtering, and a Schmitt trigger are provided on each input to the KW11-W, thus enabling the unit to be connected directly to a wide variety of remote user devices. The input signals available to the user are as follows:

Latch Input
This input can be used to inhibit the watchdog relay from being re-energized.

D15 and D07 Inputs
These are status inputs that can be read by the system programmer whenever required.

Receive Input
The receive input can also be considered a status input. However, when the input transitions from high to low, an interrupt is generated. This input could, for example, be used with a second KW11-W in multiprocessor configuration.

Options
KW11-Y
This option includes the KW11-W watchdog timer, a control panel which contains a sonic alarm, an alarm inhibit switch, and user access points to the KW11-W functions.

KW11-YZ
The KW11-YZ is a watchdog timer option that includes the KW11-W watchdog timer, an integrated $5\frac{1}{4}$" cover panel which contains the sonic alarm and alarm inhibit switch, but with no user access points to the KW11-W functions.

Figure 8-5  KW11-W System
REGISTERS
The KW11-W is controlled from the CPU by four addressable registers.

Watchdog Control and Status Register 772400

Bit: 15  Name: T1, Short Loop
Function: Set to a 1 if the KW11-W is readdressed before T1 times out. An interrupt is generated if enable interrupts (bit 6) is also set. This bit is cleared by the initialize and clear flag signals. Read only.

Bit: 14  Name: Receive Flag
Function: Under control of the user’s device and set to a 1 when enabled. An interrupt is generated if enable interrupts (bit 6) is also set. Bit 14 is cleared by the initialize and the clear receive flag signals. Read only.

Bit: 8   Name: Clear Receive Flag
Function: When set to a 1, this bit clears the receive flag (bit 14). Write only.

Bit: 7   Name: Second Chance
Function: If T2 times out, this bit is set to a 1. Once set, it can be used as a warning to the program that watchdog (T3) is about to time out. An interrupt is generated if enable interrupts (bit 6) is also set. This bit is cleared by the initialize and the clear flag signals. Read only.

Bit: 6   Name: Enable Interrupts
Function: When set, this bit allows an interrupt to be generated if T1 (bit 15), receive flag (bit 14), or T2 (bit 7) becomes set. Bit 6 is cleared by the Initialize signal. Read only.

Bit: 1   Name: Enable Timer
Function: When set to a 1, this bit enables the output stage of watchdog (T3). This bit is cleared by the trailing edge
of the 5-ms error pulse and the internally generated power clear pulse on POWER-UP only. Write only.

Bit: 0  Name: Start Time
Function: When set to a 1, this bit starts the timer. Write only.

Clear Flags Register 773402
This commands clears bit 15 and bit 7 in the watchdog clear and status register.

External Control and Status Register 772404
Bit: 15  Name: D15
Function: Input bit used to monitor external device status.
Bit: 7  Name: D07
Function: Input bit used to monitor external device status.

All other bits are unused.

Switch Relay Register 772406
Bit 0 energizes the output relay, all other bits are unused.

SPECIFICATIONS

Mechanical
Logic Mounting 1 SPC slot in PDP-11 backplane

Electrical
Power Requirements +5V (±.25V) at 1.3A
−15V (±.75V) at .05A
Power Dissipation 12W at 48V
Logic Levels TTL
UNIBUS Loads One

Operational Inputs (optically isolated)
Input Levels 6V, 24V, 48V nominal
(selected by jumpers)
Input Current +13 mA to +2 mA = Logic 1
−2 mA to +2 mA = Logic 0
Input Response Time 2.5 ms max. normal
(6V step input) 500 µs max. optional
Input Rate 200 Hz max. normal
(6V step input) 1 kHz max. optional
Common Mode 10(**)10 ohms
Input Impedance

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### Operational Outputs

**Relay Output**
- Form C
- 28Vdc or 250 mA (3VA max)

**Solid State Output**
- Open Collector
- 55Vdc or 100 mA (.3W max)

### Timing

**T1, Short Loop**
- 1.5 ms to 10 ms

**T2, Second Chance**
- 180 ms to 1.5 sec.

**T3, Watchdog**
- 180 ms to 1.5 sec.

**T4, Error Pulse**
- 5 ms \(\pm 30\%\)

### Environment

**Operating Temperature**
- 50° to 122°F (10° to 50°C)

**Relative Humidity**
- 20% to 95% (no condensation)

**CSS**
The LPA11-K is an intelligent direct memory access (DMA) controller for DIGITAL's laboratory data acquisition I/O devices. It is intended for use in applications where I/O loads in excess of 2-5 kHz are expected, and where there is a requirement for multi-programming or concurrent data processing.

FEATURES

- Direct Memory Access control of DIGITAL laboratory interfaces; A/D, D/A and digital I/O.
- High performance analog and digital I/O in a multi user environment.
- Only one interrupt per buffer of data transferred permits high speed A/D or D/A data processing with minimal CPU overhead.
- Full FORTRAN, FORTRAN IV PLUS, BASIC and MACRO support under RSX11-M and VMS.
- Programming is accomplished via Direct Memory Access to Command Tables.
- Silo (first in, first out) memory internal to the LPA11-K subsystem allows data to be transferred continuously without interruption, regardless of buffer switching, status reporting, CPU bus latencies, or system software latencies.
- Shared use of I/O resources among up to eight users.

DESCRIPTION

The LPA11-K is an intelligent controller and data mover that transfers 16-bit words between PDP-11 memory and specified analog-to-digital, digital-to-analog or digital I/O devices. It is a fast, flexible, easy to use microprocessor subsystem which allows analog data acquisition and data reduction at high throughput rates.

By using the LPA11-K, multiple users can share analog-to-digital converters, digital-to-analog converters, real-time clocks, digital input and digital output. Interactions with these peripherals is performed by the microprocessors, freeing the host PDP-11 from the overhead of the interrupt service routines normally associated with these devices.

To effectively serve a variety of applications, the LPA11-K operates in two distinct modes: dedicated mode and multi request mode.

In Dedicated Mode the LPA11-K performs high-speed analog input or output for a single user. In Multirequest Mode the LPA11-K
LPA11-K

allows up to eight, simultaneous users to perform I/O at individual rates from any combination of the supported device types. Each user programs the LPA11-K as if the user had sole access to it. Starting and stopping of requests from a given user does not affect the other active LPA11-K requests.

Because the LPA11-K transfers data and control information using non-processor requests (NPRS), the interrupt load on the host PDP-11 is almost completely eliminated. This allows real-time data reduction to occur simultaneously with the data acquisition and makes high speed real-time I/O feasible under multi-user operating systems. This significantly increases the PDP-11 processor power available for application programs. In addition, previously unobtainable high throughput rates can be continuously maintained without data loss.

In situations where higher throughput is required, multiple LPA11-Ks can be included in the system. The total number depends on the individual application, but generally up to four LPA11-Ks can be active concurrently.

LPA11-K Architecture
The LPA11-K is implemented using two, 300-nanosecond microprocessors. The first microprocessor is identified as the master. The second microprocessor is called the slave. The PDP-11 is known as the host.

The host PDP-11 is responsible for initializing the LPA11-K, sending requests to start and stop sampling of data, and for handling errors and other status conditions. The master microprocessor is responsible for all transactions between the PDP-11 and the LPA11-K. These include control information as well as storage and retrieval of all data from the PDP-11 main memory. The slave microprocessor is responsible for all control of the physical laboratory data acquisition peripherals. The slave microprocessor accepts “start data acquisition” commands from the master microprocessor and then sends (or receives) a continuous stream of data until a stop command is noted or a fatal error condition occurs.

The master and slave are connected by the inter-microprocessor buffer module. This module buffers all transactions between the microprocessors with two, 64-byte first-in-first-out silo registers. This allows the two microprocessors to operate asynchronously and independently. The inter-microprocessor buffer also provides the necessary control signals for the slave microprocessor to communicate with the laboratory data acquisition peripherals.
**Channel Address Selection**

In both dedicated mode and multirequest mode there is a need to specify the address of the next channel to be sampled. In the case of analog input, the channel address specifies which channel of a multiplexer to enable. In the case of digital I/O, the channel address specifies which digital I/O word to access. Three types of channel address selection are provided by the LPA11-K: single-channel mode, sequential-channel mode, and random-channel mode.

In **single-channel mode**, the LPA11-K repeatedly samples the same channel. This is the simplest mode and allows the highest throughput.

In **sequential-channel mode**, the LPA11-K calculates the address of the next channel by adding a user-supplied positive or negative increment to the current channel. When the last channel is sampled, the LPA11-K resets the current channel to the start channel. This allows users to scan a pre-selected range of channels without introducing significant overhead in the process.

In **random-channel mode**, the LPA11-K determines the address of the next channel by accessing a user-supplied table in the host PDP-11’s main memory. This is the most general of the channel address selection modes since channels can be sampled in any sequence, but results in a lower aggregate throughput rate.
Storage of Data in PDP-11 Memory

In Dedicated Mode and for each of the possible eight users in Multirequest Mode, up to eight independent buffer addresses can be specified for each user. The LPA11-K maintains each user's buffers separately and the size of each set of buffers for a given user is the same (specified at the beginning of each request). When a buffer is full, LPA11 automatically switches buffers without any interaction with the user program.

Multirequest Mode Operations

Sampling from all device types is supported in multirequest mode. Up to eight users can be active concurrently. Each user's sampling rate is a user-specified multiple of the common real-time clock rate. Thus, independent rates can be maintained for each user. Each request specifies the device type so that, A-to-D, D-to-A or digital I/O can be synchronously sampled; the transition of a bit in a digital word can synchronize the sampling with a user event.

Digital I/O sampling can also be synchronized using hardware control lines (external data ready, external data accepted, internal data ready, etc.). This capability allows 16-bit parallel data to be transferred at a rate determined by an external device.

Each user sampling analog or digital channels can request that the data be time-stamped with a value from an internal clock. This allows an application program to mark the time when each sample was taken. There is also a mode that provides the capability to mark each sample with a one-bit flag indicating whether a user-specified external event has occurred. This allows a user to examine data at positive or negative time in relation to this event. In multirequest mode, the throughput of data is determined by the number and types of requests. The aggregate throughput rate for all users is typically 15,000 samples per second.

Dedicated Mode Operation

In dedicated mode, one user at a time can sample from analog-to-digital converters, or output to a digital-to-analog converter. Two analog to digital converters can be controlled simultaneously. Sampling is initiated by an overflow of the real-time clock, or by an external signal. Two sampling algorithms are implemented. One, at each overflow, samples both analog to digital converters in parallel, allowing two channels to be sampled simultaneously. The maximum single channel rate is 75,000 samples per second for one ADC or twice 75,000 samples for two ADCs (150,000 aggregate). The maximum multiple channel rate is 40,000 samples per second per channel per A to D (80,000 aggregate).
LPAl-K

The other algorithm samples the two analog to digital converters on an interleaved basis, beginning with the first whose sampling begins on alternate clock overflows.

Alternately, in Dedicated Mode, one four channel digital-to-analog converter can be controlled. Sampling is initiated under microcode control by an overflow of the real time clock. The maximum rate is 150,000 samples per second, divided by the number of channels in use.

FORTRAN interface subroutines for accessing the LPAl-K.

Table 8-1 FORTRAN Subroutines for the LPAl-K under RSX11-M V3.1

<table>
<thead>
<tr>
<th>Subroutine</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADSWP</td>
<td>Initiate synchronous A/D sweep</td>
</tr>
<tr>
<td>CLOCKA</td>
<td>Set Clock A rate</td>
</tr>
<tr>
<td>CLOCKB</td>
<td>Control Clock B</td>
</tr>
<tr>
<td>CVADF</td>
<td>Convert A/D input to floating point</td>
</tr>
<tr>
<td>DASWP</td>
<td>Initiate synchronous D/A sweep</td>
</tr>
<tr>
<td>DISWP</td>
<td>Initiate synchronous digital input sweep</td>
</tr>
<tr>
<td>DOSWP</td>
<td>Initiate synchronous digital output sweep</td>
</tr>
<tr>
<td>FLT16</td>
<td>Convert unsigned integer to a real constant</td>
</tr>
<tr>
<td>IBFSTS</td>
<td>Get buffer status</td>
</tr>
<tr>
<td>IGBTBUF</td>
<td>Return buffer number</td>
</tr>
<tr>
<td>INXTBF</td>
<td>Set next buffer</td>
</tr>
<tr>
<td>IWTBUF</td>
<td>Wait for buffer</td>
</tr>
<tr>
<td>LAMSKS</td>
<td>Set masks buffer</td>
</tr>
<tr>
<td>RLSBUF</td>
<td>Release data buffer</td>
</tr>
<tr>
<td>RMVBUF</td>
<td>Remove buffer from device queue</td>
</tr>
<tr>
<td>SETADC</td>
<td>Set channel information</td>
</tr>
<tr>
<td>SETIBF</td>
<td>Set array for buffered sweep</td>
</tr>
<tr>
<td>STPSWP</td>
<td>Stop sweet</td>
</tr>
<tr>
<td>XRATE</td>
<td>Compute clock rate and preset</td>
</tr>
</tbody>
</table>

SPECIFICATIONS

PREREQUISITE UNIBUS PDP-11 with Hex mounting space, and a KW11-K real time clock dedicated for use on the LPAl-K I/O bus.
### LPA11-K

**BACKPLANE**  
Space Required: UNIBUS: Hex  
LPA Bus: Hex + Quad

**POWER REQUIREMENTS**  
- UNIBUS + 5V: 5A  
- LPA Bus + 5V: 8A  
- LPA Bus - 15V: 1A  
- UNIBUS LOAD: 1

**DEVICES SUPPORTED**  
- **Dedicated Mode**  
  Either KW11-K, (2) AD11-K, (2) AM11-K  
  or KW11-K, AA11-K  
  or AR11  
  or LPS11-S, LPSKW, LPSAD-12, BA408, LPSAM, LPSAM-SG, LPS11-E, LPSAM-E

- **Multirequest Mode**  
  Either KW11-K, (2) AD11-K, (2) AM11-K, AA11-K, (5) DR11-K  
  or AR11, (5) DR11-K  
  or LPS11-S, LPSKW, LPSAD-12, BA408, LPSAM, LPSAM-SG, LPS11-E, LPSAM-E, LPSDR-A, LPSVC, (4) DR11-K

**ENVIRONMENT**  
- **Temperature**: 10° C (50° F) to 40° C (104° F)  
- **Rel. Humidity**: 10% to 90% Non-Condensing

<table>
<thead>
<tr>
<th>Operating Modes</th>
<th>Dedicated Mode</th>
<th>Multirequest Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer control</td>
<td>Microprocessor-controlled NPR (direct memory access)</td>
<td>Microprocessor-controlled NPR (direct memory access)</td>
</tr>
<tr>
<td>Number of independent user-operations (requests)</td>
<td>1 request</td>
<td>8 requests</td>
</tr>
<tr>
<td>Aggregate throughput to memory</td>
<td>100 kHz single channel</td>
<td>15 kHz</td>
</tr>
<tr>
<td></td>
<td>2 x 75 kHz two ADCs</td>
<td></td>
</tr>
</tbody>
</table>
## LPA11-K

<table>
<thead>
<tr>
<th>Operating Modes</th>
<th>Dedicated Mode</th>
<th>Multirequest Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operations</td>
<td>High speed A/D conversions or D/A conversions</td>
<td>Simultaneous A/D conversions D/A conversions Digital I/O Time stamping Event marking DIGITAL trigger</td>
</tr>
<tr>
<td>Rate selection</td>
<td>Single-rate triggered by programmable clock or external user clock</td>
<td>Individual rates per request (max 8) as sub-multiples of real time clock rate</td>
</tr>
</tbody>
</table>

**Dedicated Mode A to D Sampling Aggregate Throughput Rates**

### **AD11-K**

<table>
<thead>
<tr>
<th></th>
<th>AD11-K</th>
<th>AM11</th>
<th>AR11</th>
<th>LPS11</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINGLE ADC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single</td>
<td>75</td>
<td>75</td>
<td>35</td>
<td>75</td>
</tr>
<tr>
<td>Sequential</td>
<td>40</td>
<td>23</td>
<td>30</td>
<td>40</td>
</tr>
<tr>
<td>Random</td>
<td>40</td>
<td>23</td>
<td>30</td>
<td>40</td>
</tr>
<tr>
<td>DUAL ADC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SERIAL MODE</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single</td>
<td>100**</td>
<td>100**</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Sequential</td>
<td>80</td>
<td>46</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Random</td>
<td>70</td>
<td>46</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>DUAL ADC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PARALLEL MODE</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single</td>
<td>2 x 75</td>
<td>2 x 75</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>(TWO channels sampled in parallel)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sequential</td>
<td>2 x 40</td>
<td>2 x 23</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Random</td>
<td>2 x 40</td>
<td>2 x 23</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

* Throughput rates in thousands of samples per second
** Obtained by wiring user signal to same channel on both A to Ds

NA—Not Supported

### REGISTERS
LPA11-K programming is handled through four UNIBUS control and status registers and through two interrupt vectors.
Control In Status Register

Bit: 15  Name: RUN
Function: Start LPA11-K master microprocessor

Bit: 14  Name: RESET
Function: Initialize LPA11-K subsystem including all I/O devices

Bit: 13  Name: Not Used

Bit: 12  Name: Not Used

Bit: 11  Name: ENABL
Function: Enable the LPA11-K inter-microprocessor buffer to control the data acquisition I/O bus.

Bit: 10  Name: Not Used.

Bit: 9   Name: Not Used.

Bit: 8   Name: Not Used.

Bit: 7   Name: Ready In
Function: The LPA11-K is ready to accept a new command from the PDP-11 host

Bit: 6   Name: In Intr
Function: When set, allows the LPA11-K to interrupt through vector + 04 when it is ready to accept a new command from the PDP-11 host

Bit: 5   Name: Not Used

Bit: 4   Name: Not Used

Bit: 3   Name: BA17
Function: Used in conjunction with CSR word 4 to specify address of next command for LPA11-K in PDP-11 memory

Bit: 2   Name: BA16
Bit: 1   Name: Not Used
Bit: 0   Name: Go
Function: Set by PDP-11 to indicate a new command address is ready for the LPA11-K to process

Control Out Status Register

Bit: 15  Name: ERROR
Function: An error condition has been detected by the LPA11-K
Bit: 14  Name: STAT 06
Function: a code identifying what error status condition is pending
Bit: 13  Name: STAT 05
Function: a code identifying what error status condition is pending
Bit: 12  Name: STAT 04
Function: a code identifying what error status condition is pending
Bit: 11  Name: STAT 03
Function: a code identifying what error status condition is pending
Bit: 10  Name: STAT 02
Function: a code identifying what error status condition is pending
Bit: 9   Name: STAT 01
Function: a code identifying what error status condition is pending
LPA11-K

Bit: 8  Name: STAT 00
Function: a code identifying what error status condition is pending

Bit: 7  Name: Ready Out
Function: The LPA11-K has status information or an error to report to the PDP-11 host

Bit: 6  Name: Out Intr
Function: When set, allows the LPA11-K to interrupt through vector + 00 when it has status information or an error to report

Bit: 5  Name: Not Used
Bit: 4  Name: Not Used
Bit: 3  Name: Not Used
Bit: 2  Name: UID 02
Function: a 3-bit code provided by the LPA11-K to identify which of the eight potential active users the error or status condition applies

Bit: 1  Name: UIT 01
Function: a 3-bit code provided by the LPA11-K to identify which of the eight potential active users the error or status condition applies

Bit: 0  Name: UID 00
Function: a 3-bit code provided by the LPA11-K to identify which of the eight potential active users the error or status condition applies

Command Address Register

The low order 16-bits of the bus address is used to specify the address of the next command for the LPA11-K in PDP-11 memory.
CHAPTER 9
SYSTEM OPTIONS

BA11/L, K, P, F

The BA11 series of general purpose expansion mounting boxes fits into a frame designed to provide a strong enclosure, with maximum accessibility. The BA-11 expansion systems can contain all memory, peripheral controllers, devices, or options that are compatible with the PDP-11 family. Modular in design, they assure a high degree of serviceability, with minimum down time.

<table>
<thead>
<tr>
<th>EXPANSION BOX</th>
<th>PROCESSOR</th>
<th>SYSTEM UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BA11-L</td>
<td>PDP-11/04,</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>PDP-11/34</td>
<td></td>
</tr>
<tr>
<td>BA11-K</td>
<td>PDP-11/04,</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>PDP-11/34</td>
<td></td>
</tr>
<tr>
<td>BA11-P</td>
<td>PDP-11/60</td>
<td>6</td>
</tr>
<tr>
<td>BA11-F</td>
<td>PDP-11/70</td>
<td>9</td>
</tr>
</tbody>
</table>

SPECIFICATIONS

BA11-L Physical Specifications

Parameter

Chassis size
(with expansion console)

Specifications

13.5 cm H × 48 cm W × 64 cm D (5 1/4 in. H × 19 in. W × 25 in. D)
SYSTEM OPTIONS

**BA11/L, K, P, F**

Chassis weight (without logic modules)
H777 power supply size

**Slide extension**
Slideweight capacity (BA11-L fully extended)
Mounting capacity

Fan air movement direction
Shock and vibration characters
  - Operating
  - Nonoperating

**Temperature**
  - Operating
  - Nonoperating

Humidity

**BA11-K Physical Specifications**

**Parameter**
Chassis size (with H765 power system and pop panel)
Chassis size (with H765 power system without console panel and bezel)
Chassis size (without H765 power system, console panel and bezel)
BA11-K expander box chassis weight (without system units)
H765 power system size

Slide extension (three-section slide)
Slide weight capacity (BA11-K fully extended)
Three-stop slide

20 kg (45 lb)

12.7 cm H × 15.3 cm W × 50.8 cm D
(5 in. H × 6 in. W × 20 in. D)
57.15 cm (22.5 in)
18.14 kg (40 lb)

1 double system unit backplane or 2 single system unit backplanes

Front to back

10G for 10 ms—\(1/2\) sine pulse
40G for 30 ms—\(1/2\) sine pulse

0° to 50°C (32° to 120°F)
-55° to 85°C (−67° to 185°F)
0 to 90% (no condensation)

**Specification**
10.44 in. high, 17.12 in. wide,
26.53 in. deep
10.44 in. high, 17.12 in. wide,
25 in. deep

10.44 in. high, 17.12 in. wide,
17.25 in. deep
87 lb

10.38 in. high, 17.12 in. wide,
7.25 in. deep
27 in. maximum
150 lb

Positions: Horizontal, 45 degrees, and 90 degrees (front panel facing up)
SYSTEM OPTIONS

BA11/L K, P, F

Fan air movement direction
Horizontally toward rear of BA11-K

Module slots
22 maximum (2 double system units and 1 single system unit) using DEC standard configuration backplanes

Operating temperature range at inlet to box
41°F — 122°F (5°C — 50°C)

Operating humidity
10% to 95%
(no condensation)

Cooling efficiency for both fans at 90 Vac, 50 Hz
Temperature rise no greater than 18°F (10°C) from inlet air temperature to exhaust air

BA11-P Physical Specifications

Parameter

Specification

Chassis size
24½ in. H (62.23 cm) x 12 in. D (30.78 cm) x 15¾ in. W (40 cm)

Weight of unit (pivoting type)
75 lb (33.75 kg)

Fan
self contained, top to bottom see graph for range

Temperature
0° to 50°C (32° to 122°F)
—55° to 85°C (—67° to 185°F)

Humidity
0% to 90%
(no condensation)

Table 9-1 T Rise C on System of 300 CFM at 6-in. Ps

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Volts</th>
<th>T Rise C</th>
</tr>
</thead>
<tbody>
<tr>
<td>60 Hz</td>
<td>132</td>
<td>55</td>
</tr>
<tr>
<td>60 Hz</td>
<td>115</td>
<td>50</td>
</tr>
<tr>
<td>60 Hz</td>
<td>90</td>
<td>43</td>
</tr>
<tr>
<td>50 Hz</td>
<td>132</td>
<td>67.5</td>
</tr>
<tr>
<td>50 Hz</td>
<td>115</td>
<td>42.5</td>
</tr>
<tr>
<td>50 Hz</td>
<td>90</td>
<td>30.7</td>
</tr>
</tbody>
</table>

Blower should not be operated in an ambient exceeding 60°C at sea level. For altitudes up to 8,000 ft., ambient temperature should be lowered 1°C for each 1,000 meters.

It is recommended to keep the motor ambient temperature below 50°C for motors operating on frequency of 50 Hz.

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Figure 9-1  Output Characteristics of Blower Unit at 115 Volts

**BA11-F Physical Specifications**

- **Parameter**
  - Chassis size: 21 in. H × 19 in. W (48 cm) × 25 in. D (64 cm)
  - Chassis weight: 130 lb (58.8 kg)
  - Power supply: 2 H7420s
  - Slide extension: 27 in. (43.18 cm)
  - Slideweighting capacity: 250 lb (112.5 kg)
  - Fan air movement direction: top to bottom
  - Shock and vibration characteristics
    - Operating: 10 G for 10 ms—½ sine pulse
    - 40 G for 30 ms—½ sine pulse.

- **Temperature**
  - Operating: 0° to 50°C (32° to 122°F)
  - Nonoperating: −55° to 85°C (−67° to 185°F)

- **Humidity**
  - 0% to 90% (no condensation)
DESCRIPTION
The BB11 Blank Mounting Panel is a prewired System Unit (SU) designed for general interfacing. It is prewired for the UNIBUS and for power. The unit contains three 288-pin blocks assembled end-to-end in a casing which can be mounted in the various PDP-11 assembly units. Bus and power connectors, described here, use only 6 of the module slots, leaving 18 slots available for customer use.

The BB11 is wired to accept the UNIBUS in slots A1 and B1. This connection can be made with an M920 UNIBUS Connector or a BC11A UNIBUS Cable Assembly. All bus signals, including grant signals, are wired directly to corresponding pins in slots A4 and B4. From this point, the UNIBUS can be continued to the next unit by using a M920 or BC11A. If the BB11 is the last unit on the bus, slot A4-B4 accepts the M930 Bus Terminator Module. Standard bus pin names are listed in Appendix B.

The bus grant signals are wired through the BB11. These grant signal wires must be removed and replaced with wires to and from the user’s control circuits for the grant levels used by the customer-supplied device.

Slot A3 accepts the G772 Power Connector (furnished as part of the BA11 Mounting Box). Power for +5V is distributed to all A2 pins; −15V is distributed to all B2 pins except in slots A1, B1, A4 and B4; and ground is maintained through the frame and power connector on pins C2 and T1 of all slots.

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>UNIBUS CONN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>POWER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>RESERVED</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>UNIBUS CONN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

BB11 Module Layout
The DA11-B Interprocessor Link is a means for half-duplex, parallel, DMA (Direct Memory Access) data transfer between two PDP-11 computers.

The DA11-B option consists of two identical sections; each comprises one system unit which mounts in a BA11 Mounting Box associated with each PDP-11 computer.

![Diagram of DA11-B Interprocessor Link]

Figure 9-1  System Block Design

REGISTERS
Four registers are associated with each processor used with the DA11-B option. These registers are assigned bus addresses and can be read or loaded (with the exceptions noted) using any instruction that refers to the assigned address.

Signal INIT is the signal produced by power up, power down, the RESET instruction, or the START switch on the console; R/W specifies read/write.

Status and Command Register 772414
The DRST register is used for issuing commands and providing status for both the control and the companion computer.
**SYSTEM OPTIONS**

**DA11-B, DA11-BJ**

---

**Bit: 15**  
**Name:** Error  
**Function:** Specifies an error condition when: the DR11-B has attempted to address non-existent memory (also indicated by NEX bit 14); or when the companion computer has asserted ATTN (bit 13) because of either an input interrupt request or an initialize pulse (refer to the description of bit 13); or when the test module is not inserted in slot AB02 or CD04 of the DR11-B; or when the bus address register DRBA has overflowed by incrementing from all 1’s to all 0’s.

Error sets Ready (bit 7) and causes an interrupt if Interrupt Enable (bit 6) is set.

The Error bit is cleared by removing the condition(s) that caused it to be set: NEX is cleared by loading bit 14 with a zero; ATTN is cleared automatically by the companion computer; insert the test module in slots AB02 for normal operation or slots DC04 for diagnostic tests; reload the bus address register DRBA. Read-only.

**Bit: 14**  
**Name:** Non-Existent Memory  
**Function:** The non-existent memory condition specifies that, as UNIBUS master, the DA11-B did not receive a SSYN response within 20 μs following assertion of MSYN. NEX sets Error (bit 15), Ready (bit 7), and causes an interrupt request if IE (bit 6) has been set. This bit is cleared by INIT or by loading a zero; it cannot be loaded with a one. Read/write.

**Bit: 13**  
**Name:** Attention
**FUNCTIONS**

**Function:** Reads the state of the ATTN signal from the companion computer. When the companion computer is requesting an interprocessor interrupt, the 500 ns ATTN pulse is generated by the companion's Interrupt Request (bit 11). An ATTN pulse is also generated whenever INIT is asserted on the companion computer's bus. If caused by INIT, the ATTN pulse may be as long as 20 ms. Because the ATTN signal is a pulse, it should be ignored by the interprocessor programs.

ATTN sets ERROR and is set and cleared automatically by the DA11-B link. Read-only.

**Bit: 12**  
**Name:** Maintenance  
**Function:** Used exclusively with diagnostic programs and is cleared by INIT. Read/write.

**Bit: 11**  
**Name:** Input Interrupt Request  
**Function:** Status bit which reads the status of the Output Interrupt Request bit of the companion computer. When set, the bit specifies that an interprocessor interrupt has been requested by the companion computer.

Setting this bit also sets READY (bit 7) and causes an interrupt request if IE (bit 6) has been set. Read-only.

**Bit: 10**  
**Name:** Input Direct  
**Function:** Reads the status of the Output Direct bit of the companion computer. The transfer direction is specified as follows:

<table>
<thead>
<tr>
<th>Input Direct</th>
<th>Companion Computer Is:</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Transmitter</td>
</tr>
<tr>
<td>1</td>
<td>Receiver</td>
</tr>
</tbody>
</table>

**Bit: 9**  
**Name:** Input Mode  
**Function:** Status bit for reading the status of the Output Mode bit of the companion computer. This bit specifies the mode in which the interprocessor link is to be used as follows: Input Mode Block0- Mode, Input Model-Word Mode. Read-only.

**Bit: 8**  
**Name:** Cycle  
**Function:** This bit primes bus cycles. If it is set when GO is issued, an immediate bus cycle occurs. It is cleared at the beginning of the bus cycle and by INIT. CYCLE is also set whenever the companion computer requests a bus cycle via Cycle Request A or B and is cleared when the cycle begins. Read/write.
SYSTEM OPTIONS

DA11-B, DA11-BJ

Bit: 7  Name: Ready
Function: Specifies that the DR11-B is ready to accept a new command. When set, Ready forces the DR11-B to release control of the UNIBUS and inhibits further DMA cycles. This bit is set by INIT, Error (bit 15), or Word Count'Overflow and is cleared by Go (bit 0). Note that Ready must be cleared prior to initiating the block transfer. When set, Ready causes an interrupt request if IE (bit 6) has been set. Read only.

Bit: 6  Name: Interrupt Enable
Function: Enables an interrupt to occur when either Error or Ready is asserted, or when Input Interrupt Request is posted from the companion computer. This bit is cleared by INIT. Read/write.

Bit: 5, 4  Name: XBA17, XBA16
Function: These two Read/write extended bus address bits (17 and 16) are used with DRBA to specify a 17-1 in direct memory transfers. XBA17 and XBA16 do not increment when DRBA overflows; instead, Error is set. Read/write.

Bit: 3  Name: Output Interrupt Request
Function: Used to send an interrupt request to the companion computer. When set, this bit sets Input Interrupt Request and Ready in the companion computer and causes an interrupt request in the other computer if its Interrupt Enable has been set. This bit is cleared by INIT. Read/write.

Bit: 2  Name: Output Direct
Function: Specifies to the companion computer that the initiating computer is requesting to transmit (0) to receive (1). During the subsequent block transfer, this bit must be in the opposite state to Input Direct (bit 10). This bit is cleared by INIT. Read/write.

Bit: 1  Name: Output Mode
Function: Specifies to the companion computer (through Input Mode) that either a word or block transfer is taking place. A 0 specifies a block transfer and a 1 a word transfer. Output Mode is not used in any way by the DA11-B control logic but is simply displayed in the companion computer. It may be used by the interprocessor programs to keep track of the progress of the
cross-communications dialog that proceeds a block transfer and also to note that a block transfer is in progress. This bit is cleared by INIT. Read/write.

Bit: 0  Name: Go

Function: Causes a pulse to initiate the first DMA cycle in the block transfer. When set in conjunction with Cycle (bit 8), this bit causes the first cycle to occur in this computer if this DR11-B is the transmitter. When set alone, it causes the first cycle to occur in the companion computer if that DR11-B is the transmitter. Note that both Direction bits should be set properly before issuing the Go command.

This bit always reads as a zero. When set, this bit clears Ready (bit 7). Write only.

**Word Count Register**

The Word Count register is a read/write register. It is initially loaded with the 2's complement of the number of transfers to be made and increments toward zero after each bus cycle. When the overflow occurs (all 1's to all 0's), the Ready bit of DRST sets and bus cycles cease. DRWC is cleared by INIT. DRWC is a word register; use word instructions when loading this register.

**Bus Address Register**

The Bus Address register is a 15-bit read/write register. Bit 0, corresponding to address line A00, is set permanently to 0. With XBA16 and 17 in DRST, DRBA specifies BUS A 17-1 in direct bus access. The register is incremented by two following each bus cycle, advancing the address to the next sequential word location on the bus. If DRBA corresponding to A 15-1 overflows (all 1's to all 0's) the Error bit in DRST sets. This error condition (BA0F) is cleared by loading DRBA or by INIT. DRBA is a word register; use word instructions when loading this register.

The DRBA is cleared by INIT. Overflow does not increment the extended address bits XBA16 and 17; therefore, the maximum block that can be transferred is 32K words.

**Data Buffer Register**

The Data Buffer register is a 16-bit word register that can be loaded under program control and is used to buffer information when transferring data from one computer to the other. The output lines of this register are buffered; the inputs are not. These lines, therefore, must be held until the data are transferred to the memory of the receiving computer.
The data buffer register performs two separate functions in the interprocessor channel. In word mode, it is used as a 16-bit addressable register to transfer information between computers under program control. In block mode, it serves as a temporary storage register that holds the word being transferred under NPR control.

**Word Mode**—During program controlled transfers, the data buffer register is write/only register for data transmitted to the companion computer and a read/only register for data received. Because only a single flip-flop register exists for each direction, data must be maintained in DRDB until read by the companion computer. The cross interrupt facility in DRST should be used in conjunction with DRDB to pass parameters between computers as illustrated in the following example (assume Processor A is sending a file header to Processor B):

**Processor Processor A**

Load DRDB with the first word

Set: OUTPUT INTR REQ DRST3

OUTPUT Mode DRST 1

- Interrupt B
- Enter Interrupt Service Routine
- Read DRST
- Read DRDB
- Set OUTPUT INTR REQ DRST 3
- (Message Received)

**Processor Processor B**

(New Message)

Enter Interrupt Service Routine

Load DRDB with second word

Clear, the set OUTPUT INTR REQ DRST 3

Interrupt B
- repeat

repeat
SYSTEM OPTIONS

DA11-B, DA11-BJ

Block Mode—During block transfers under NPR control, the data buffer register temporarily stores the word read by the transmitter until it is written into memory by the receiver. Because this sequence of operations is transparent to the program. The data buffer register must not be used for word mode transfers until the block transfer has completed. If the data buffer register is loaded by the program during a block transfer, incorrect data may be transmitted between computers. This register is cleared by INIT. This is a word register; use word instructions when loading this register.

REGISTER ADDRESS ASSIGNMENT
Register address assignments for the DA11-B are the same as for the DR11-B option. Whenever both standard DR11-Bs and DA11-Bs exist in a given system, the DR11-Bs should be assigned first. Four register address complements are reserved. Additional DR11-Bs and/or DA11-Bs may be installed with addresses assigned in the user address Space.

DR11-B/DADR11-B Register Address Assignments

<table>
<thead>
<tr>
<th>Register</th>
<th>Unit 1</th>
<th>Unit 2</th>
<th>Unit 3</th>
<th>Unit 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRW</td>
<td>772410</td>
<td>772430</td>
<td>772450</td>
<td>772470</td>
</tr>
<tr>
<td>DRBA</td>
<td>772412</td>
<td>772432</td>
<td>772452</td>
<td>772472</td>
</tr>
<tr>
<td>DRST</td>
<td>772414</td>
<td>772434</td>
<td>772454</td>
<td>772474</td>
</tr>
<tr>
<td>DRD8</td>
<td>772416</td>
<td>772436</td>
<td>772456</td>
<td>772476</td>
</tr>
</tbody>
</table>

VECTOR ADDRESS ASSIGNMENTS
Vector address assignments for the DA11-B are the same as for the DR11-B option. Whenever both standard DR11-Bs and DA11-Bs exist in a given system, the DR11-Bs should be assigned first. The first unit is assigned vector address $124_8$. Subsequent units are user assigned in the floating vector address pace beginning at $300_8$. The DA11-B requires only one vector; however, it must be of the form $XX4_8$.

SPECIFICATIONS
Mechanical:
Units: Two
Logic Panels/Units: One system unit
Dimensions/Unit: 16 in. h, 2⅛ in. w, 10 in. d
Mounting Prerequisite: BA11-Mounting Box space

Electrical:
Input Power: 120/240 Vac ± 10%, 47-63 Hz

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SYSTEM OPTIONS

DA11-B, DA11-BJ

Current (at 5V) 4.3 A
Power Dissipation 25 W
Heat Dissipation 82 Btu/hr.
Module Type M-Series
Logic Levels TTL

Operational:

Data Transfers
Word Size 16-bits
Method Direct Memory Access (DMA or NPR)
or word transfer

Modes of Operation
Size Word or Block
Direction Send or Receive

Hardware Prerequisites Two 4K PDP-11 computers with multi
level priority

UNIBUS
Bus Load One Unit load/each bus
Interrupt Vector Same as DR11-B (124 for first unit)
Register Address Same as DR11-B (772410 for first unit)
BR Level Same as DR11-B (BR5 hardwired)

Unit Separation
Distance
25 foot cables Model DA11-BD (Standard)
50-foot cables Model DA11-BE (Optional)

DA11-BJ

DESCRIPTION
The DA11-BJ is a UNIBUS link (DA11-B) designed with differential
drivers and receivers that allow high reliability communication
over long distances between two PDP-11s.

REGISTERS
Each DA11-BJ section consists of four registers: command and
status, word count, bus address and data. Data transfer is initial-
ized under program control and proceeds via DMA until the entire
data block has been transferred. A transfer sequence is:

- The sending PDP-11 loads its bus address and word count reg-
isters.
- The sending PDP-11 then loads the command and status reg-
ister and causes an interrupt in the receiving PDP-11.

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**SYSTEM OPTIONS**

**DA11-B, DA11-BJ**

- The receiving PDP-11 responds to the interrupt and loads its bus address, word count and command and status registers to initiate the transfer.
- Transfers continue until completion, at which time both PDP-11s receive an interrupt.

The DA11-BJ is programmed in the same way as the DA11-B.

**DA11-BJ SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Mechanical</th>
<th>One system unit on each UNIBUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cable Connector Used</td>
<td>40-pin Berg</td>
</tr>
<tr>
<td>Register Address</td>
<td>Same as DA11-B, 772410 for first unit</td>
</tr>
<tr>
<td>Vector Address</td>
<td>Same as DA11-B, 124 for first unit</td>
</tr>
<tr>
<td>Transfer Modes</td>
<td>Interrupt Control and DMA</td>
</tr>
<tr>
<td>BR Level</td>
<td>5</td>
</tr>
<tr>
<td>CSS</td>
<td></td>
</tr>
</tbody>
</table>
DR70

A general purpose user interface to the Massbus, the DR70 is normally used with an RH70 Massbus Controller to create a high speed interface to the main memory of a PDP-11/70 computer. However, the DR70 may be used with any processor that has a Massbus controller. Figure 9-2 shows the DR70 in a typical system application.

The DR70 allows a user device to perform block data transfers to or from memory via the Massbus and appropriate Massbus controller. The maximum transfer rate of the DR70 is typically limited only by memory and/or system band width considerations. The transfer rate is determined by the user device.

![System Block Diagram](image)

**Figure 9-2 System Block Diagram**

**PROGRAMMING**

Five programming registers are located in the DR70 and a number of other registers are contained in the Massbus controller. The format of the registers changes slightly with each type of controller. The RH70 is used in conjunction with the PDP 11/70 and the RH11 is implemented with all other PDP-11 processors.

**SPECIFICATIONS**

**Mechanical:**
- Logic Mounting: One System Unit
SYSTEM OPTIONS

DR70

Dimensions       8½ in. h, 16⅜ in. w, 2⅓ in. d.
Weight           15 lbs.
Prerequisites     Mounting space for one system unit (DR70) with each user device and adequate source of DC power.

Electrical:
Input Power      +5 Vdc, @ 5A. −15Vdc @ 500 MA
Logic Levels     TTL
Module Type      M-Series

Operational:
Transfer Rate    4.0 Megabytes/second (max.)
Output Levels    TTL (30 ft. max. length from user device to DR70)

CSS
The DT07 family of UNIBUS switches allows one or a group of UNIBUS peripheral devices to be switched between two, three or four PDP-11 processors.

FEATURES
- multi processor configurations for resource sharing and high availability through redundancy
- two, three and four port switches
- solid-state switching, manual or programmable initiation
- failure isolation
  (Failures on one bus are isolated from other buses.)
- fail-over operation
  built-in watch-dog timer for automatic fail-over
- modular and flexible
  can accommodate a variety of system configurations
- software support
  device driver optionally available

DESCRIPTION
As well as allowing a single or a group of UNIBUS peripheral devices to be switched between two, three and four PDP-11 processors, DT07 switches also facilitate on-line system back-up and
dynamic reconfiguration for systems where very high availability or resource sharing is required.

The BAS11-K Switched Bus Foundation Box is used in conjunction with the DT07. It provides space for the switched UNIBUS and its peripherals. The DT07 can operate under either program control or manual control through user-accessible switches on the BAS11-K panel.

The DT07 UNIBUS switch implements a switched or shared bus that can be connected selectively to the UNIBUS of any processor in a multi processor system. Any device or devices except a processor may be connected to this shared bus. When the switch is connected to a particular processor's UNIBUS, all peripherals and memory on the shared bus operate essentially as if they are permanently connected to that bus. When the switch is disconnected, all peripheral devices on the shared bus are removed from that UNIBUS and are available for connection to any other processor's UNIBUS.

The switch is engineered to preserve the transmission properties of all buses to which it is attached, regardless of the switch's position. Even during on-line switching, all buses are synchronized to prevent interfering with individual programs. The DT07 includes the functionality of a UNIBUS repeater in that the entire shared bus appears as a single load to each processor bus. The electronic switching circuits utilized in the DT07 not only eliminate impedance-mismatch and crosstalk problems, but also provide the long-term reliability inherent in solid-state circuits, and a high degree of isolation between buses.

In both manual and programmable modes, a bus synchronizer assures that the switch changes position without interfering with any operations on the processor bus; i.e., the switch can be thrown while a program is running. (During switchover, all peripherals on the switched bus must be idle.) If two or more processors request use of the shared bus simultaneously, a priority-arbitration circuit within the switch specifies which processor will be served first. The priority-arbitration circuit assures that no more than one processor is connected to the shared bus at any one time.

An important feature of the UNIBUS switch in high availability applications is the ability to disconnect from a processor that is no longer operational. This is facilitated by a watch-dog timer contained within the DT07. The timer is initiated by the backup processor not currently using the switch. If the connected processor
does not reset the timer within the allotted interval (thereby indicating that the processor has halted or is executing an invalid program), the switch automatically disconnects. Similarly, power failure in the system to which the shared bus is connected automatically disconnects the switch. A back-up processor can then assume control of the switch and proceed to operate devices on the shared UNIBUS.

In a multi-processor configuration with a DT07 UNIBUS switch, there is a port module plugged into each PDP-11's UNIBUS. These modules are interconnected to form the DT07 switch. The switched bus foundation box (BAS11-K), when connected to a DT07, forms the switched bus. If desired, a number of switched buses can be implemented for a given multi processor system by employing additional sets of DT07s and BAS11-Ks.

Each DT07 port module is designed to provide failure isolation between buses. The method of connection between the individual DT07 port modules permits complete shutdown of the switched bus and removal of cables from each DT07 port module with no effect on the continuous operation of the individual systems.

The prerequisite BAS11-K box forms the shared bus with appropriate termination slots for peripheral devices and a manual bus control panel. The BAS11-K has an expansion space for four additional systems units.

SOFTWARE (OPTIONAL)
The DT07 Device Driver, supported under RSX-11M, provides the user access to control the DT07 UNIBUS switch and all the devices connected to it.

The driver supports normal and device specific OIO functions. These functions provide control and sensing of activities occurring with the switch. An application task, written by the user in MACRO or FORTRAN, can control the switch by using these driver functions.

MODULARITY AND FLEXIBILITY
The basic two-processor switch (DT07-BA) is modularly expandable to switch a UNIBUS among three or four processors. In addition, two or more UNIBUS switches can be used on one processor. The BAS11-K mounted control panel provides system configuration control for switching up to four processors.
SYSTEM OPTIONS

SPECIFICATIONS
DT07-BA/CA/DA

Electrical:
Module Type: M Series. One Hex SPC module per CPU for each switched bus (adjacent slot can be used for short modules only).
Circuitry: Solid-state
UNIBUS Loading: 1 load/bus
Output Bus Drive: See Configuration Table
Input Current: 6 A (approx.) at +5Vdc (each port)

Operational:
Interrupt Vector: One: 170, 174, 270, 274 or from the floating vector field.
Priority Level: BR7
Latency (propagation delay): Bus cycles that go through the switch (i.e., between a switched and a non-switched peripheral) are extended by 300ns (typically).
Watch-Dog Timer: Interval preset to approximately 10ms

BAS11-KA/KB/KC/KD

Mechanical:
Weight: 90 lb (without any peripheral controllers)
Prerequisite 10½ in. H mounting space in a 19 in. H960 or H9500 Series cabinet.

Electrical:
Input Power: 115/230 Vac ±10%, 47-64Hz
Line Current: 12A/6A, single phase

CSS
FEATURES
• fast
• plugs into UNIBUS
• overlaps processor operations
• provides signed integer multiply and divide
• provides signed normalize and multiple shifts

DESCRIPTION
The PDP-11 EAE option executes high-speed arithmetic operations. This system performs signed integer multiply (16 bit × 16 bit), signed integer divide (32 bit/16bit), and signed normalize and multiple shifts either with sign extension or by filling with zeros.

Timing
The execution times for EAE operation are:
Multiply: 6.6 μsec
Divide: 7.4 μsec
Normalize: 0.5 to 6.6 μsec
Logical Shift: 0.5 to 6.6 μsec
Arithmetic Shift: 0.5 to 6.6 μsec

Since this unit is a bus peripheral, there is overlap between its operation and the fetch and address decoding of the instruction used to fetch the results from the bus. This overlap provides an approximate 1.2 microsecond increase in system operational speed over a comparable “wait for completion” type of system.

Programming Considerations
The PDP-11 EAE option is a fast signed integer arithmetic unit. All registers are read/write; therefore it can be used by reentrant programs. The EAE option is driven by addressing its registers according to their significance as defined in the attached table. For example, a multiply would be initiated by moving the multiplicand to 777 306.

Addressable Registers
The registers, their significance and their addresses are:

Register Name: DIVIDE
Bits 0-15 Address: 777 300
Significance: When the divisor is moved to this address, the 32 bit dividend in the AC MQ is divided by this number.
Register Name: AC (Accumulator)
Bits: 0-15  Address: 777 302
Significance: High order word of arithmetic unit. Contains high order product on multiply, remainder or high order dividend on divide.

Register Name: MQ (Multiplier Quotient)
Bits: 0-15  Address: 777 304
Significance: Low order word of arithmetic unit. Contains low order product or quotient on divide.

Register Name: MULTIPLY
Bits: 0-15  Address: 777 306
Significance: When the multiplicand is loaded into this address, the EAE begins the multiplication of this number by the number in the MQ.

Register Name: SC (Step Count)
Bits: 0-5  Address: 777 310
Significance: The step count contains the count for long shifts and the step count following normalize.

Register Name: SR (Status Register)
Bits: 0  Address: 777 311
Significance: On shifts, contains the last bit shifted out of MQ or AC.

Register Name: SR
Bits: 1  Address: 777 311
Significance: Indicates the result is single word and is in MQ.

Register Name: SR
Bits: 2  Address: 777 311
Significance: Indicates the result is zero.

Register Name: SR
Bits: 3  Address: 777 311
Significance: MQ is zero.

Register Name: SR
Bits: 4  Address: 777 311
Significance: AC is zero.

Register Name: SR
Bits: 5  Address: 777 311
Significance: AC is all ones.
**Register Name:** SR  
**Bits:** 6-7  
**Address:** 777 311  
**Significance:** These bits indicate sign and overflow conditions.

**Register Name:** NORMALIZE  
**Bits:**  
**Address:** 777 312  
**Significance:** Writing into this address results in the 32 bit number in the AC being normalized; reading this address fetches the shift count.

**Register Name:** LOGICAL SHIFT  
**Bits:** 0-5  
**Address:** 777 314  
**Significance:** Output to this address results in a logical shift of the AC and MQ (filling with zeros) the specified number of bits.

**Register Name:** ARITHMETIC SHIFT  
**Bits:** 0-5  
**Address:** 777 316  
**Significance:** Output to this address initiates an arithmetic shift of the AC and MQ (sign extension) with the shift count being the value moved to this address.
The PRS01 is a small, portable paper-tape reader that connects into the serial line of a system console or terminal.

**FEATURES**
- 20mA current loop compatible
- 300- or 2400-baud models
- operates with or without console device
- portable
- self-contained with own power supply

**DESCRIPTION**
The PRS01 portable paper-tape reader provides a convenient and inexpensive method of loading paper tapes by using the keyboard device codes of the terminal. It is designed primarily for loading maintenance and diagnostic programs. Because the reader produces a 20mA serial asynchronous signal, it can be interconnected to a console device or terminal, or to any 20mA current loop input, if no console device is available.

A switch on the reader permits selection of either the console keyboard or the PRS01 as the computer input device. This lets the user switch back and forth between devices without having to disconnect the reader once it is installed. Operation is continuous, with start and stop functions controlled by a front panel switch. Otherwise, the reader is similar in operation to the low-speed reader on an ASR teleprinter.

The PRS01 reads 8-level tapes with in-line feed hole. Two versions of the reader are available with transfer rates of 300 baud or 2400 baud.

The entire reader, including a self-contained power supply, is housed in a small 2-piece plastic case. The back cover is removable for easy access to all sub-assemblies which are mounted inside the front cover.

Four different models of the PRS01 are available:

- PRS01-AA 2400 baud, 115 VAC, 50/60 Hz
- PRS01-AB 2400 baud, 230 VAC, 50 Hz
- PRS01-BA 300 baud, 115 VAC, 50/60 Hz
- PRS01-BB 300 baud, 230 VAC, 50 Hz
A problem with many computer systems is the lack of a reliable but low-cost console terminal that also includes a paper-tape reader. Although many good quality terminals exist, their inability to read-in programs forces the user to consider costly alternatives. The PRS01 solves the problem of loading programs.

A different problem faces the user who has one or more dedicated computers, each designed to handle a specific operation. Although there is no need to re-program a dedicated computer, there is also no way of running diagnostic tests in the event of a malfunction, particularly if the computer has a turn-key console. The PRS01 solves this problem. It takes just a few minutes to plug the reader into the malfunctioning computer so that diagnostic programs can be loaded and run. In addition, the portability of the reader makes it easy for the user to disconnect it and plug it into any one of the other computers. Its light weight (6 1/2 pounds) and small size (12" by 7" by 5") make it ideal for carrying from site to site. Nothing else is needed because the PRS01 is self-contained and has its own power supply. The power cord and interface cable are an integral part of the assembly.

**SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Power</th>
<th>PRS01-AA</th>
<th>1.0 amp @ 117 VAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Requirements</td>
<td>-BA</td>
<td>(+–10%/), 50/60 Hz</td>
</tr>
<tr>
<td></td>
<td>PRS01-AB</td>
<td>0.5 amp @ 230 VAC</td>
</tr>
<tr>
<td></td>
<td>-BB</td>
<td>(+–10%/), 50 Hz</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>15°C to 32°C (59°F to 90°F)</td>
<td></td>
</tr>
<tr>
<td>Humidity</td>
<td>20% to 80% (non-condensing)</td>
<td></td>
</tr>
<tr>
<td>Dimensions</td>
<td>12&quot; wide by 7 1/2&quot; high by 5 1/4&quot; deep</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(30.4 cm wide x 19.0 cm high x 13.3 cm deep)</td>
<td></td>
</tr>
<tr>
<td>Weight</td>
<td>6 1/2 pounds (2.92 kg)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(approx. 8 pounds (3.6 kg) shipping weight)</td>
<td></td>
</tr>
<tr>
<td>Feed Hole</td>
<td>in-line</td>
<td></td>
</tr>
<tr>
<td>Tape Level</td>
<td>8-level</td>
<td></td>
</tr>
</tbody>
</table>
SYSTEM OPTIONS

PRS01

SPECIFICATIONS (Cont.)

Transmission Rates
PRS01-AA 2400 baud (approx. 120 char/sec)
-AB
PRS01-BA 300 baud (approx. 22 char/sec)
-BB

Interface
20mA current loop, passive with Mate-N-Lok connector (12-09378-01)

Data
Data is in the form of a serial pulse string. Each character time consists of one start bit, eight data bits, and one stop bit (see below). The stop bit (or 1) is current flowing.

Interface Cables

Standard (part of PRS01) “Y” cable, 10 feet long, male and female Mate-N-Lok connectors.

Optional BC05M-1F Female Mate-N-Lok to Berg
The RH01 MASSBUS Dual Port Adapter provides a means of dual porting single-ported MASSBUS peripherals.

**FEATURES**
- allows dual porting of single-ported MASSBUS peripherals
- expandable to eight drives per RH01
- enhances high availability in single or dual access configurations
- switching can be done manually through software programming

**DESCRIPTION**

The RH01 MASSBUS Dual Port Adapter permits sharing or switching MASSBUS peripherals between two computers for either resource sharing or for high availability redundant systems. Any PDP-11 processor with a MASSBUS controller can connect to the RH01. The RH01 may be used with MASSBUS devices. As many as eight devices can be shared on the common MASSBUS of the RH01. The RH01 is also designed to allow local drives to be used on the same MASSBUS controller. A local drive can be used by its processor without interfering with simultaneous operating of one of the shared drives by the other processor. The RH01 can be used with devices having transfer rates as high as 1 MHz and will not reduce the data throughput of the MASSBUS. A maximum of 200 ns latency will be added to all read or write operations out of the device control registers of the common MASSBUS.

Switching of the RH01 can be controlled either manually or through a software program. A 4 position switch on the front panel
allows the controller to be locked on either the A or B port, to be put in the program control mode, or to be switched to the OFF position to allow maintenance on any device. When an attempt is made by either port to read or write any of the device registers on the common MASSBUS, the RH01 will automatically switch from the unseized state to the requesting port. If the RH01 is not used or released for a certain period of time (1 to 4 min.) after it has been seized, it will automatically release itself for use by either port.

**SPECIFICATIONS**

**Mechanical**

- Mounting Box: BA11-L
- Dimensions: 5¼ in. (13.3 cm) h, 19 in. (48.2 cm) w, 24 in. (60.9 cm) d
- Weight: 65 lb (29.2 kg)
- Prerequisite: 5¼ in. (13.3 cm) h rack mounting space in a 19 in. (48.2 cm) cabinet
SYSTEM OPTIONS

RH01

Electrical:
Input Power
120/240 Vac ±10%, 47-63 Hz

Operational:
Bit Capacity
The RH01 may be used with 16- or 18-bit MASSBUS devices
Transfer Rates
1 mW (2 megabytes/second)

CSS
## APPENDIX A

### APPENDIX A CONTROL AND REGISTER
### ADDRESSES AND VECTOR ASSIGNMENTS

Control and Status Register Addresses

<table>
<thead>
<tr>
<th>Device</th>
<th>Address</th>
<th>Size</th>
<th>Number</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>AA11</td>
<td>776750</td>
<td>8</td>
<td>1</td>
<td>(first unit)</td>
</tr>
<tr>
<td>AA11</td>
<td>776400</td>
<td>8</td>
<td>4</td>
<td>(extra units)</td>
</tr>
<tr>
<td>AD01</td>
<td>776770</td>
<td>4</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>ADF11</td>
<td>770460</td>
<td>8</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>AFC11</td>
<td>772570</td>
<td>4</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>AR11</td>
<td>770400</td>
<td>8</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>BM792-YA</td>
<td>773000</td>
<td>32</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>BM792-YB</td>
<td>773100</td>
<td>32</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>BM792-YC</td>
<td>773200</td>
<td>32</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>BM792-YH</td>
<td>773300</td>
<td>32</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>BM873-YA</td>
<td>773000</td>
<td>128</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>BM873-YB</td>
<td>773000</td>
<td>256</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>BM873-YC</td>
<td>773000</td>
<td>256</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>CD11</td>
<td>777160</td>
<td>4</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>CM11</td>
<td>777160</td>
<td>4</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>CR11</td>
<td>777160</td>
<td>4</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>DC11</td>
<td>774000</td>
<td>4</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>DC14-D</td>
<td>777360</td>
<td>8</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>DL11-A</td>
<td>777560</td>
<td>4</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>DL11-A</td>
<td>776500</td>
<td>4</td>
<td>16</td>
<td>(console)</td>
</tr>
<tr>
<td>DL11-B</td>
<td>777560</td>
<td>4</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>DL11-B</td>
<td>776500</td>
<td>4</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>DL11-C</td>
<td>775610</td>
<td>4</td>
<td>31</td>
<td></td>
</tr>
<tr>
<td>DL11-D</td>
<td>775610</td>
<td>4</td>
<td>31</td>
<td></td>
</tr>
<tr>
<td>DL11-E</td>
<td>775610</td>
<td>4</td>
<td>31</td>
<td></td>
</tr>
<tr>
<td>DL11-W</td>
<td>777546</td>
<td>1</td>
<td>1</td>
<td>(line clock, first unit only)</td>
</tr>
<tr>
<td>DL11-W</td>
<td>777560</td>
<td>4</td>
<td>1</td>
<td>(console)</td>
</tr>
<tr>
<td>DL11-W</td>
<td>776500</td>
<td>4</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>DM11</td>
<td>775000</td>
<td>4</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>DM11-BB</td>
<td>770500</td>
<td>4</td>
<td>16</td>
<td>(modem control for DM11)</td>
</tr>
<tr>
<td>DN11-AA</td>
<td>775200</td>
<td>4</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>DN11-DA</td>
<td>775200</td>
<td>1</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>DP11</td>
<td>774400</td>
<td>4</td>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>
APPENDIX A

CSR Addresses

<table>
<thead>
<tr>
<th>Device</th>
<th>Address</th>
<th>Size</th>
<th>Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>DR11-A/C</td>
<td>772300</td>
<td>4</td>
<td>16</td>
</tr>
<tr>
<td>DR11-B (1)</td>
<td>772410</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>DR11-B (2)</td>
<td>772430</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>DR11-B (3)</td>
<td>772450</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>DR11-B (4)</td>
<td>772470</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>DS11</td>
<td>775400</td>
<td>67</td>
<td>1</td>
</tr>
<tr>
<td>DT11</td>
<td>774200</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td>DV11</td>
<td>775000</td>
<td>16</td>
<td>4</td>
</tr>
<tr>
<td>DX11</td>
<td>776200</td>
<td>16</td>
<td>2</td>
</tr>
<tr>
<td>FP11</td>
<td>772160</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>GT40</td>
<td>772000</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>ICR/ICS11</td>
<td>771000</td>
<td>256</td>
<td>1</td>
</tr>
<tr>
<td>IP11/IP300</td>
<td>771000</td>
<td>128</td>
<td>1</td>
</tr>
<tr>
<td>IP11</td>
<td>771776</td>
<td>128</td>
<td>1</td>
</tr>
<tr>
<td>KE11</td>
<td>777300</td>
<td>8</td>
<td>2</td>
</tr>
<tr>
<td>KG11</td>
<td>770700</td>
<td>4</td>
<td>8</td>
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426
## APPENDIX A

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(MASBUS Multiple)

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### Fixed Interrupt Vector Assignments

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### Fixed Interrupt Vector Assignments

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\(^1\) Not assigned to any device, RSTS/E uses this vector
### APPENDIX A

#### OPTION

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\(^2\) RSTS does not support the AA11, UCD11, and ICS/ICR11 which use these vectors required by RSTS

\(^3\) USER RESERVED vectors are used for additional printers

### Floating Interrupt Vector Devices

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## APPENDIX A

### Floating Interrupt Vector Devices

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## APPENDIX A
APPENDIX B

SUMMARY OF PERIPHERALS SPECIFICATIONS

The following table briefly summarizes the outstanding physical specifications of the listed peripherals. Some peripherals are older models that are supported, but no longer sold. They are noted by the X in the page column. Specifications are given in inches, pounds and degrees centigrade. These numbers should be considered only as quick referential guidelines. Complete detailed specifications for the devices are included in the text of the handbook. Some specifications are subject to site modification. If there are any questions, call your local DIGITAL sales office for specific information.
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