The SWII-X option consists of one multi-layered SMO module.

There are two tests for system checkout and acceptance
of the SWII-X option. The SWII-X diagnostic (H00000-12-9020-X)
and the SWII-X diagnostic module to the DEC-II system exerciser.
Since the AP-11 (12-bit A/D) option can run in conjunction with
the SWII-X, there are two procedures that follow, only one should
be used. Refer to the respective diagnostic for setup and
starting procedure.

I SWII-X (stand-alone or no AP-11-X)

Logic Test (starting address 200) of the SWII-X Diagnostic,
with SR = 000000, must run without any error printout for a
minimum of 15 minutes or 20 passes. An End Pass is printed at
the end of each pass of the diagnostic.

The DEC-II System Exerciser with the SWII-X diagnostic
module should run for a minimum of one hour.

II SWII-X AND AP-11-X

There are two jumpers (J010771) that are included with the
AP-11-X option. These jumpers are made up with fast-on terminators.
Both the AP-11-X module (2009) and the SWII-X module (H00205)
have two Fast-on connectors, indicated as tab 1 and tab 2. Tab 1 and
the AP-11-X Schmitt Trigger dual to the AP-11-X External Start
input and ties the SWII-X Clock A Overflow to the AP-11-X Clock
Overflow input.

The SWII-X Diagnostic has five special tests, each with its
own starting address. Each test requires certain pins on the
SWII-X I/O connector to be connected together. Each test should
run for a minimum of two minutes. The tests and jumpers are listed
below. Two short 300pF capacitors are needed to run these tests.

<table>
<thead>
<tr>
<th>TEST</th>
<th>STARTING</th>
<th>ADDRESS</th>
<th>JUMPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>F02 output &amp; 271</td>
<td>212</td>
<td>V to LS</td>
<td></td>
</tr>
<tr>
<td>272</td>
<td>254</td>
<td>VO to LS</td>
<td></td>
</tr>
<tr>
<td>273 &amp; 274 output</td>
<td>220</td>
<td>V to T and L to LL</td>
<td></td>
</tr>
<tr>
<td>A Event Out</td>
<td>224</td>
<td>Uw to LL</td>
<td></td>
</tr>
<tr>
<td>B Event Out</td>
<td>230</td>
<td>TT to LL</td>
<td></td>
</tr>
</tbody>
</table>
The N705 module is used in the N711-K option, a dual programmable real time clock. The N705 is a hex multi-layer module consisting of a unibus interface, a 16-bit programmable clock with mode and rate controls, an 8-bit programmable clock with rate control, and oscillators with dividers.

The circuits to be described are referenced to prints DGS-76428-2-1, which consist of 10 sheets. Each sheet has a name description and an alpha-numeric identification (01-010). All signals are source precoded with the alpha-numeric identification. For example, signal D1 LO STAT A will load A status register high byte is generated on sheet D1 which is titled Address Selection.

It is assumed that the reader is familiar with Unibus operation and is familiar with interpreting circuit schematics of logic and circuits so that detailed description is not necessary. The description given here is to familiarize the user with the N705 circuits enough to identify a portion needing attention. It is recommended that the user read the N711-K manual (EXD-76100-00-001).

There are two programmable clocks on the N711-K designated as Clock A and Clock B. The 16-bit clock is Clock A and the 8-bit clock is Clock B. Signal designation will contain the letters A or B to signify which clock is involved.

The Unibus interface consist of the device address decoding, interrupt logic and arbitration, and the Unibus signal receivers and drivers. On sheet D1 the bus address lines are received and gated with BUS MUX (master sync) to decode D1 DEVICE.
The count-down input is used to increment (2's compliment-decrement) the A Buffer data in Auto Increment Mode. Data to the A Buffer can be from the A Counter or the Buffered Data Bus. The A Buffer data is multiplied by 74153, two to one line multipliers.

The B Clock Counter, Preset Buffer and Status registers are located on sheet 06. The B Counter is made up of 74191 binary counters. The Overflow from the counter is used to reload the counter with the data in the B Buffer is from the buffered data bus.

A 20 MHz oscillator is used to generate timing pulses and various other frequencies that are a multiple of 20 MHz. The 20 MHz oscillator is located on the lower left of sheet 05, 740124. It is divided by 74190 BCD counters to 1 MHz, 100kHz, 10kHz, and 1kHz. These frequencies are decoded by a 74157 (multiplexer) to one frequency which is used to increment Clock A Counter.

Clock B frequency dividers and multiplexer are located on sheet 05.

The four Schmitt Triggers are located on sheet 05. Three of the Schmitt Triggers inputs have threshold control and slope control. The fourth Schmitt Trigger is used for line frequency (location 97). The outputs of Schmitt Triggers one, two and the line frequency are synchronized to the timing pulses produced on sheet 05. Refer to the timing chart in figure 1 for timing overlap one. The resistor/diode network on the output of INV 872 and 873, is for protection and converting the input to 0 to +9V. The LM399 (200) inputs cannot exceed +4V.

**FIGURE 1: TIMING DIAGRAM**