The KWII-X option consists of one multi-layer hex module. When the KWII-X option is installed, the KWII-X diagnostic module (EC2-0400-A) and the KWII-X diagnostic module to the DECK-II system exerciser. Since the KWII-X (12-bit A/D) option can run in conjunction with the KWII-X, there are two procedures that follow, only one should be used. Refer to the respective diagnostic for setup and starting procedure.

**KWII-X (Utilization of no KWII-X)**

- Units Test (setting address 255 of the KWII-X diagnostic, with 08 is system, must run without any error prints for a minimum of 15 minutes or 30 pages. The DCS-XXXX is printed at the end of such pass of the diagnostic.

The DCS-II system exerciser with the KWII-X diagnostic module should run for a minimum of one half hour.

**KWII-X and KWII-X**

There are two jumpers (J102774) that are included with the KWII-X option. These jumpers are made up with contact terminals. Both the A/D and B/D module and the MII module have two contact connectors, indicated as tab 1 and tab 2. Tab 1 and tab 2 should be jumpered to tab 1 and tab 2 respectively. This time the KWII-X shutdown (due to KWII-X External Start signal and KWII-X Clock) shut down the KWII-X clock (overflows, input).

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**Print set**

KWII-X 24
**DIGITAL EQUIPMENT CORPORATION**  
MAYNARD, MASSACHUSETTS

**ENGINEERING SPECIFICATION**  
DATE: 4-MAR-76

### M7025 CIRCUIT DESCRIPTION

#### REVISIONS

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### M7025 CIRCUIT DESCRIPTION

The M7025 module is used in the WM7-K option, a dual programmable real time clock. The M7025 is a 6×2 32-bit module consisting of a 16-bit programmable clock with mode and rate controls, an 8-bit programmable clock with rate control, and uncertainties with dividers.

The circuits to be described are referenced to the M7025-2, 2, 1, which consists of 10 sheets. Each sheet has a name description and an alphanumeric identification (name: D11). All signals are source driven with the alphanumeric identification. For example, M7025-2 10 is the D11 10 bit register high byte is generated on sheet 10 which is titled Address Selection.

It is assumed that the reader is familiar with Unibus operation and is familiar with interpreting circuit schematic symbols of logic and circuits so that detailed description is not necessary. The description given here is to familiarize the user with the M7025 circuits enough to identify a problem solving situation.

It is recommended that the user read the WM7-K manual (XEN-M7K-SP-001).

There are two programmable clocks on the WM7-K designated as Clock A and Clock B. The 16-bit clock is Clock A and the 8-bit clock is Clock B. Signal designation will contain the lettering A or B to signify which clock is involved.

The Unibus interface consists of the device address decoding, interrupt logic and arbitration, and the Unibus signal receivers and drivers. On sheet 10 the address lines are received and routed with BSG SV (unisyn) to decode of DEVICE N.

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### M7025 CIRCUIT DESCRIPTION

When Run Grant occurs a Bus back is sent and D2 FREE (Bus Ready) is set. One tap response is then sent off the various, and not used, and the vector lines are put onto the Unibus. The vector address is switch selectable to avoid conflicts with other devices and is decoded with D2 B RSVP to decode a clock A or Clock B vector address. Since this interrupt is Clock A Clock B grants, it is not true sending a logical zero for vector address line no. When the CP accepts the vector address, it sends a BUS SV (Clock Sync) which clears the D2 A INTR and D2 B RSVP.

In the upper right of sheet 12 is the interrupt for Clock B. D2 RSVP is the only interrupt for the B clock interrupt enable is assumed if data bit RSVP is true and a load B Status Register occurs. The interrupt operates in the same manner as Clock A interrupt. Here vector line D6 is sent a logical one to signify a Clock B interrupt.

The bus data line receivers and drivers are on sheet 13 and 14.

The registers which are readable are multiplexed and driven onto the Unibus by the BMSR (B Buffer). The receiving of the Data Bus is also done by the BMSR.

The Clock A Counter, Present Buffer and Status register are located on sheet 13. The A Counter register is made up of 7143 cascading binary counters. D7 A Overflow occurs at the top counter is true when the An Counter is all ones and count up pulse is present. The A overflow is delayed and counted on 0 A Reloaded (located at the top right). This is used to re-clock the buffer data into the A Counter in modes 0 and 1. The A Buffer is made up of 7143 binary counters.
The count-down input is used to increment (2's complement increment) the A Buffer data in an increment mode. Data in the A Buffer can be from the A Counter or the buffered data line. The A Buffer data is multiplied by 4,655, two to one line multiplexer. The B Clock Counter, A and B Buffer and Status registers are located on sheet 8B. The B Counter is made up of 74194 binary counters. The overflow from the counter can even reload the counter with data in the A Buffer for from the buffered data bus.

A 20 MHz oscillator is used to generate timing pulses and various other frequencies that are a multiple of 20 MHz. The 20 MHz oscillator is divided on the lower left of sheet 8B, 74194. It is divided by (74194 M6 counters) to 1 MHz, 100 kHz, 10 kHz, and 1 kHz. These frequencies are divided by a 4 MHz counter to one frequency which is used to increment clock A Counter.

Clock B frequency dividend and multipliers are located on sheet 8A.

The line Schmidt Triggers are located on sheet 8B. These of the Schmidt Triggers inputs have threshold control and slope control. The Schmidt Triggers is used for line frequency detection of the output. The outputs of Schmidt Triggers one, two and the line frequency are synchronized to the timing pulses produced on sheet 8A. Refer to the timing chart in Figure 1 for timing relationship. The resistor/diode network on the input of ST1, ST2 and ST3 is for protection and converting the input to +5 to +10. The units 1000 input cannot exceed 10V.

**Figure 1: Timing Diagram**