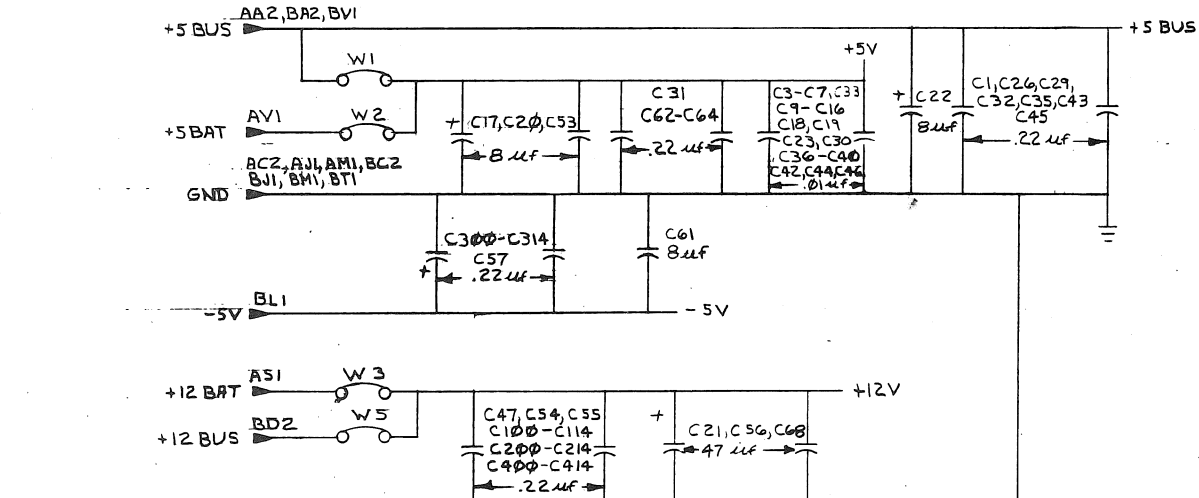
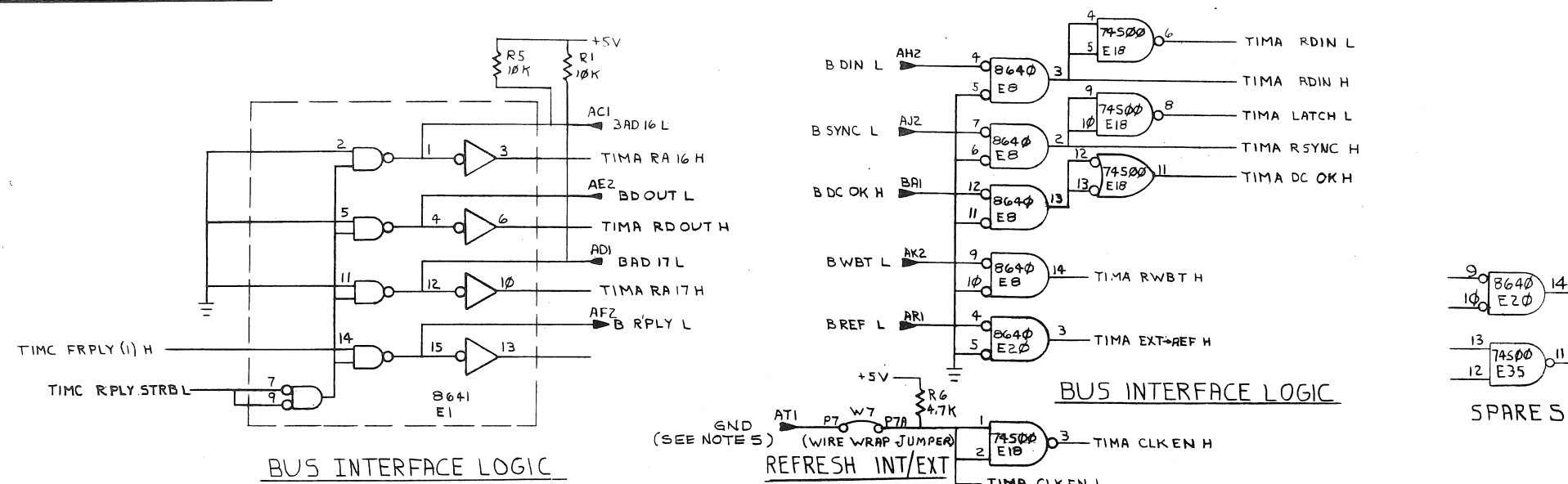
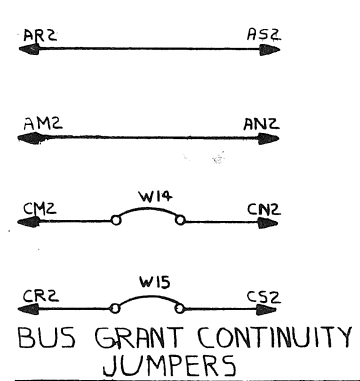
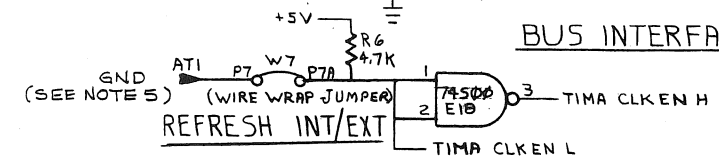


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- NOTES:**
- OPTION DESIGNATION:
 M7955-AA=M7955-YA OR M7955-YE
 M7955-AB=M7955-YB OR M7955-YF
 M7955-AC=M7955-YC OR M7955-YH
 M7955-AD=M7955-YD OR M7955-YJ
 - ALL 8641 BUS REC/DR PLUS 7483A ADDER AND 745138 DECODER ARE POWERED BY +5 BUS. ALL OTHER CIRCUITS GO TO +5V AS SELECTED BY W1 & W2.
 - W1, W2, W3, W5, W14, W15 ARE MACHINE INSERTABLE JUMPERS. W4, W6, W7, W8, W12, W16 ARE WIRE WRAP JUMPERS.
 - ALL BDAL-XX CONNECTIONS ARE BI-DIRECTIONAL LINES
 - DURING MANUFACTURING TEST, GROUND MAY BE REMOVED
- NOT USED REF DES**
- C100-C114, C200-C214, W8, W12, W16
 C100-C114, C200-C214, W12, W16
 C100-C114, W16



W6 W7 REFRESH OPTIONS

IN	IN	INTERNAL REFRESH WITH NO B R'PLY
IN	OUT	EXTERNAL REFRESH WITH NO B R'PLY
OUT	IN	ILLEGAL
OUT	OUT	EXTERNAL REFRESH WITH B R'PLY

REFRESH SELECTION

M7955 VARIATIONS JUMPERS -AA -AB -AC -AD

W4	1	1	1	1
W8	∅	1	1	1
W12	∅	∅	1	1
W16	∅	∅	∅	1

ALL JUMPERS NOTED AS ∅ MUST NOT BE INSTALLED

IC PIN LOCATIONS

I.C. TYPE	GND	+5	+12
555 @ E2	1	8	
555 @ E44	1		8
7493	10	5	
7483A	12	5	
74LS75	12	5	
8640	1	8	
OTHER 16 PIN I.C.'S	8	16	
OTHER 14 PIN I.C.'S	7	14	

STARTING ADDRESS SELECTION

STARTING ADDRESS	SWITCH S1 SETTINGS				
	-1	-2	-3	-4	-5
∅	1	1	1	1	1
4K	∅	1	1	1	1
8K	1	∅	1	1	1
12K	∅	∅	1	1	1
16K	1	1	∅	1	1
20K	∅	1	∅	1	1
24K	1	∅	∅	1	1
28K	∅	∅	∅	1	1
32K	1	1	1	∅	1
36K	∅	1	1	∅	1
40K	1	∅	1	∅	1
44K	∅	∅	1	∅	1
48K	1	1	∅	∅	1
52K	∅	1	∅	∅	1
56K	1	∅	∅	∅	1
60K	∅	∅	∅	∅	1
64K	1	1	1	1	∅
68K	∅	1	1	1	∅
72K	1	∅	1	1	∅
76K	∅	∅	1	1	∅
80K	1	1	∅	1	∅
84K	∅	1	∅	1	∅
88K	1	∅	∅	1	∅
92K	∅	∅	∅	1	∅
96K	1	1	1	∅	∅
100K	∅	1	1	∅	∅
104K	1	∅	1	∅	∅
108K	∅	∅	1	∅	∅
112K	1	1	∅	∅	∅
116K	∅	1	∅	∅	∅
120K	1	∅	∅	∅	∅
124K	∅	∅	∅	∅	∅

EXCEPT M7955-AD
 EXCEPT M7955-AC & AD
 EXCEPT M7955-AB, AC, & AD

OVER LAPPING IS NOT ALLOWED IN ANY PERIPHERAL PAGE

DRN. <i>[Signature]</i> 11/18/76	FIRST USED ON	MSVII-C	digital
CHK'D <i>[Signature]</i> 11/18/76	TITLE	MSVII-C MOS MEMORY, LSI (TIMA)	
ENG. <i>[Signature]</i> 11/18/76	PROD. ENG. <i>[Signature]</i> 11/19/76	SIZE	CODE
PROD. R. <i>[Signature]</i> 11/19/76	NEXT HIGHER ASSY.	D	CS
B-DD-M7955-0-0	SCALE	NUMBER	REV.
SHEET 1 OF 8	DIST.	M7955-0-1	B

REVISIONS

REV.	CHANGE NO.

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FAILING ROW	MEMORY SIZE			
	M7955-AA(4K)	M7955-AB(8K)	M7955-AC(12K)	M7955-AD(16K)
ROW 0	NO SWAPPING POSSIBLE	P4 TO P8A	REMOVE W4 ADD JUMPER P4 TO P12A	REMOVE W4 ADD JUMPER P4 TO P16A
ROW 1		* REMOVE W8	REMOVE W8 ADD JUMPER P8 TO P12A	REMOVE W8 ADD JUMPER P8 TO P16A
ROW 2			* REMOVE W12	REMOVE W12 ADD JUMPER P12 TO P16A
ROW 3				* REMOVE W16

1. DETERMINE MEMORY SIZE & REMOVE UPPER 4K ROW JUMPER. (INDICATED BY *)
2. LOCATE FAILING ROW, REMOVE SPECIFIED ROW JUMPER, ADD SWAPPING JUMPER IF FAILING ROW IS UPPER ADDRESS SPACE ROW, THERE IS NO SWAPPING JUMPER
3. THIS RECONFIGURED MEMORY BLOCK STILL HAS THE SAME STARTING ADDRESS AS BEFORE. IT OCCUPIES 4K LESS ADDRESS SPACE THAN BEFORE. RECONFIGURE STARTING ADDRESSES OF MEMORIES ABOVE THIS ONE IF NECESSARY SO THERE WILL BE CONTIGUOUS ADDRESS SPACE.

ROW SWAPPING MATRIX

ROW SELECTION

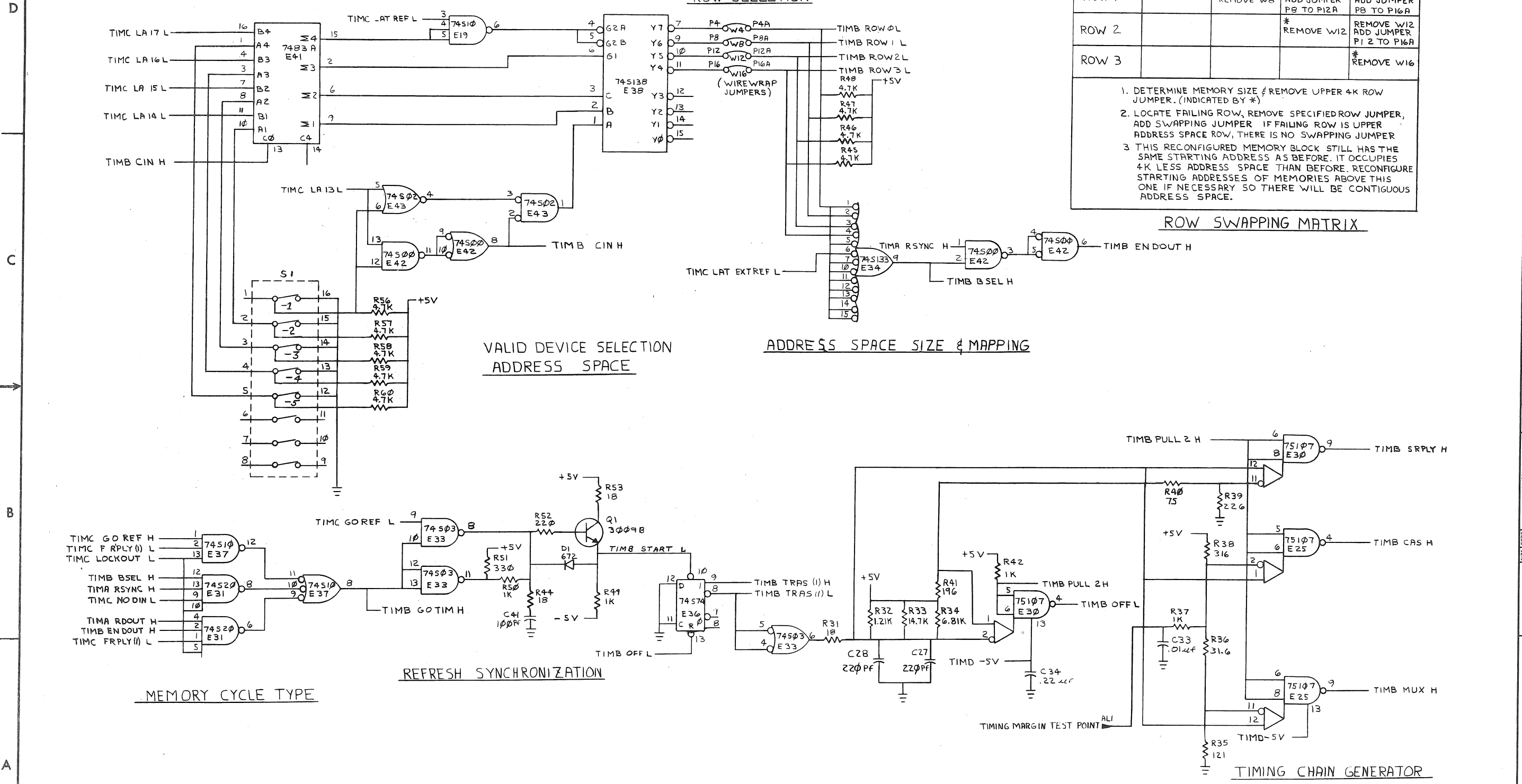
ADDRESS SPACE SIZE & MAPPING

VALID DEVICE SELECTION ADDRESS SPACE

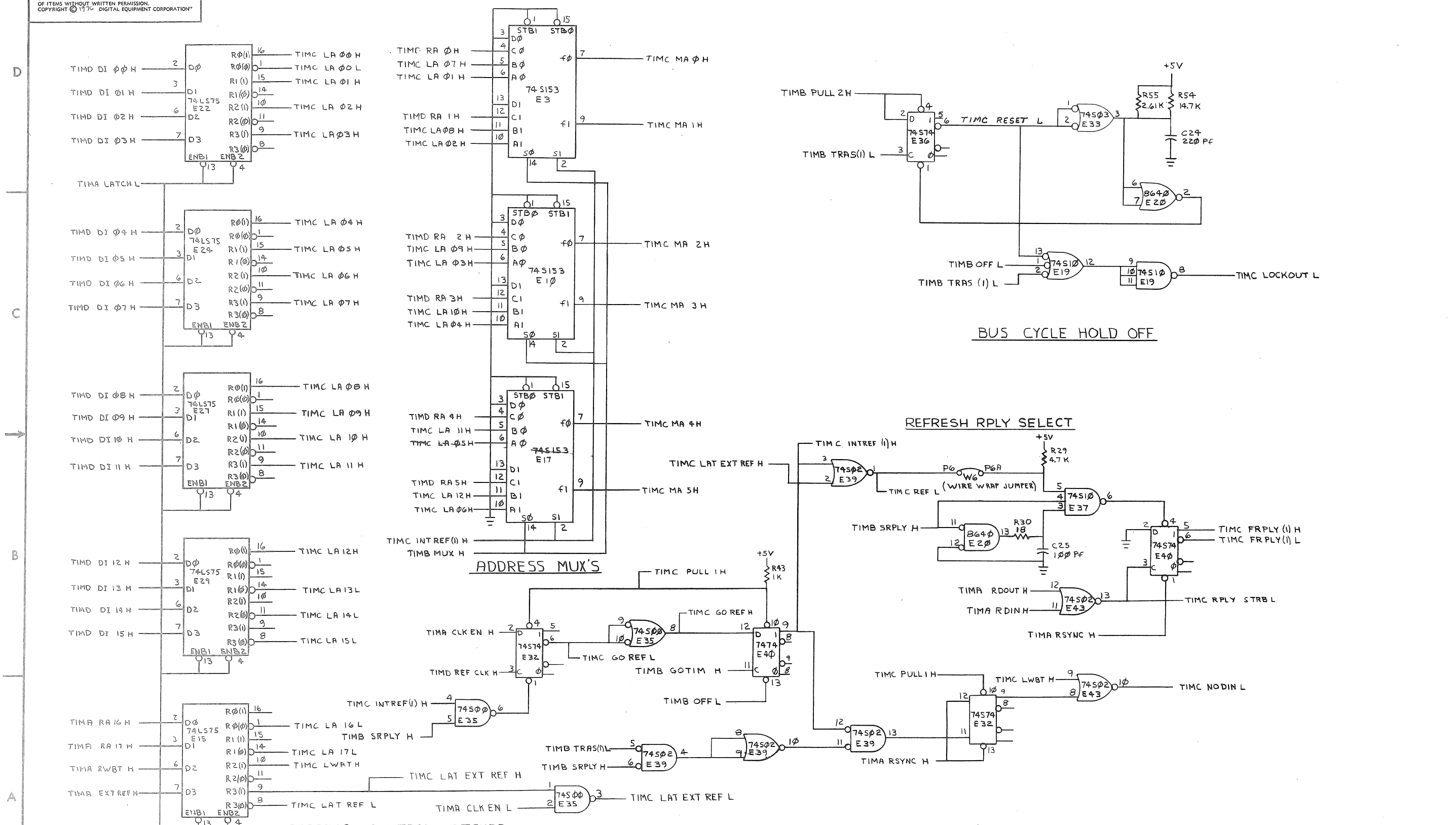
REFRESH SYNCHRONIZATION

MEMORY CYCLE TYPE

TIMING CHAIN GENERATOR



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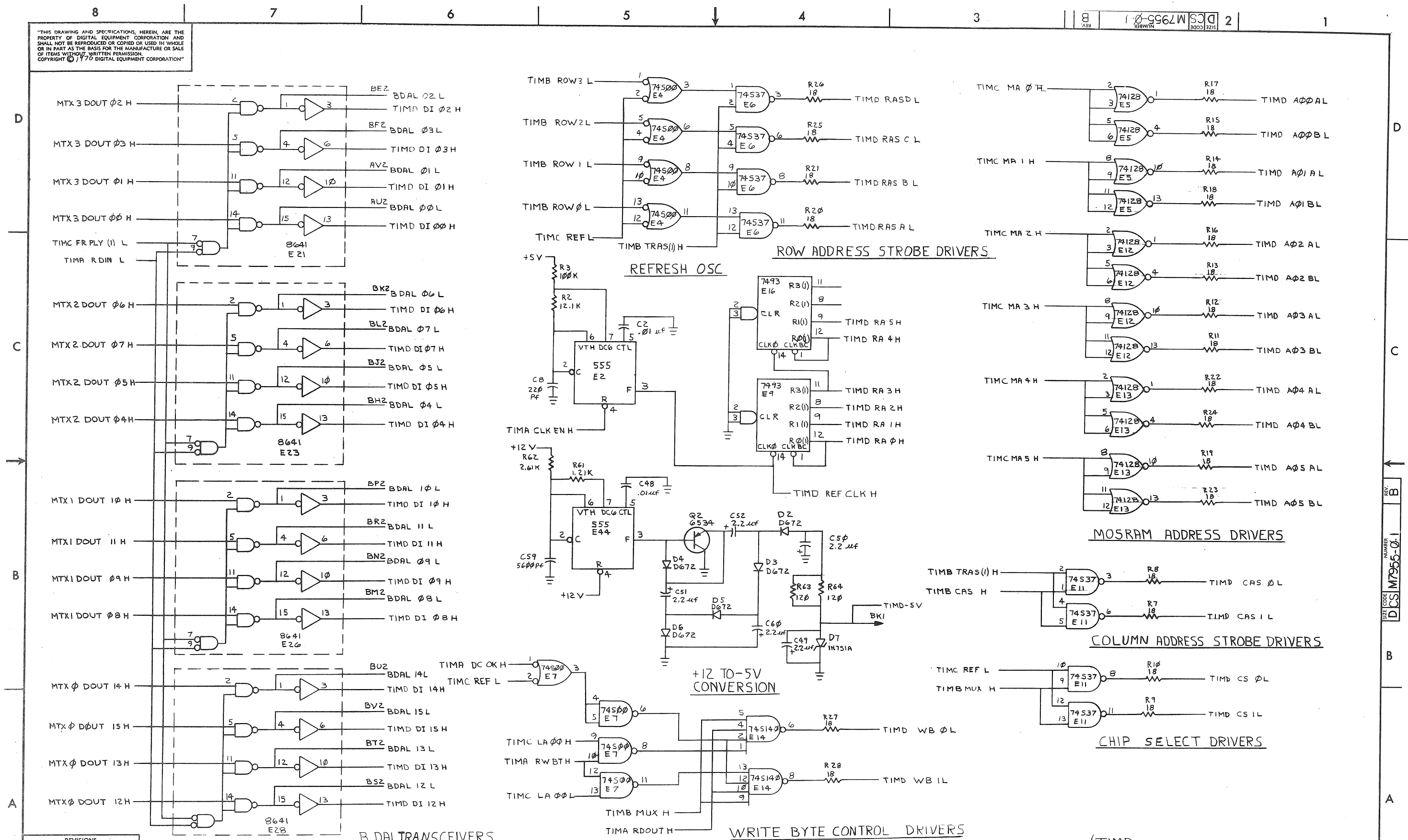
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CHK	CHANGE NO.	REV.

TITLE	(TIMC)	SIZE CODE	NUMBER	REV.
MSVII-C MOS MEMORY LSI	DCS	M7955-01	B	
SCALE	SHEET 3 OF 8	DIST.		

BLK. P116

REV. 1 DCS M7955-01

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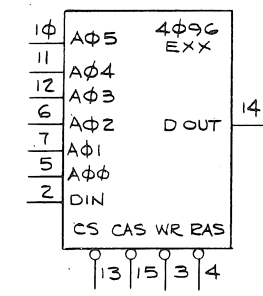
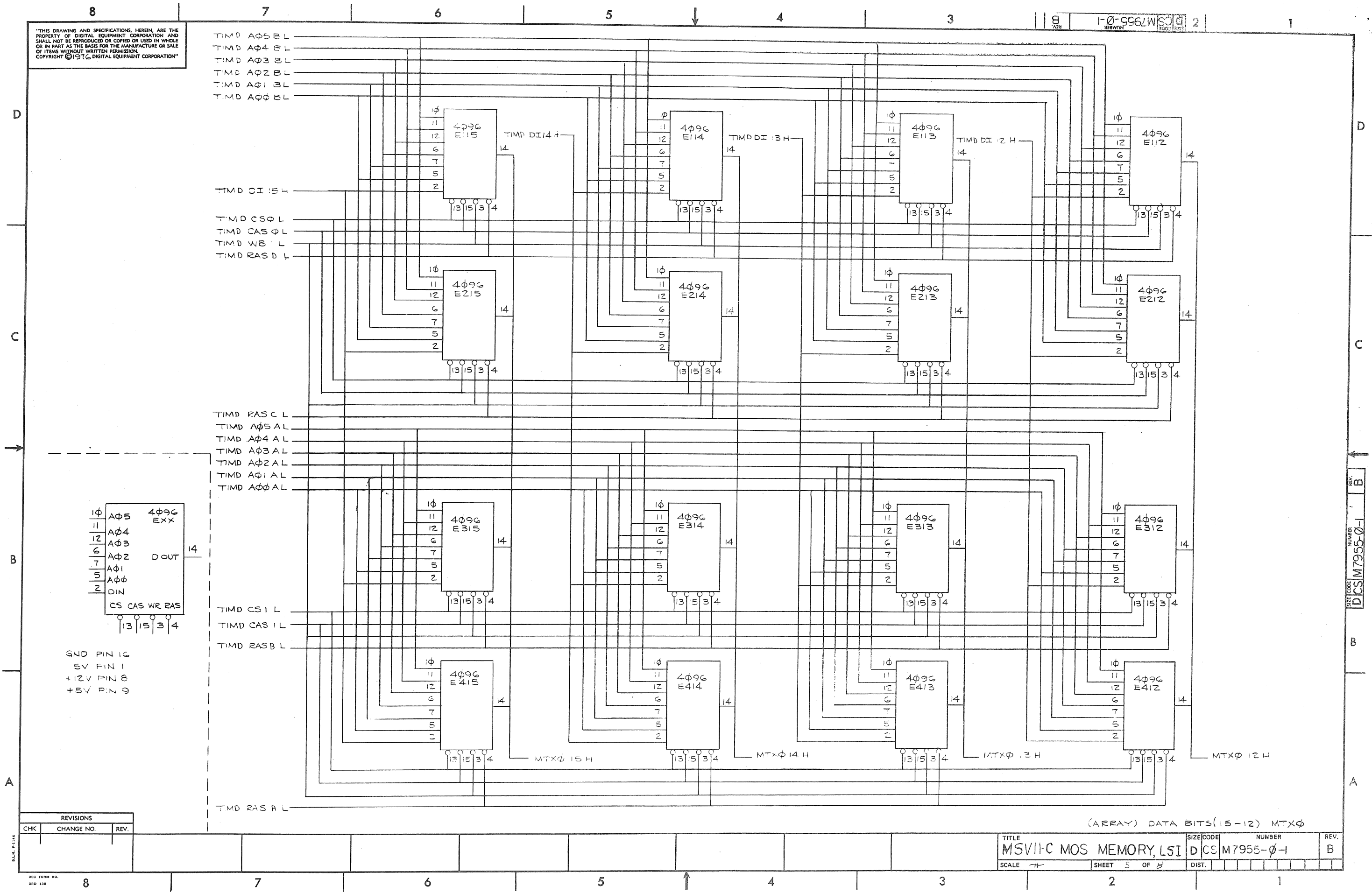
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CHK	CHANGE NO.	REV.

TITLE	(T1MD1) MSV11-C MOS MEMORY LSI	SIZE CODE	D CS	NUMBER	M7955-0-1	REV.	B
SCALE		SHEET	4	OF	8	DIST.	

REV. B NUMBER DCS M7955-0-1

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1-0-996/M7955-0-1



GND PIN 16
5V PIN 1
+12V PIN 8
+5V PIN 9

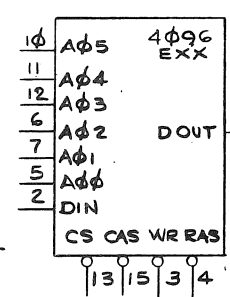
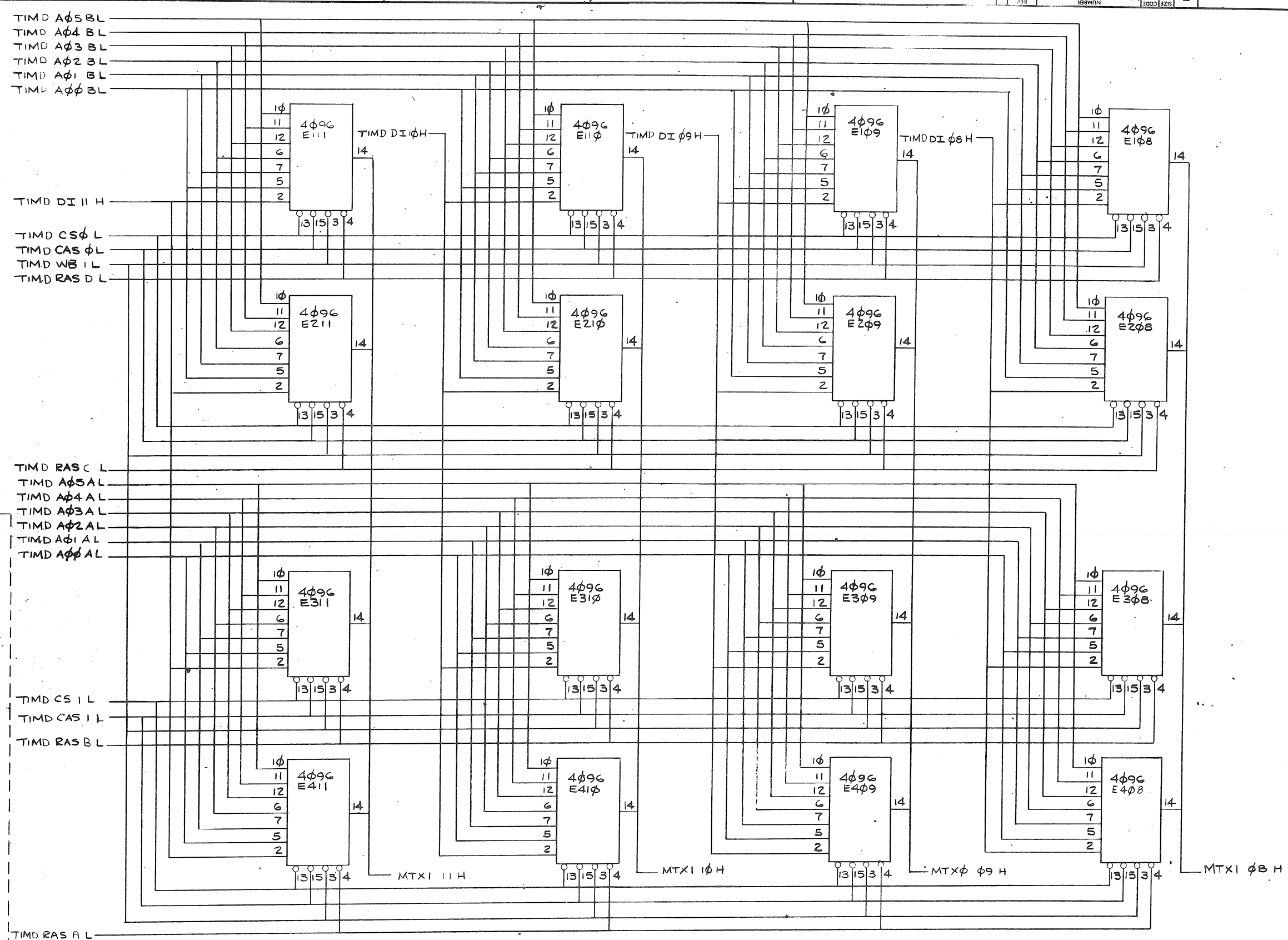
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: MSV11-C MOS MEMORY, LSI
 SCALE: 1/8
 SHEET: 5 OF 8
 SIZE CODE: DCS M7955-0-1
 NUMBER: B
 REV: B

SIZE CODE NUMBER
 DCS M7955-0-1
 REV. B

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REV. B
 SIZE CODE NUMBER
 DCS M7955-0-1



GND PIN 16
 -5V PIN 1
 +12V PIN 8
 +5V PIN 9

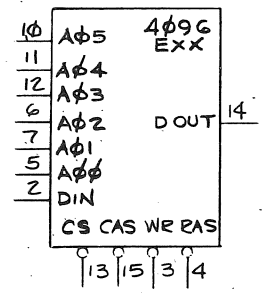
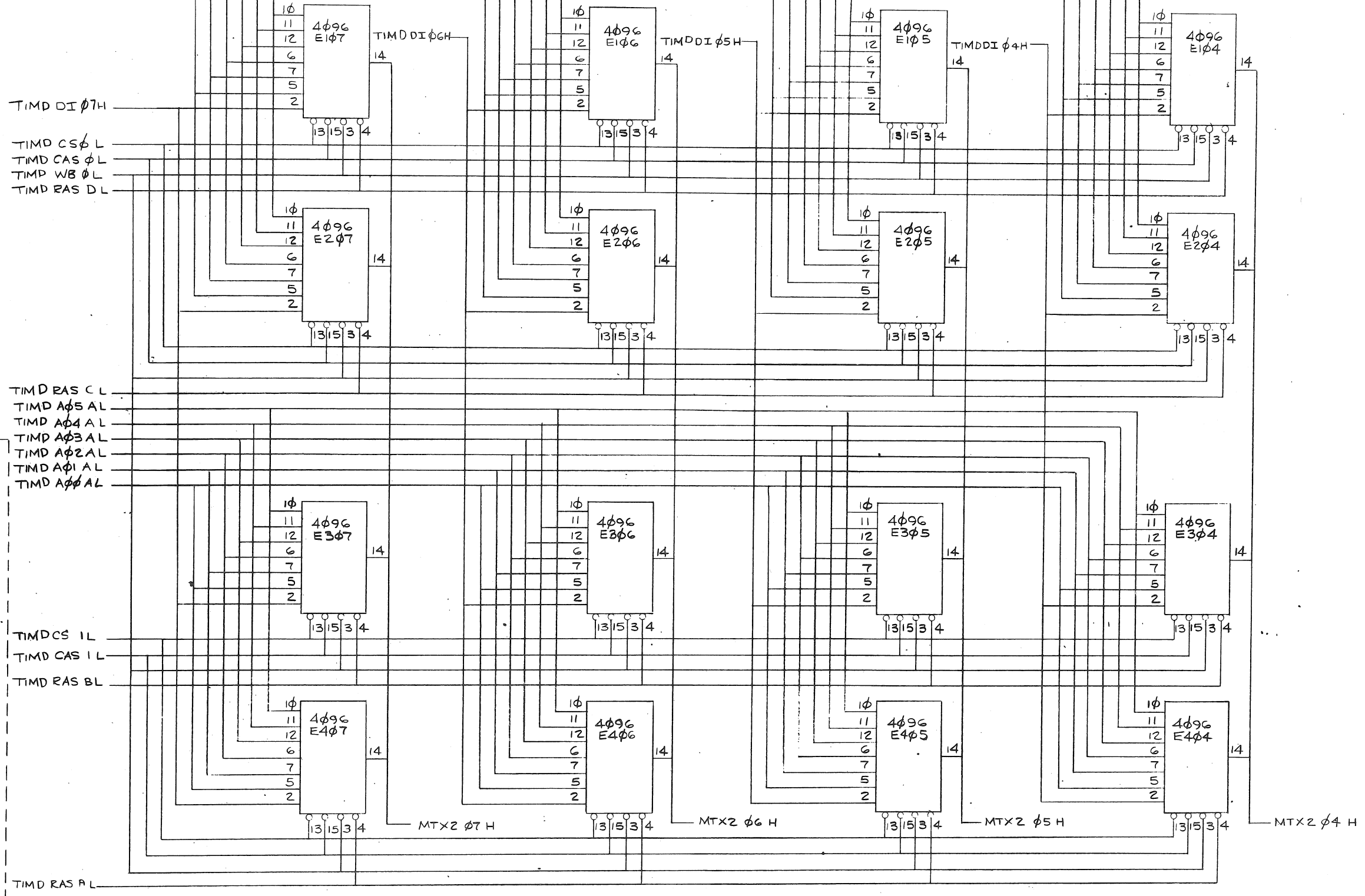
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE MSVII-CMOS MEMORY, LSI		SIZE CODE DCS	NUMBER M7955-0-1	REV. B
SCALE 1/8"	SHEET 6	OF 8	DIST.	

(ARRAY) DATA BITS (11-8) MTXI

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TIMD A ϕ 5 BL
 TIMD A ϕ 4 BL
 TIMD A ϕ 3 BL
 TIMD A ϕ 2 BL
 TIMD A ϕ 1 BL
 TIMD A ϕ 4 BL



GND PIN 16
 -5V PIN 1
 +12V PIN 8
 +5V PIN 9

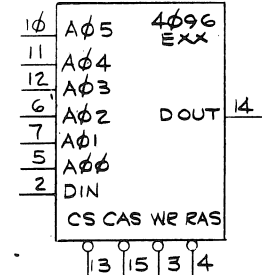
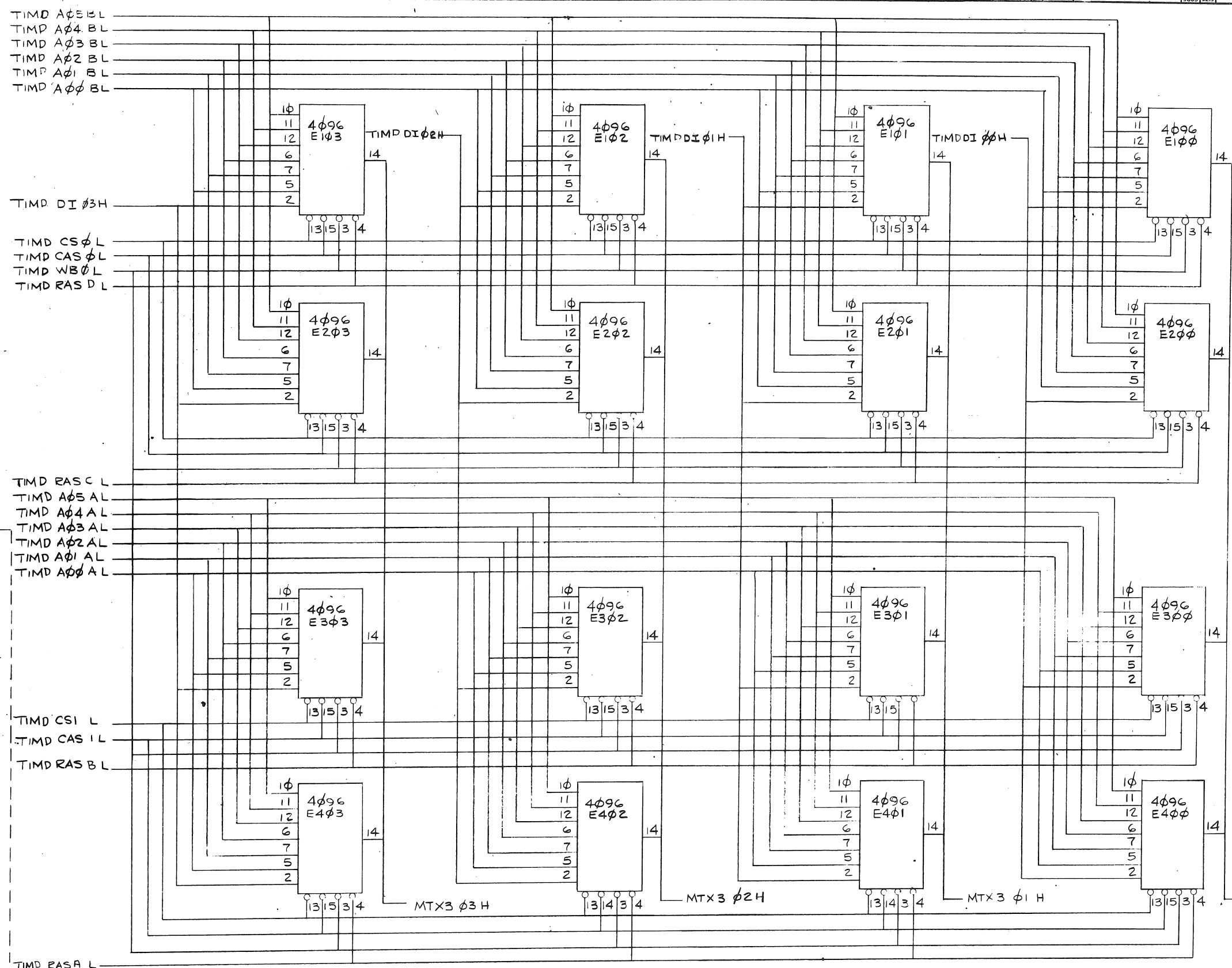
REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO. 138

(ARRAY) DATA BITS (7-4) MTX2

TITLE	MSVII-C MOS MEMORY, LSI	SIZE CODE	D CS	NUMBER	M 7955-0-1	REV.	B
SCALE	SHEET 7 OF 8	DIST.					

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GND PIN 16
-5V PIN 1
+12V PIN 8
+5V PIN 9

REVISIONS		
CHK	CHANGE NO.	REV.

(ARRAY) DATA BITS (03-00) MTX3

TITLE	MSV CMOS MEMORY, LSI	SIZE CODE	DCS	NUMBER	M7955-0-1	REV.	B
SCALE	1/4	SHEET	3	OF	3	DIST.	

REV. B
NUMBER M7955-0-1
SIZE CODE DCS

