

DMA10-F MEMORY LINK INTERFACE

FEATURES

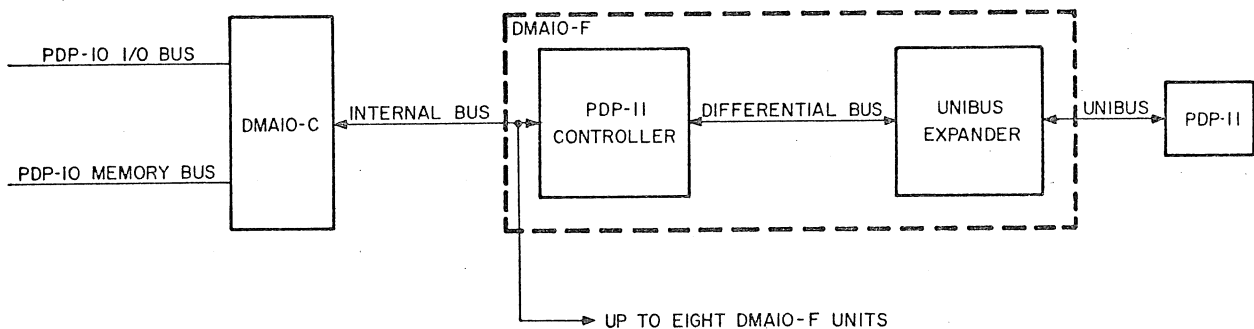
- Double Buffering
- Remote Separation
(80 feet between PDP-11 and DMA10-F)
- PDP-11 Uses PDP-10 Core As Its Own
- Highly Flexible Interprocessor Interrupt Capability
- Four PDP-11 Bytes Packed Per PDP-10 Word
- Dual Address Relocation and Boundary Register
(read-only and read/write segments)
- Sequential Address Detection

The DMA10-F Memory Link Interface forms a high-speed word transfer link between a PDP-10 memory and PDP-11 memories. The interface appears to be transparent to the PDP-11; that is, the PDP-11 may use the PDP-10 memory in the same manner as it uses its own memory.

The DMA10-F is comprised of two sections: the PDP-11 interface controller and the Unibus expander. The controller is the heart of the whole interface. Two relocation registers in the controller are provided to map the PDP-11 address into the PDP-10 memory

address space. An upper-boundary protection facility is provided to limit the size of the segments in PDP-10 memory. An interprocessor interrupt capability is implemented to facilitate communication between the PDP-10 and the PDP-11 processors.

The purpose of the Unibus expander is to provide an increased separation distance of up to 80 feet beyond the maximum Unibus length. The Unibus is converted to a differential bus in which the data and control signals are transmitted and received via differential send/receive circuits.



10-1010

System Block Diagram

SPECIFICATIONS

	PDP-11 Controller	Unibus Expander
Logic Panel	Three, Type H911	One, Type H911
Dimensions	15-3/4 in. h, 19 in. w, 16-3/4 in. d	5-1/4 in. h, 19 in. w, 16-3/4 in. d
Input Power	120/240 Vac	120/240 Vac
Line Frequency	50/60 Hz	50/60 Hz
Line Current	4A max	1A max
Power/Heat Dissipation	960W/3160 Btu/hr	250W/825 Btu/hr
Power Supplies	One, Type H720	One, Type H726F
Modules	M-Series	M-Series
Power Control	None	854
Memory Bus Loading	None	None
I/O Bus Loading	None	Three (Unibus)

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