PDP-8 MEMORY TUNING PROCEDURE

This procedure describes a method for checking out and tuning the basic 4K core memory and memory wing of the PDP-8 digital computer, using the rest of the computer (central processor wing and power supply). It is assumed that all of the equipment used is in working condition and properly calibrated.

TEST EQUIPMENT REQUIRED

The following test equipment is required for checking out and tuning the memory and memory wing, in addition to the ordinary hand tools. If the specified equipment is not available, a substitute may be used if its parameters equal or exceed those of the specified item.

<table>
<thead>
<tr>
<th>Test Equipment</th>
<th>Manufacturer and Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Computer</td>
<td>DEC, PDP-8</td>
</tr>
<tr>
<td>Oscilloscope</td>
<td>Tektronix, Type 547</td>
</tr>
<tr>
<td>Preamplifier</td>
<td>Tektronix, Type 1A1</td>
</tr>
<tr>
<td>Voltage Probes (2)</td>
<td>Tektronix, Type P6010</td>
</tr>
<tr>
<td>Current Probe with</td>
<td>Tektronix, Type P6016</td>
</tr>
<tr>
<td>Terminator or Pre-amplifier</td>
<td></td>
</tr>
<tr>
<td>Multimeter</td>
<td>Triplet, 630-NA</td>
</tr>
<tr>
<td>Program Tapes*</td>
<td>DEC, Maindec 802</td>
</tr>
<tr>
<td></td>
<td>(Checkerboard-Low and</td>
</tr>
<tr>
<td></td>
<td>Checkerboard-High)</td>
</tr>
</tbody>
</table>

*Optional, requires that an ASR-33 Paper Tape Reader be available.

PRELIMINARY

This part of the procedure is to be used before a new memory wing is first installed. If the memory wing has previously been checked out, go on to the next part, POWER. Figure 1 shows the flow of operations in this part.

Components

Check that all the modules listed below are installed in their correct locations. From the module side, location 1 is on the right and location 32 is on the left.
Figure 1. Preliminary Operations Flow Diagram
<table>
<thead>
<tr>
<th>Location</th>
<th>Module</th>
<th>Location</th>
<th>Module</th>
<th>Location</th>
<th>Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>MA25</td>
<td>GØ7</td>
<td>MCDØ6</td>
<td>G2Ø9</td>
<td>MC19</td>
<td>W6Ø7</td>
</tr>
<tr>
<td>MA26</td>
<td>GØ7</td>
<td>MCDØ7</td>
<td>G2Ø9</td>
<td>MC2Ø</td>
<td>B6Ø2</td>
</tr>
<tr>
<td>MA27</td>
<td>GØ7</td>
<td>MCDØ8</td>
<td>G2Ø9</td>
<td>MC21</td>
<td>G2ØE</td>
</tr>
<tr>
<td>MA28</td>
<td>GØ7</td>
<td>MCDØ9</td>
<td>G2Ø9</td>
<td>MC22</td>
<td>G2ØE</td>
</tr>
<tr>
<td>MA29</td>
<td>GØ7</td>
<td>MCDØ12</td>
<td>G2Ø9</td>
<td>MC24</td>
<td>G2Ø8</td>
</tr>
<tr>
<td>MA3Ø</td>
<td>GØ7</td>
<td>MCDØ13</td>
<td>G2Ø9</td>
<td>MC25</td>
<td>G2Ø8*</td>
</tr>
<tr>
<td>MA31</td>
<td>GØ7*</td>
<td>MCDØ14</td>
<td>G2Ø9</td>
<td>MD19</td>
<td>B1Ø4</td>
</tr>
<tr>
<td>MB25</td>
<td>GØ7</td>
<td>MCDØ15</td>
<td>G2Ø9</td>
<td>MD2Ø</td>
<td>B36Ø</td>
</tr>
<tr>
<td>MB26</td>
<td>GØ7</td>
<td>MC16</td>
<td>B684</td>
<td>MD21</td>
<td>G2Ø8</td>
</tr>
<tr>
<td>ME</td>
<td>GØ1</td>
<td>MD16</td>
<td>B2Ø4</td>
<td>MD22</td>
<td>G2Ø8</td>
</tr>
<tr>
<td>MB28</td>
<td>GØ7</td>
<td>MCDØ17</td>
<td>W3ØØ</td>
<td>MD24</td>
<td>G2Ø8</td>
</tr>
<tr>
<td>MB29</td>
<td>GØ7</td>
<td>MCDØ18</td>
<td>W3ØØ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MB3Ø</td>
<td>GØ7</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MB31</td>
<td>GØ8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Installed only when the 188 Parity Option is used.

Check that the core stack is fastened to the wing at MAB9-24 and the current limiting resistors are installed on the component plate at MAB1-8. The two WØ25 connectors with white wires from the core stack should be plugged into MCDØ and MCDØ11; the WØ25 connector with colored wires should be plugged into MCDØ2.

Check that eight G6Ø3 Memory Selection Matrix modules are plugged into the sockets on the side of the core stack, and that their contacts align with the connector contacts. If the contacts are not aligned, remove the module, file the shallow index keyway deep enough to align the contacts, and replace the module.

Check that a 6.8 microfarad 35 vdc capacitor is connected from the sense amplifier +1ØA, -15B, and +1ØP busses in either MA25-31 or MB25-3Ø to ground. Also check that a 22 ohm resistor is connected from the MEM STROBE bus at MA25L to ground.

**Wiring**

Check each of the power connections on the memory wing frame for shorts to ground or each other. Use an ohmmeter set to the XLØ scale and the positive probe on ground. With all the marginal power switches off (down), all connections except +1Ø and -15 should read ¥: the latter should read less than 1ØØ ohms. With all the marginal switches on MC (up), the
+1Ø and -15 connections should read Ø and the +1ØMC and -15MC connections should read less than 1ØØ ohms.

Check both the + and - sides of the R/W and INH terminals on the power supply for any short to ground. When this has been done, the memory wing can be mounted on the main computer frame, the power wires can be connected, and the cables from the central processor wing plugged into the memory wing.

Check the memory wing logic wiring for loose or broken wires, and foreign objects such as solder whiskers, pieces of wire, etc. Remove all foreign objects.

Check that all modifications have been made. In particular, check that one wire connects the following terminals together. If other wires are present or go to different terminals, remove and install the correct wire.

<table>
<thead>
<tr>
<th>MD17E</th>
<th>to</th>
<th>MD175</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCL7S</td>
<td>to</td>
<td>MCL7M</td>
</tr>
<tr>
<td>MCL8P</td>
<td>to</td>
<td>MCL8S</td>
</tr>
<tr>
<td>MCL8M</td>
<td>to</td>
<td>MCL8M</td>
</tr>
<tr>
<td>MCL8H</td>
<td>to</td>
<td>MCL8F</td>
</tr>
</tbody>
</table>

**NOTE:** These connections may be shown wrongly on the W3ØØ modules at the lower left of print BS-D-8M-Ø-15.

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**Logic Power**

Unplug the R/W and INH wires from their connections on the memory wing and be sure they are not touching anything. Then turn the POWER switch on: the fans should now be running. Set the voltmeter to the 3Ø vdc scale and measure the +1Ø volts on all the +1Ø volt busses (A terminals) in the memory wing: it should be +1Ø ± 1/2 volts dc. Then measure the -15 volt busses (B terminals): they should have -15 ± 1/2 volts dc on them.

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**Memory Power**

Switch the voltmeter to the 6Ø vdc scale and measure the voltage across the R/W and INH connectors at the power supply. Each should read 3Ø ± 3 volts dc. If either is too low, turn the power switch off and check for a low resistance path.

Turn the POWER switch off, plug the R/W and INH wires into their connectors on the memory wing, and place the voltmeter probes across the INH terminals. Then turn the POWER switch back on and check the voltage. If less than 27 volts or significantly less than previously measured, turn the POWER switch off and check the inhibit circuit in the memory wing. If normal,
POWER

Disconnect INH and R/W wires, turn on computer, and check Memory logic power.

+10 ± .5v. ?
No Find and fix faulty +10v.
Yes

-15 ± .5v. ?
No Find and fix faulty -15v.
Yes

INH = 30 ± 3v. ?
No Find and fix faulty INH.
Yes

R/W = 30 ± 3v. ?
No Find and fix faulty R/W.
Yes

Turn off computer, connect INH and R/W wires, and turn the computer back on.

Check memory power.

INH ≤ 27v. ?
Yes Turn off power, find and fix the faulty circuit.
No

R/W ≤ 27v. ?
Yes Turn off power, find and fix the faulty circuit.
No

Turn off computer, remove B360 from MD20, turn back on, and press START.

Runs OK ?
No Find and fix fault in CP.
Yes

Check Inhibit currents

Any waveforms ?
Yes Ω Repair and/or replace bad MEM ENABLE flip-flop
No

Signal on MD19P ?
Yes Repair and/or replace bad B602 in MC20.
No

Pulse on MD19K ?
Yes
No

Pulse on MC19L ?
Yes Repair and/or replace bad B104 in MD19.
No

Pulse on MC18D ?
Yes Repair and/or replace bad W607 in MC19.
No

Signal on MD18H ?
Yes Repair and/or replace bad W300 in MCD13 or bad INHIBIT flip-flop
No

POWER

Figure 2. Power Check Procedures Flow Diagram, sheet 1.
Figure 2. Power check Procedures
Flow Diagram, sheet 2.
check the R/W voltage: again turn the POWER switch off if less than 27 volts or significantly less than previously measured.

Turn the POWER switch off and remove the B36Ø module from MD2Ø. (This is the MEMORY STROBE delay module — when missing the MB register can never be set by the contents of any cores). Now turn the POWER switch back on and, after the memory power delay, press the START key. The computer should run continuously, cycling through memory as it reads and writes all zeros. The AND, FETCH, EXECUTE, and RUN indicators should be on. If not working properly, correct the trouble before proceeding further.

**Inhibit Current**

Set up the oscilloscope for external triggering, and trigger it with the BT2A pulse. (This is a negative pulse obtained at MD3ØU). Then connect the current probe and its terminator or preamplifier to the input of channel 1 and a voltage probe to the input of channel 2. Calibrate both probes, then adjust the sensitivity of channel 1 for 5Ø milliamperes per centimeter and of channel 2 for 2 volts per centimeter.

Observe the bit 5 inhibit current by placing the current probe around the yellow wire from MC 24N. If normal, adjust the potentiometer on the outside G8Ø8 (located in the power supply) for an inhibit pulse amplitude of 31Ø milliamperes. If not normal, move the current probe to another yellow wire in the same vicinity and adjust the inhibit current.

![Inhibit Current Waveforms](image)

Figure 3. Representative Inhibit Current Waveforms.

Check all 12 (or 13 if the Parity Option is used) inhibit currents. Use the yellow wires from the terminals listed below. If the timing is wrong, check the INHIBIT flip-flop in the B2Ø4 at MD16 (see drawing BS-D-8M-Ø-15) and/or the W3ØØ
at MCD18. If one bit is abnormal, swap the G2Ø8 module with a known good one to determine if the module is bad. Be sure the POWER switch is off when removing and replacing modules.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Output</th>
<th>Bit</th>
<th>Output</th>
<th>Bit</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ø</td>
<td>MC21E</td>
<td>4</td>
<td>MC24E</td>
<td>8</td>
<td>MD22E</td>
</tr>
<tr>
<td>1</td>
<td>MC21N</td>
<td>5</td>
<td>MC24N</td>
<td>9</td>
<td>MD22N</td>
</tr>
<tr>
<td>2</td>
<td>MC22E</td>
<td>6</td>
<td>MD21E</td>
<td>1Ø</td>
<td>MD24E</td>
</tr>
<tr>
<td>3</td>
<td>MC22N</td>
<td>7</td>
<td>MD21N</td>
<td>11</td>
<td>MD24N</td>
</tr>
<tr>
<td>P</td>
<td>MC25N</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Read/Write Current

Observe the Y axis read and write current waveforms by placing the current probe around the yellow wire from MCL2N. If normal, adjust the potentiometer on the inside G8Ø8 (located in the power supply) for read and write pulse amplitudes of 33Ø milliamperes. If not normal, decrease the oscilloscope sweep speed and observe the abnormal envelope. Then, with alternate sweeps in use, look at the outputs and inputs of the G2Ø9 modules in MCD12-15 to determine which (if any) is faulty. (Use drawing BS-D-8M-Ø-13). Turn off the POWER switch and swap the seemingly-bad module(s) for a good one(s) to see if the G2Ø9 module or G6Ø3 module is at fault. If not these modules, check the MB levels.

![Waveform Diagram]

Figure 4. Representative Read and Write Current Waveforms.

Observe the X axis read and write current waveforms by placing the current probe around the yellow wire from MCØ9N. These should be the same as those for the Y axis. If the amplitude has not already been set, adjust it for 33Ø milliamperes with the inside G8Ø8 in the power supply. Be sure all malfunctions are corrected in both axes before proceeding further.
**CLAMPS**

**First Stage Clamp**

Check the first stage clamp voltage with respect to -15 volts. Set the voltmeter to the 6 volt dc scale, place the negative probe on the -15 volt bus (B terminals), and look at terminals MA31M and MB30M. Each should read approximately 4.0 volts. If different, check the circuit for low-resistance shorts.

**Second Stage Clamp**

Check the second stage clamp voltage with respect to -15 volts. Change the voltmeter to the 12 volt dc scale and look at terminals MA31N and MB30N with the positive probe. The meter should read approximately 7.2 volts. If not, adjust it to this value with the lower potentiometer on the GØØ8 in MB31.

Now place the oscilloscope voltage probe on terminals E and F of every sense amplifier in MA25-31 or MB25-3Ø. Both terminals should show identical signals at +8.0 volts dc. Readjust the second stage clamp voltage for this operating level if it is different. If any individual GØØ7 Sense Amplifiers are at different levels, check both the first and second stage clamp voltages at terminals M and N, respectively, to be sure they are the same as the other modules. If not, remove and check the module.

**STATIC BALANCE**

Remove the sense lines from the GØØ7 sense amplifiers, set the voltmeter to the Ø.3 volt dc scale and measure the voltage between terminals E and F of all the sense amplifiers in MA25-31 and MB25-30. These should be within ± 25 millivolts of each other, but may be as much as 75 millivolts if the memory has been tuned before. If more than 75 millivolts, adjust the balance potentiometer R4 on the module for a minimum voltage. If a good balance cannot be obtained, the module must be repaired. Before removing it, check the first and second stage clamp voltages to see if they are different from the other sense amplifiers.
Figure 5. Clamp Procedure Flow Diagram.
Figure 6. Static Balance and DC Tracking Procedure Flow Diagram
DC TRACKING

With the inputs of all the sense amplifiers open, measure the voltage difference between the modules on terminals E and on terminals F. Set the voltmeter on the 0.3 volt dc scale and put one probe on terminal E of some sense amplifier such as bit 0 in MA25. Then look at terminal E of the other sense amplifiers, being careful about the polarity. The reading between the highest and the lowest must not exceed 200 millivolts. If any module is more than 200 millivolts from the others, recheck its static balance and readjust if necessary. If it is still more than 200 millivolts from the others, it must be removed and repaired.

Repeat the above process for terminals F of all the sense amplifiers. When finished, connect the core sense lines to the modules. Use drawing BS-D-8M-0-15 to locate any specific sense amplifiers.

SLICE VOLTAGE

Set the voltmeter to the 12 volt dc scale and measure the slice voltage between ground and MA31H. It should be +7.2 volts (0.8 volts less than the sense differential amplifier dc levels). If different, adjust the upper potentiometer on the G008 at MB31 for this voltage.

SENSE AMPLIFIER TUNING

Replace the oscilloscope current probe with the second voltage probe, and set the channel 1 gain to 1 volt per centimeter. Now look at the slicer output, terminal J, of all the sense amplifiers in MA 25-31 and MB25-30. A dc level of +0.7 volts should be observed. Place the channel 2 probe on terminal E, then F, of the same module and check that there is no slicer response during the core=0 responses of the amplifier. Be sure all sense amplifiers are checked, and that the core=0 response of the amplifier does not exceed 0.5 volts.

With probe 1 on MA25J and probe 2 on MA25E (bit 0), place a temporary jumper from ground to MC21D. (This is the bit 0 inhibit driver: the jumper disables it, causing a 1 to be written in this bit throughout the memory). The core=1 response of the amplifier should now be seen on channel 1.
TUNING

Check all the core=∅ differential amplifier outputs on terminals E and F of all G007's.

Any bit missing? Yes -> All addresses? No -> Recheck READ and WRITE currents. R/W

No

Yes

Exchange inputs with another G007

Still missing? Yes -> Replace the bad Core Stack. PRELIMINARY

No

Noise? Yes -> Repair and/or replace bad G007. BALANCE

No

Any < 0.5 v.? Yes -> All < 0.5 v.? Yes -> Slightly increase the INH current. TUNING

No

ZERO

Check all the slicer outputs on terminal J of all G007's.

Core = ∅ response? Yes

No

Noisy? Yes -> Repair and/or replace bad G007. BALANCE

No

+0.7 v. DC level? No

Yes

Figure 7. Sense Amplifier Tuning Flow Diagram.
Ground the MD input of an Inhibit Driver and check the core=1 differential amplifier outputs of a C07.

Both ≥2.9 v.?

Yes

No

Repair and/or replace bad C07. → BALANCE

Noisy ?

Yes

No

Slightly decrease the second stage clamp voltage. → ONE

Any clipping ?

Yes

No

Check the slicer output on terminal J of all the Sense Amplifiers.

Good waveforms ?

Yes

Noisy ?

No

Adjust the Slice Level. → ONE

No

Yes

-4±.3 v.?

No

Repair and/or replace bad C07. → BALANCE

Yes

Balanced ?

No

Adjust balance potentiometer R4. → ONE

Yes

Wide dispersion ?

Yes

No

Replace bad Core Memory Stack. → PRELIMINARY

No

Slow core ?

Yes

No

STROBE
Check that the amplitude of this signal is at least 2 volts, and that no core=∅ responses are produced. The slicer output must have a negative trapazoidal wave for each core=1 response, both negative and positive. See Figure 7 for representative waveforms.

Check the slicer output waveform on terminal J carefully. Its amplitude must go to -4.0 ± 0.3 volts. Its width, at the +0.7 volt dc level, must equal the width of the core=1 response at the +7.2 volt slice level. There should be a little time jitter in the rising and falling times; this should equal the same time jitter of the core=1 output at the slice level caused by differences of core response. This is called the core dispersion.

If the sense amplifier is both statically and dynamically balanced, then each half of the differential amplifier and slicer will have equal gain and two equal response waveforms will be produced as the computer cycles through the alternating core arrangement. Slightly readjust the potentiometer on the sense amplifier to minimize the difference between the two falling and rising waveforms: try to get the rising waveforms to coincide. If the sense amplifier cannot be dynamically balanced, it must be removed and repaired.

If any core has a slow response time, the falling waveform will be delayed and/or distorted (See Figure 8). If this occurs, the core stack must be rejected. To look at a specific location, connect a temporary jumper from ground to PDL8D, shorting out the COUNT PC pulse. Then set the switch register to the address desired, press LOAD ADDRESS, and finally press START.

If there is a lot of time jitter in the falling and rising waveforms, it can be caused by excessive core dispersion, poor common mode rejection in the differential amplifiers, or read and write currents that are too great or which do not change linearly. Poor common mode rejection can be recognized because other sense amplifiers will not show this problem. When this occurs, the sense amplifier must be removed and repaired. When the problem is in the memory, examine the read and write current waveforms carefully. If they are smooth and the proper size (33∅ milliamperes), then the core stack has too much dispersion and it must be rejected. However, try a smaller read and write
Figure 8. Typical Sense Amplifier Output Waveforms
current (and consequently a smaller inhibit current) and see if this improves the slicer waveforms. (Be sure you can get a 2 volt core=1 response from the differential amplifiers).

Repeat the above process for every bit, placing the jumper and probes at the locations listed below.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Ground Jumper</th>
<th>Probe 1 (slicer)</th>
<th>Probe 2 (amplifier)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ø</td>
<td>MC21D</td>
<td>MA25J</td>
<td>MA25E or F</td>
</tr>
<tr>
<td>1</td>
<td>MC21T</td>
<td>MB25J</td>
<td>MB25E or F</td>
</tr>
<tr>
<td>2</td>
<td>MC22D</td>
<td>MA26J</td>
<td>MA26E or F</td>
</tr>
<tr>
<td>3</td>
<td>MC22T</td>
<td>MB26J</td>
<td>MB26E or F</td>
</tr>
<tr>
<td>4</td>
<td>MC24D</td>
<td>MA27J</td>
<td>MA27E or F</td>
</tr>
<tr>
<td>5</td>
<td>MC24T</td>
<td>MB27J</td>
<td>MB27E or F</td>
</tr>
<tr>
<td>6</td>
<td>MD21D</td>
<td>MA28J</td>
<td>MA28E or F</td>
</tr>
<tr>
<td>7</td>
<td>MD21T</td>
<td>MB28J</td>
<td>MB28E or F</td>
</tr>
<tr>
<td>8</td>
<td>MD22D</td>
<td>MA29J</td>
<td>MA29E or F</td>
</tr>
<tr>
<td>9</td>
<td>MD22T</td>
<td>MB29J</td>
<td>MB29E or F</td>
</tr>
<tr>
<td>10</td>
<td>MD24D</td>
<td>MA30J</td>
<td>MA30E or F</td>
</tr>
<tr>
<td>11</td>
<td>MD24T</td>
<td>MB30J</td>
<td>MB30E or F</td>
</tr>
<tr>
<td>P</td>
<td>MC25T</td>
<td>MA31J</td>
<td>MA31E or F</td>
</tr>
</tbody>
</table>

STROBE

Turn the POWER switch off, replace the B36Ø in MD2Ø, and ground MD24T with a temporary jumper. Turn the POWER switch back on, and press START. Place probe 1 on MB3ØJ and observe the output of the bit 11 slicer. Place probe 2 on MB3ØF and observe the MEMORY STROBE pulse. Adjust the delay line on the B36Ø at MD2Ø until the leading edge of the MEMORY STROBE pulse occurs at or just past the midpoint of the slice output. Refer to Figure 9 for typical waveforms.

Check the SAll pulse output by moving probe 1 to M33ØK. The pulse must go positive to ~0.3 volts at least, and must be at least 8Ø nanoseconds wide. If not, the sense amplifier module must be removed and repaired. Then check all the other output pulses by grounding the corresponding inhibit driver inputs. (Note that the instruction register decoder may require ground jumpers on PB27H, PB27F, and PB27L in order to cycle when grounding bits Ø, 1, and 2).
STROBE

Turn the POWER switch off, replace the B360 in M20, turn the POWER switch back on, and press START.

Ground the MB input of an Inhibit Driver, and check the Strobe and slicer output.

Time right?

No Adjust the MEM STROBE delay line

Yes

Check the SA pulse output of the Sense Amp.

Good waveform?

No Repair and/or replace bad G027.

Yes

All done?

No

Remove all jumpers.

Working?

No TUNING

Yes

MARGINS

Figure 9. Strobe Operations Flow Diagram
<table>
<thead>
<tr>
<th>Bit</th>
<th>Ground Jumper</th>
<th>Probe 1 (pulse output)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ø</td>
<td>MC21D</td>
<td>MA25K</td>
</tr>
<tr>
<td>1</td>
<td>MC21T</td>
<td>MB25K</td>
</tr>
<tr>
<td>2</td>
<td>MC22D</td>
<td>MA26K</td>
</tr>
<tr>
<td>3</td>
<td>MC22T</td>
<td>MB26K</td>
</tr>
<tr>
<td>4</td>
<td>MC24D</td>
<td>MA27K</td>
</tr>
<tr>
<td>5</td>
<td>MC24T</td>
<td>MB27K</td>
</tr>
<tr>
<td>6</td>
<td>MD21D</td>
<td>MA28K</td>
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<td>MD21T</td>
<td>MB28K</td>
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<tr>
<td>8</td>
<td>MD22D</td>
<td>MA29K</td>
</tr>
<tr>
<td>9</td>
<td>MD22T</td>
<td>MB29K</td>
</tr>
<tr>
<td>1Ø</td>
<td>MD24D</td>
<td>MA3ØK</td>
</tr>
<tr>
<td>11</td>
<td>MD24T</td>
<td>MB3ØK</td>
</tr>
<tr>
<td>P</td>
<td>MC25T</td>
<td>MA31K</td>
</tr>
</tbody>
</table>

Remove all jumpers when finished. Then check that both 1's and Ø's can be deposited and examined throughout the memory.

**MARGINS**

If the ASR 33 or other paper tape reader is available and working, first load the RIM Loader subroutine into memory (see Appendix 1), then read in the checkerboard-low tape. If a paper tape reader is not available, load this program in memory manually. Set the Switch Register (SR) to ØØØ1 and press LOAD ADDRESS, then set the SR to Ø1ØØ* and press START.

Place probe 1 on the slice level bus (H terminals in MA25-31 and MB25-30) and probe 2 on the output of some differential amplifier (terminal E or F in MA25-31 or MB25-3Ø). Set both channels for a gain of 2 volts per centimeter with ground reference on the lowest grid line.

Turn the SENSE AMP switch on the memory wing to MC, then very slowly decrease the +1Ø volt marginal voltage. When the program halts at location 71, record the contents of the ACCUMULATOR indicators (the bit that is on or off is the bit (sense amplifier) that failed) and the marginal voltage. Then return the marginal voltage to +1Ø volts and press CONTINUE.

* For EMI or Ferroxcube core memories. Refer to the Maindec 8Ø2 write-up if other memories are used.
The computer will halt again at location 74, with the ACCUMULATOR indicators containing the address where the error occurred. The sense amplifiers must be able to operate with the marginal voltage reduced 5.5 volts (to +4.5 volts), and normally will operate 6 volts below normal (at +4 volts).

Press CONTINUE again to resume testing, and slowly increase the +10 volt marginal voltage until the program again halts at location 71. Once again note which single bit in the ACCUMULATOR indicators is on or off, decrease the marginal voltage to +16 volts, then press CONTINUE. Now note the address, and press CONTINUE again to resume testing. The sense amplifiers must be able to operate with the marginal voltage increased 5.5 volts (to +15.5 volts), and normally will operate 6 volts above normal (at +16 volts).

If the voltage spread is at least 11 volts and centered at +16 volts, then the memory is working passably (it's working well if the spread is 12 volts or more). If the spread is reasonably wide but not centered, set the marginal voltage to whichever margin it will work at, then change the slice level until the program fails at this point. Return the marginal voltage to normal, press CONTINUE twice to restart the program, and vary the marginal voltage to the other extreme until the program again fails. In this manner the marginal spread can be centered using the slice level.

Rebalancing a sense amplifier can also help it to meet the marginal conditions. With the program running at normal marginal voltage, place probe 1 on terminal J of the sense amplifier that fails at high margins and observe the slicer output. Then place probe 2 on the MEMORY STROBE bus (terminal L) and adjust the two traces for a common ground reference. Now increase the marginal voltage and observe the slicer output move to the left as the sense amplifier speeds up. When the program fails (the trailing edge of the strobe pulse will occur with the trailing edge of the slicer output), reduce the marginal voltage a little bit and restart the program (by pressing CONTINUE twice), then adjust the balance potentiometer on the sense amplifier module until the two traces at the trailing edge of
the slicer output are as nearly together as possible. Then increase the marginal voltage again and see if it has improved enough. If it has, then check the lower marginal voltage limit to see if it has changed.

The same procedure can be used to improve the lower marginal voltage limits. In this case, the slicer output moves to the right as the sense amplifiers slow down.

If the same bit fails at both the upper and lower limits, it is due to either a poor core output in that plane, or a low sense amplifier gain, or both. Place probe 1 on terminal J of this module, and probe 2 on all the other slicer outputs (terminal J) and observe the relative widths of the waveforms when the program is running at normal margins. Find the sense amplifier with the widest response, and swap the two modules (be sure to turn the POWER switch off). Then check to see how much this has improved the margins.

Changing the read/write current, inhibit current, and/or the second stage clamp voltage can improve the marginal voltage limits slightly if done correctly. However, once any of these are changed, the slice level and probably one or more of the others must also be readjusted and a new set of marginal voltage limits established. Increasing the read and write currents increases the core=1 response and the noise in the rest of the core. The optimal inhibit current will produce the smallest core=0 response (as seen on terminals E and F). The second stage clamp voltage changes the operating level of both the second stage of the differential amplifiers and the slicer, with only small changes in gain and common mode noise rejection. The second stage clamp should only be changed slightly if limiting is noticed on one side of any sense amplifier output at either terminal E or F.
APPENDIX 1

RIM LOADER

The readin mode (RIM) loader is a short program that reads the contents of another program tape and loads it into memory. The program tape must be punched in the RIM format, i.e., first an absolute address and then the information to be placed in that address. This program will only work with the 33 ASR reader, and must be loaded into memory manually.

<table>
<thead>
<tr>
<th>Location</th>
<th>Content</th>
<th>Mnemonic</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>7700</td>
<td>6032</td>
<td>KCC</td>
<td>/Clear ac and reader flag.</td>
</tr>
<tr>
<td>7701</td>
<td>6031</td>
<td>KSF</td>
<td>/Skip if flag is set.</td>
</tr>
<tr>
<td>7702</td>
<td>5031</td>
<td>JMP .-1</td>
<td>/Do it again if flag is clear.</td>
</tr>
<tr>
<td>7703</td>
<td>6036</td>
<td>KRB</td>
<td>/Read buffer when filled.</td>
</tr>
<tr>
<td>7704</td>
<td>7106</td>
<td>CLL RTL</td>
<td>/Clear link and rotate left twice.</td>
</tr>
<tr>
<td>7705</td>
<td>7006</td>
<td>RTL</td>
<td>/Rotate left twice again for check.</td>
</tr>
<tr>
<td>7706</td>
<td>7510</td>
<td>SPA</td>
<td>/Skip if not leader or trailer.</td>
</tr>
<tr>
<td>7707</td>
<td>5301</td>
<td>JMP 7701</td>
<td>/Repeat if leader or trailer.</td>
</tr>
<tr>
<td>7710</td>
<td>7006</td>
<td>RTL</td>
<td>/Rotate left twice if program.</td>
</tr>
<tr>
<td>7711</td>
<td>6031</td>
<td>KSF</td>
<td>/Skip if flag is set.</td>
</tr>
<tr>
<td>7712</td>
<td>5311</td>
<td>JMP .-1</td>
<td>/Do it again if flag is clear.</td>
</tr>
<tr>
<td>7713</td>
<td>6034</td>
<td>KRS</td>
<td>/Read buffer without clearing ac.</td>
</tr>
<tr>
<td>7714</td>
<td>7420</td>
<td>SNL</td>
<td>/Skip if link is set.</td>
</tr>
<tr>
<td>7715</td>
<td>3720</td>
<td>DCA I .+3</td>
<td>/Deposit information in address.</td>
</tr>
<tr>
<td>7716</td>
<td>3320</td>
<td>DCA .+2</td>
<td>/Deposit address.</td>
</tr>
<tr>
<td>7717</td>
<td>5300</td>
<td>JMP 7700</td>
<td>/Repeat the entire program.</td>
</tr>
<tr>
<td>7720</td>
<td>0000</td>
<td>Z</td>
<td>/Storage for absolute address.</td>
</tr>
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APPENDIX 2

CHECKERBOARD

The following programs are Checkerboard-Low and Checkerboard-High. These may be loaded manually into memory in the event that the program tapes are not available, the RIM Loader is not working, or these programs do not work correctly. For a full description, flow chart, and operating instructions, refer to the MAINDEC 802 Memory Checkerboard Test manual.

<table>
<thead>
<tr>
<th>Location</th>
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<tr>
<td>3  7452</td>
<td>76Ø4</td>
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<tr>
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<td>31Ø5</td>
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<td>6</td>
<td>1111</td>
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<td>31Ø6</td>
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<td>Ø1Ø3</td>
</tr>
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<td>764Ø</td>
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<td>1Ø77</td>
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<td>11Ø6</td>
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<tr>
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<td>765Ø</td>
</tr>
<tr>
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<td>1Ø77</td>
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33 75ØØ     X     7ØØØ     7Ø4Ø     7Ø4Ø      CMA
34 75Ø1
35 75Ø2
36 75Ø3
37 75Ø4
40 75Ø5     STD
41 75Ø6
42 75Ø7
43 751Ø
44 7511
45 7512
46 7513
47 7514     CCK
50 7515
51 7516
52 7517
53 752Ø
54 7521
55 7522
56 7523
57 7524
60 7525
61 7526
62 7527
63 753Ø
64 7531
65 7532     CC2
66 7533
67 7534
70 7535     CC3
71 7536     EI
72 7537
73 754Ø
74 7541     EIÁ
75 7542
76 7543
77 7544     CC4
80 755Ø     HOT
81 7551     POT
82 7552     DOT
83 7553     NOT
84 7554     PXX
85 7555     SNL
86 7556     JMP CCK
87 7557     DCA I SA
88 7558     ISZ SA
89 7559     ISZ PAT
90 755A     TAD SA
91 755B     AND BOT
92 755C     SNA CLA
93 755D     JMP STC
94 755E     JMP X-2
95 755F     DCA WRD
96 7560     TAD I SA
97 7561     CMA IAC
98 7562     TAD WRD
99 7563     SZA CLA
100 7564     JMP CC3
101 7565     TAD WRD
102 7566     CMA
103 7567     DCA I SA
104 7568     TAD I SA
105 7569     IAC
106 756A     TAD WRD
107 756B     SZA CLA
108 756C     JMP CC3
109 756D     TAD WRD
110 756E     CLL
111 756F     JMP STD -1
112 7570     TAD I SA
113 7571     HLT
114 7572     CLA
115 7573     TAD SA
116 7574     HLT
117 7575     CLA CLI
118 7576     CLA CLI
119 7577     JMP CC2
120 7578     /Constant
121 7579     /Constant
122 757A     /Constant
123 757B     /Constant
124 757C     /Constant
125 757D     /Constant
126 757E     /Constant
127 757F     /Constant
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</table>

- Constant
- Variable