PM-DL11W Serial Line Interface Manual

Plessey Peripheral Systems

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October 1979 - Revision D

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701320
SCALE	REV D	SHEET 0-0

FORM 000021

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Section 1
General Information

1.1 INTRODUCTION

This manual provides the information needed to install and operate the PM-DL11W serial line interface with line time clock manufactured by Plessey Peripheral Systems, Irvine, California 92714.

The material is arranged into three sections as follows:

Section 1 - GENERAL INFORMATION. This section contains a brief description of the PM-DL11W and a list of the physical specifications of the interface.

Section 2 - INSTALLATION. This section explains the requirements and procedures for equipment installation. Interface information and switch settings for each option are provided.

Section 3 - FUNCTIONAL DESCRIPTION. This section contains a detailed functional description of the PM-DL11W including the format of the data word and function of each device register.

Section 4 - MAINTENANCE AND TROUBLESHOOTING. This section provides a brief description of board maintenance procedures.

Drawing Package: A separate drawing package is available. This document MD 701320 contains assembly drawings, parts lists, and schematics required for a complete understanding of the PM-DL11W.

1.2 GENERAL DESCRIPTION

The PM-DL11W is a serial line interface and a line time clock designed to operate in the Digital Equipment Corporation (DEC) PDP-11 series computers.* It is directly compatible to and is a plug for plug replacment for the DEC DL11-W. As a serial line interface it receives asynchronous serial data from an external device such as a teletype or CRT display and converts it to parallel data for transfer to the Unibus.* Parallel data from the Unibus is converted to serial data to be transmitted to the external device. As a line time clock the PM-DL11W initiates interrupt sequences at intervals determined by the line frequency.

*Teletype is a registered trademark of Teletype Corporation.
*DEC, PDP, and Unibus are registered trademarks of Digital Equipment Corp.

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The PM-DL11W contains a control and status register for programmer control and a data buffer register for storage of data prior to transfer to the external device.

Switch selection on the PM-DL11W card provides the flexibility to handle a variety of different terminals such as a teletype or a high speed CRT. The user may also select line speed, character size, stop code length, and parity error detection.

1.3 SPECIFICATIONS

The PM-DL11W is contained on a single 8.96" x 15.58" quad height printed circuit board. It can be used in conjunction with or in place of the DEC DL11-W serial line interface and line time clock.

The PM-DL11W can be mounted in any small peripheral controller (SPC) slot of a PDP-11 computer or any of the following backplanes:

- PM-D11/SPC-1 Plessey double systems unit
- PM-D11/SPC-2 Plessey single systems unit
- PM-F11/SPC Plessey double systems unit
- PM-F11/SPC-1 Plessey single systems unit
- DEC DD11-A DEC single systems unit
- DEC DD11-B DEC single systems unit
- DEC DD11-C DEC single systems unit
- DEC DD11-D DEC double systems unit
- DEC DD11-P DEC processor double systems unit

1.3.1 CONFIGURATION

The PM-DL11W is available in three versions as follows:

PM-DL11W - This version consists of the board assembly only.

PM-DL11WA - This version is used as a 20mA current loop electrical interface. It is furnished with a 4 foot cable terminated with Mate-N-Lock connectors suitable for connection to DEC terminals.

PM-DL11WB - This version is used to interface with EIA RS232C. It is supplied with a 25 foot cable terminated by a Cinch DB25P plug for connection to equipment with EIA interface.

PM-DL11WC - This version is used to interface with ADM3 type terminal interfaces. It is supplied with a 25 foot cable and requires no additional adapters.

1.3.2 POWER REQUIREMENTS

The current required to operate the PM-DL11W is shown in Table 1-1.

VOLTAGES	TYPICAL OPERATING CURRENT
+5V	2.0A
-15V	150 mA
+9 to +15V	50mA

Table 1-1: Power Requirements

Section 2

Installation

This section provides information for the installation of the PM-DL11W board. It also lists the various options available on the board and explains their incorporation.

2.1 UNPACKING AND INSPECTION

The PM-DL11W is shipped in a special packing carton designed to keep the board from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the interface requires reshipment.

To unpack the PM-DL11W, remove any packing materials and visually inspect for physical damage.

2.2 ASSEMBLY PART NUMBERS

PART NUMBER	ASSEMBLY
701065-100	Top Assembly, PM-DL11W
701116-100	Cable Assembly for PM-DL11WB
701117-100	Cable Assembly for PM-DL11WA
701239-100	Cable Assembly for PM-DL11WC

2.3 BOARD INSTALLATION

The PM-DL11W can be mounted in any small peripheral controller (SPC) slot of the PDP-11/05, 11/10, 11/35, and 11/40 processor backplanes. It can also be mounted in any of the following backplanes:

- PM-D11/SPC-1 Plessey double systems unit backplane.
- PM-D11/SPC-2 Plessey single systems unit backplane.
- PM-F11/SPC Plessey double systems unit backplane.
- PM-F11/SPC-1 Plessey single systems unit backplane.
- DEC DD11-A DEC single systems unit.
- DEC DD11-B DEC single systems unit.
- DEC DD11-C DEC single systems unit.
- DEC DD11-D DEC double systems unit.
- DEC DD11-P DEC processor double systems unit.

Mount the PM-DL11W in connectors C through F with the components facing connector row 1.

2.4 OPTIONS

The PM-DL11W contains four DIP switches for selection of baud rate, break bit enable, data word format, address selection, and vector address selection. Active and passive modes of operation are jumper selectable.

Refer to Figures 2-5 and 2-6 at the end of the section for location of switches and jumper configurations on the board. Directions for setting each switch and jumper are contained in the following.

SWITCH SW1

Switch SW1 controls the optional UART functions including data word format, break disable, and disable error bits. The format of the data word contains the following switch-selectable options: odd or even parity, number of data bits from 5 to 8, one or two stop bits and parity enable. Table 2-1 lists the UART options and their corresponding switch settings. Figure 2-5 at the end of the section shows the location of the switches on the board.

<table>
<tr><th>SWITCH 1
POSITION</th><th>FUNCTION</th></tr>
<tr><td>1</td><td>BREAK DISABLE. Opening this switch disables the break function.</td></tr>
<tr><td>2</td><td>Not used.</td></tr>
<tr><td>3</td><td>ODD OR EVEN PARITY. This switch is open for even parity and closed for odd parity.</td></tr>
<tr><td>5, 4</td><td>DATA BITS. These two switch positions select the number of data bits in a serial character. Switch settings are as follows where 1 = open and 0 = closed.
<table>
<tr><th>NUMBER OF BITS</th><th>POSITION 5</th><th>POSITION 4</th></tr>
<tr><td>5</td><td>0</td><td>0</td></tr>
<tr><td>6</td><td>1</td><td>0</td></tr>
<tr><td>7</td><td>0</td><td>1</td></tr>
<tr><td>8</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>6</td><td>STOP BITS. This switch selects the number of stop bits in the serial character. The switch is open for two stop bits and closed for one stop bit.</td></tr>
<tr><td>7</td><td>PARITY ENABLE. When this switch is closed it enables parity operation;when open it disables parity operation.</td></tr>
<tr><td>8</td><td>DISABLE ERROR BITS. When this switch is open it disables the error bits 12 through 15 of the receiver data buffer register.</td></tr>
</table>

Table 2-1: UART Function Switches

SWITCH SW2

Switch SW2 controls baud rate selection and line time clock enable.

The PM-DL11W provides completely independent speed selection for data transmission and reception. Baud rates for the receiver and transmitter are selectable using switch SW2 to any of the following rates: 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, and 9600. Table 2-2 shows the switch settings for baud rates and line time clock enable. Figure 2-5 at the end of the section shows the location of the switches on the board.

RECEIVER BAUD RATE

SWITCH 2 POSITION				BAUD RATE
7 (6)	5 (4)	3 (2)	1 (0)*	
ON	ON	ON	ON	0
ON	ON	ON	OFF	0
ON	ON	OFF	ON	50
ON	ON	OFF	OFF	75
ON	OFF	ON	ON	134.5
ON	OFF	ON	OFF	200
ON	OFF	OFF	ON	600
ON	OFF	OFF	OFF	2400
OFF	ON	ON	ON	9600
OFF	ON	ON	OFF	4800
OFF	ON	OFF	ON	1800
OFF	ON	OFF	OFF	1200
OFF	OFF	ON	ON	2400
OFF	OFF	ON	OFF	300
OFF	OFF	OFF	ON	150
OFF	OFF	OFF	OFF	110

TRANSMITTER BAUD RATE

SWITCH 2 POSITION				BAUD RATE
8 (7)	6 (5)	4 (3)	2 (1)*	
ON	ON	ON	ON	0
ON	ON	ON	OFF	0
ON	ON	OFF	ON	50
ON	ON	OFF	OFF	75
ON	OFF	ON	ON	134.5
ON	OFF	ON	OFF	200
ON	OFF	OFF	ON	600
ON	OFF	OFF	OFF	2400
OFF	ON	ON	ON	9600
OFF	ON	ON	OFF	4800
OFF	ON	OFF	ON	1800
OFF	ON	OFF	OFF	1200
OFF	OFF	ON	ON	2400
OFF	OFF	ON	OFF	300
OFF	OFF	OFF	ON	150
OFF	OFF	OFF	OFF	110

LTC ENABLE

FUNCTION	POSITION 9 (8)*	POSITION 10 (9)
LTC enabled	ON	OFF
LTC disabled	OFF	ON

*NOTE: Some switches are numbered 0-9 instead of 1-10.

Table 2-2: SW2 Switch Settings

SWITCH SW3

Switch SW3 is used to select the vector address as illustrated in Table 2-3. Figure 2-5 at the end of the section shows the location of the switches on the board. Normally the vector assigned to the PM-DL11W for console device is 60_8.

SWITCH 3 POSITION	ASSOCIATED ADDRESS	SETTING	SAMPLE SETTINGS	
			VECTOR 60	VECTOR 300
1	Not used	Always ON	ON	ON
2	ADD2		ON	ON
3	ADD3		ON	ON
4	ADD4	2 through 7	OFF	ON
5	ADD5	OFF = 1 on Bus	OFF	ON
6	ADD6		ON	OFF
7	ADD7		ON	OFF
8	ADD8	OFF = Ø on Bus	OFF	OFF

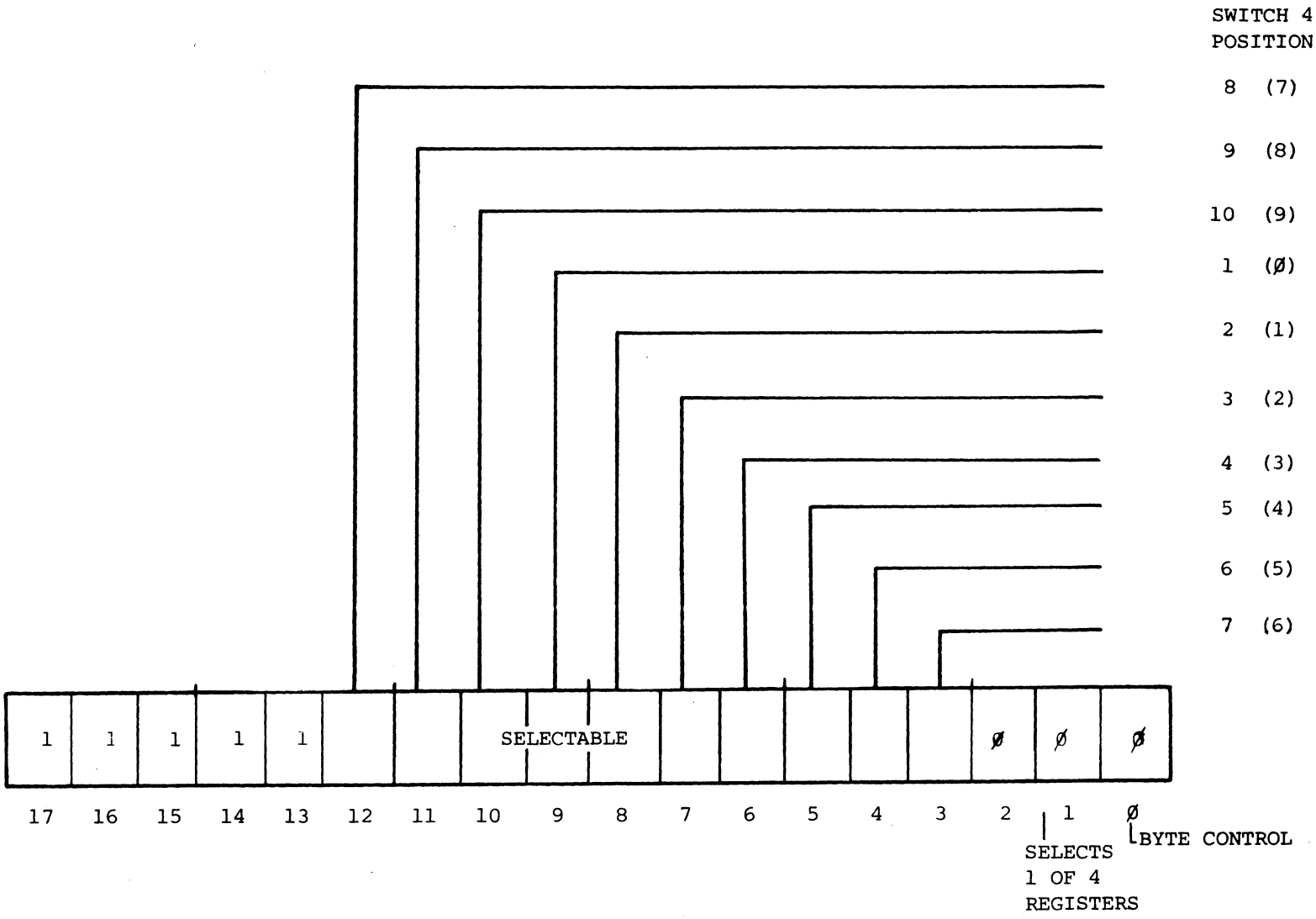
Table 2-3: Vector Address Selection

SWITCH SW4

Switch SW4 is used for address selection. The PM-DL11W card may be addressed in the range of 776000 to 777770. The address format and switch positions are shown in Figure 2-1. Table 2-4 shows sample switch settings.

	SAMPLE SETTINGS		
SW4 POSITION	BUS ADDRESS 177560	BUS ADDRESS 176500	BUS ADDRESS 176510
1	OFF	ON	ON
2	OFF	OFF	OFF
3	ON	ON	ON
4	OFF	OFF	OFF
5	OFF	ON	ON
6	OFF	ON	OFF
7	ON	ON	ON
8	OFF	OFF	OFF
9	OFF	OFF	OFF
10	OFF	OFF	OFF

Table 2-4: SW4 Address Selection



OPEN = 1

*NOTE: SOME SWITCHES ARE NUMBERED 0-9 INSTEAD OF 1-10

Figure 2-1: Address Selection

JUMPER CONFIGURATIONS

Jumpers on the board allow a reader enable for applications such as an ASR 33 teletype reader. Figure 2-2 depicts the jumper configuration for reader enable. Refer also to Figure 2-6 for location of jumpers on the board.

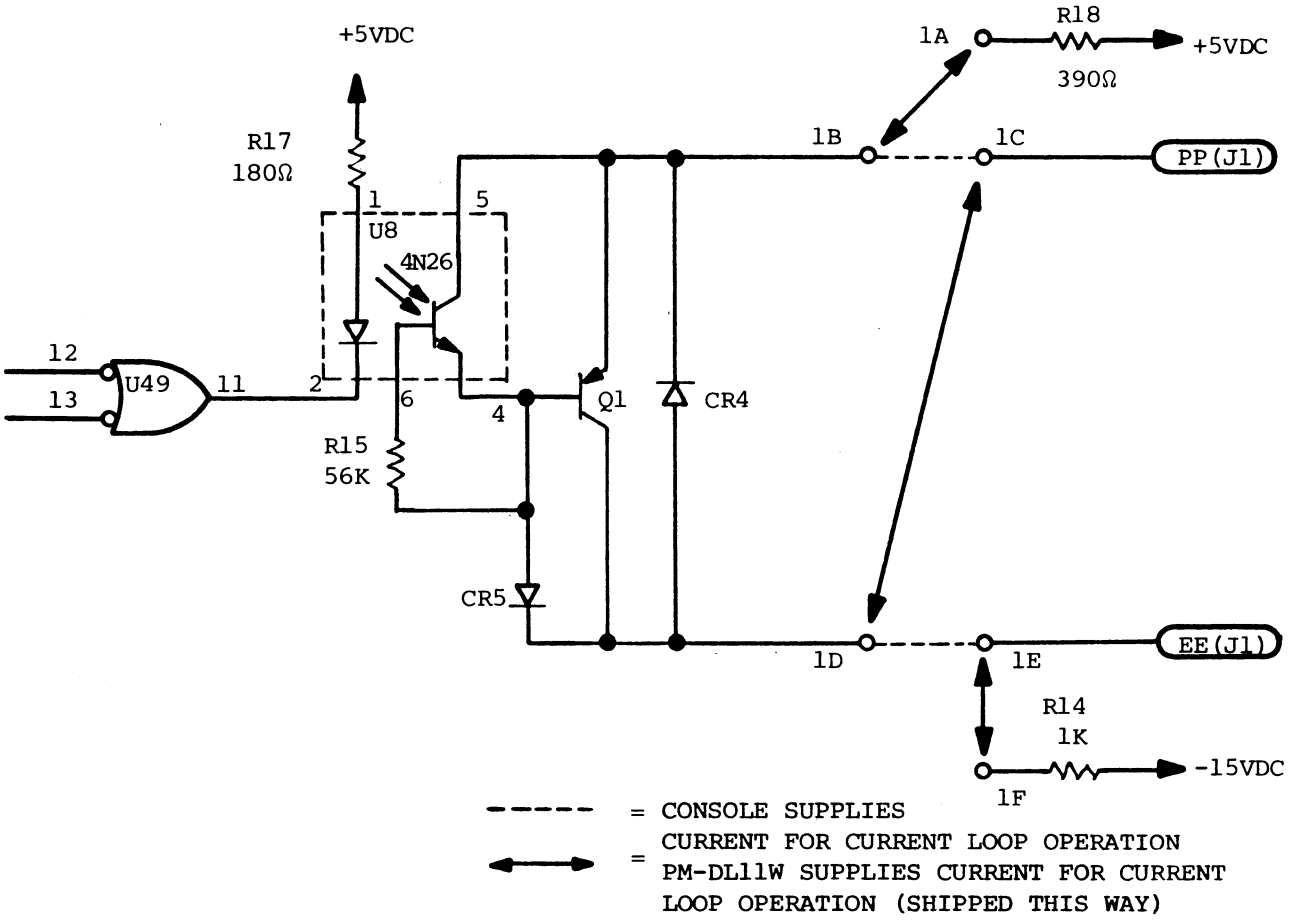


Figure 2-2: Reader Enable Circuit Options
20mA Current Loop

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701320
SCALE	REV A	SHEET 2-8

The PM-DL11WA with 20mA current loop interface can be operated in two modes: active and passive. The PM-DL11W is normally the active source of the 20mA current. However, when operating with two current loops and two processing systems only one device may provide the current; the other device is passive and receives current from the active device.

Figure 2-3 shows the jumper configuration for the receiver; and Figure 2-4 contains the transmitter configuration. Refer also to Figure 2-6 for jumper locations on the board.

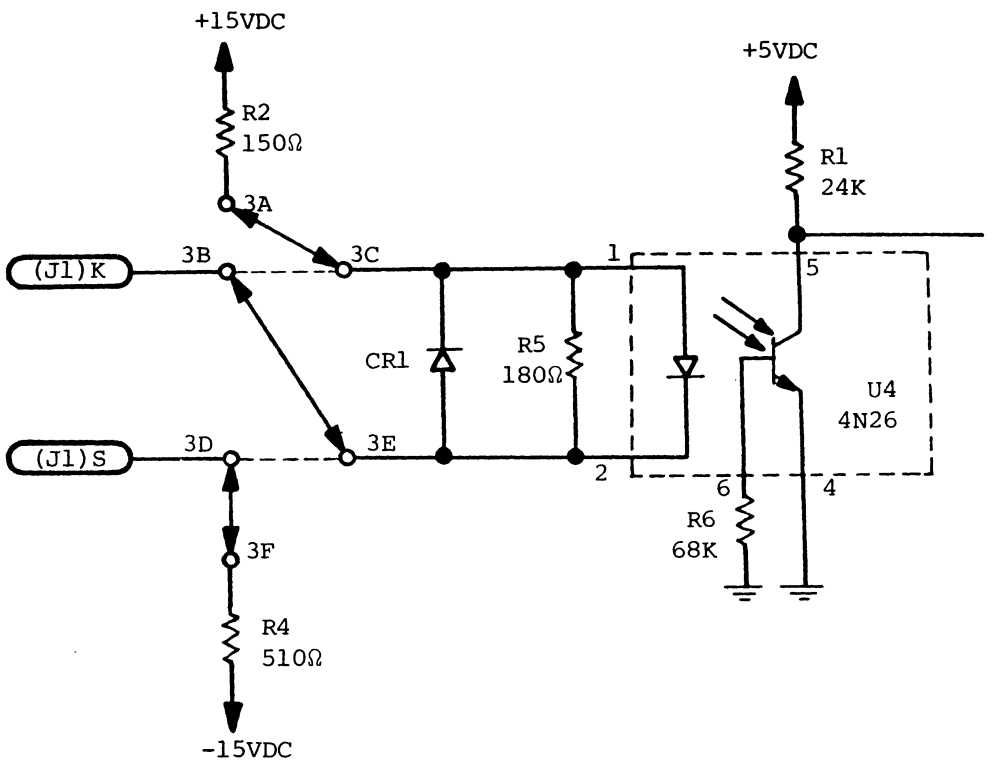


Figure 2-3: Receiver Circuit Options
20mA Current Loop

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701320
SCALE	REV A	SHEET 2-9

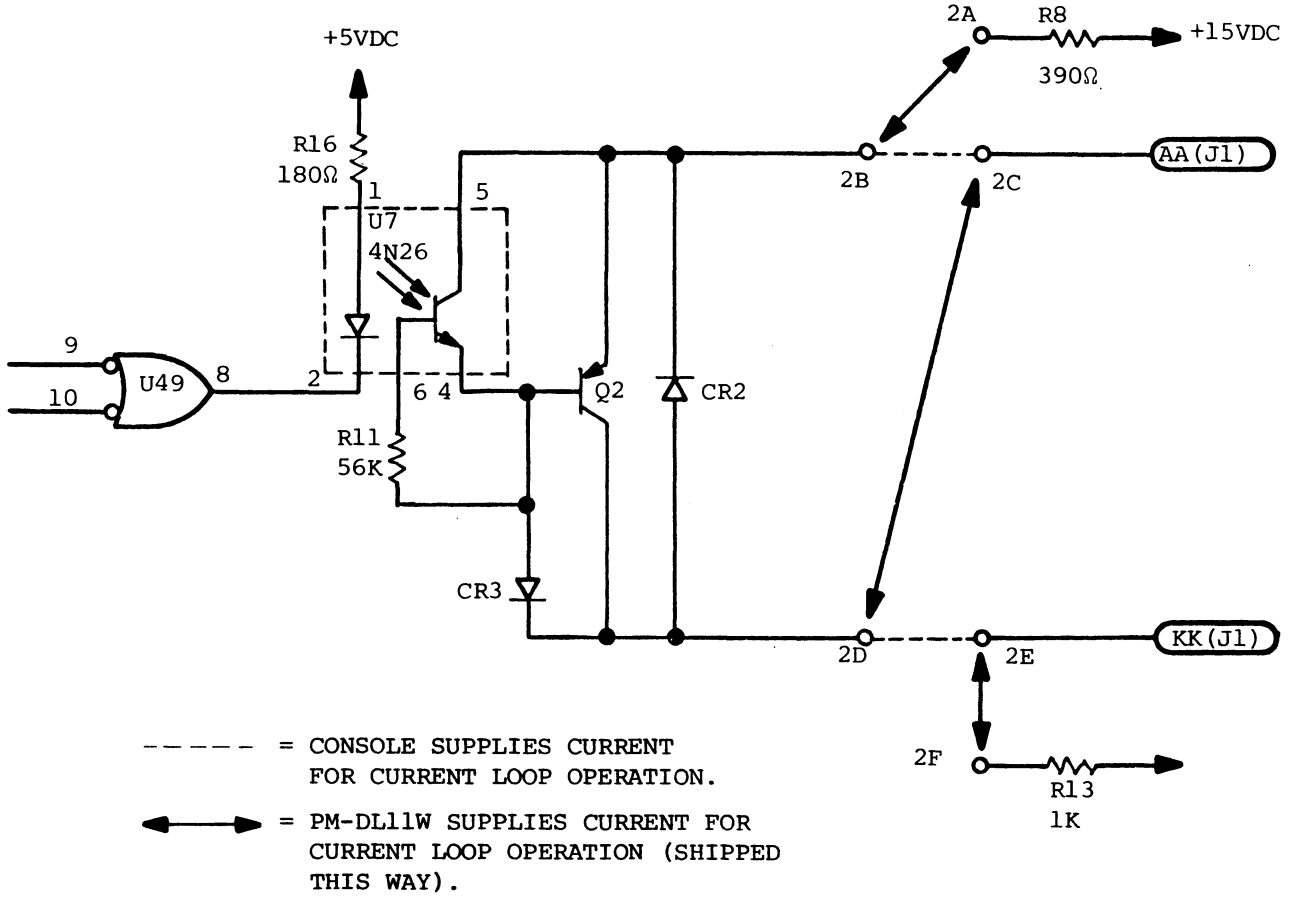


Figure 2-4: Transmitter Circuit Options
20mA Current Loop

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701320
SCALE	REV A	SHEET 2-10

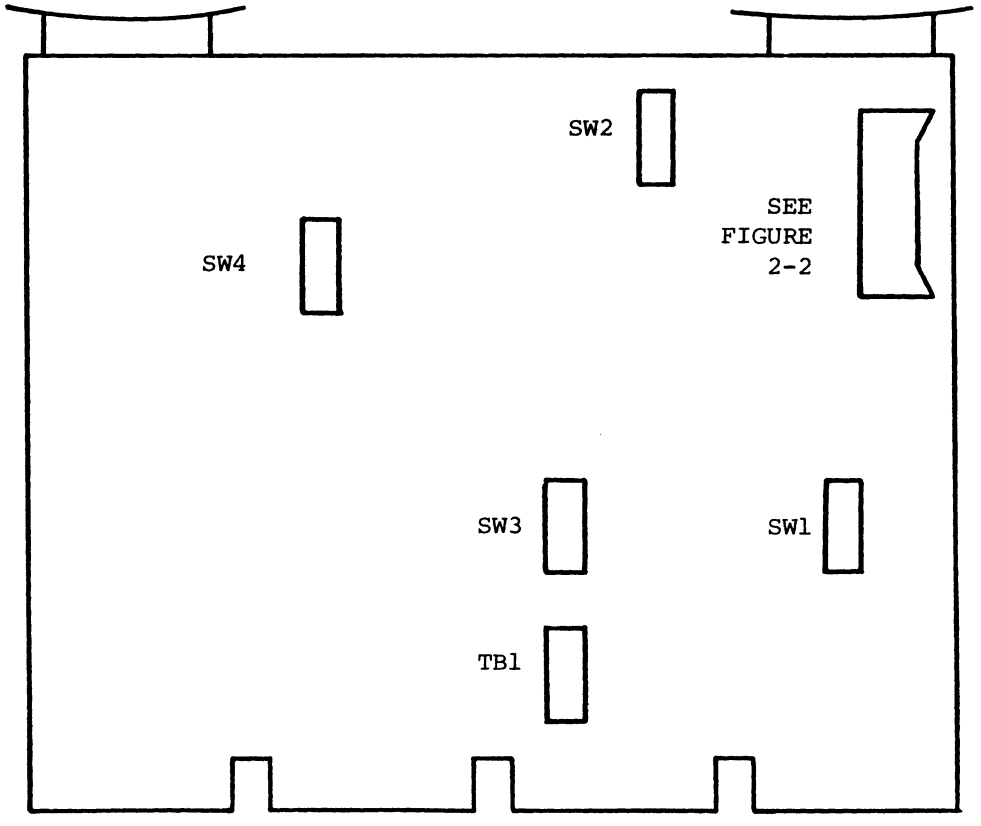


Figure 2-5: PM-DL11W Switch Locations

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701320
SCALE	REV A	SHEET 2-11

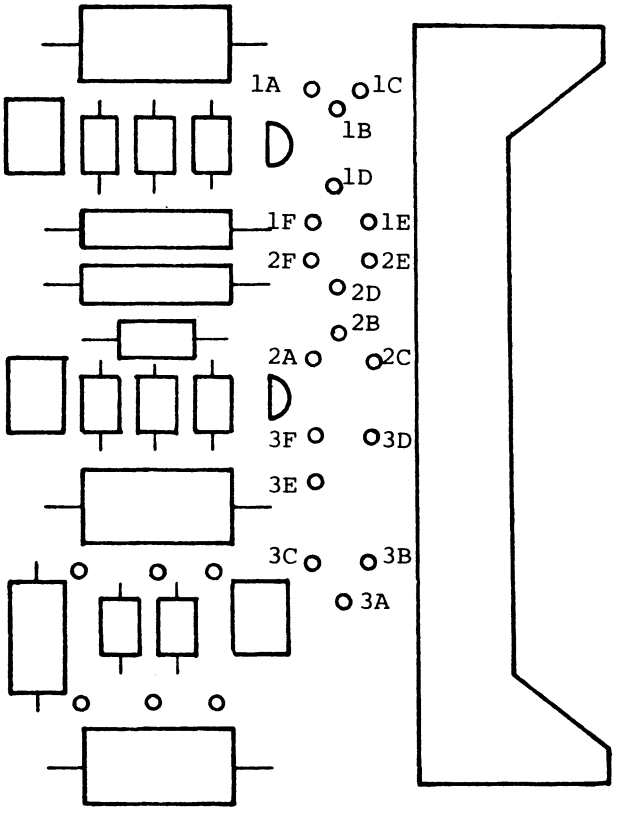


Figure 2-6: PM-DL11W Jumper Connections

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701320
SCALE	REV A	SHEET 2-12

PRIORITY LEVELS

The PM-DL11W also has a 16-pin socket (TB1) for setting priority of the BR level. In general the PM-DL11W should always be set at BR4 and the clock is fixed at BR6. The following jumper chart should be used to set the proper BR level strapping.

	TB1
Level 4 (BR4)	195
Level 5 (BR5)	196
Level 6 (BR6)	197
Level 7 (BR7)	198

Table 2- : Jumper Priority Chart

2.5 EXAMPLE CONFIGURATIONS

Example 1: If the PM-DL11W is interfaced to a terminal such as a TTY that is used as the console device using 110 baud rate, 8 bit characters, no parity, and 20mA current loop, the switch settings are as follows:

•	SW1-1	Off	(Must be on to run PM-DL11W diagnostics)
	-2	—	
	-3	—	
	-4	Off	
	-5	Off	
	-6	Off	
	-7	On	
	-8	Off	(Must be on to run PM-DL11W diagnostics)
•	SW2-1	Off	
	-2	Off	
	-3	Off	
	-4	Off	
	-5	Off	
	-6	Off	
	-7	Off	
	-8	Off	
	-9	On	Enables clock. Used only when no other clock is present.
	-10	Off	

•	SW3-1	—	Vector address 60_8.
	-2	On	
	-3	On	
	-4	Off	
	-5	Off	
	-6	On	
	-7	On	
	-8	Off	
•	SW4-1	Off	Address 777560_8.
	-2	Off	
	-3	On	
	-4	Off	
	-5	Off	
	-6	Off	
	-7	On	
	-8	Off	
	-9	Off	
	-10	Off	

Note that this setting is for a console device.

Where: the Receiver Status Register is 777560
the Receiver Data Buffer Register is 777562
the Transmitter Status Register is 777564
the Transmitter Data Buffer Register is 777566

The Clock Status Register is fixed at 777546.

If additional PM-DL11W units are installed, the address selection must fall into the preassignment space as follows:

1st unit	776XX0	Where: XX = 50 through 67
	XX2	
	XX4	
through	XX6	
16th unit	776670	
	776672	
	776674	
	776676	
Also	77XXX0	Where: XXX = 561 through 617
	77XXX2	
	77XXX4	
	77XXX6	

The PM-DL11W is normally used as the active device and the option jumpers should be installed as shown in Figures 2-2 through 2-6. These jumpers are installed at the factory and normally should not require changes.

Example 2: If the PM-DL11W is to be used as the console device with the DEC VT52AE set up as 300 baud, no parity, 8 bit character, EIA interface, the unit should be set up as follows:

•	SW1-1	Off	(Must be on to run diagnostics)
	-2	—	
	-3	—	
	-4	Off	
	-5	Off	
	-6	On	
	-7	On	
	-8	Off	(Must be on to run diagnostics)
•	SW2-1	Off	
	-2	Off	
	-3	On	
	-4	On	
	-5	Off	
	-6	Off	
	-7	Off	
	-8	Off	
	-9	On	LTC enable
	-10	Off	LTC enable
•	SW3-1	—	Vector address 60_8.
	-2	On	
	-3	On	
	-4	Off	
	-5	Off	
	-6	On	
	-7	On	
	-8	Off	
•	SW4-1	Off	Address 777560 (console device)
	-2	Off	
	-3	On	
	-4	Off	
	-5	Off	
	-6	Off	
	-7	On	
	-8	Off	
	-9	Off	
	-10	Off	

Section 3

Functional Description

This section describes the functional units of the PM-DL11W serial line interface and line time clock.

3.1 SERIAL LINE INTERFACE

Figure 3-1 contains a simplified block diagram of the interface functions of the PM-DL11W. Each functional unit of the interface is described below.

SELECTION LOGIC: The selection logic of the PM-DL11W determines if the interface has been selected and which of five internal registers is selected and whether it is to perform an input or output function.

REGISTERS: The PM-DL11W contains five internal registers which provide data transfer, and control and status information for the interface. They are program addressable and are described in detail later in the section.

INTERRUPT CONTROL LOGIC: Permits the line clock, receiver, or transmitter to request and gain control of the Unibus for a vectored interrupt.

RECEIVER STATUS REGISTER: This register provides status indicators for the receiver logic. Status indicators include the receiver active flag, receiver done flag and the interrupt enable bit which is used to initiate interrupts when the done flag is set.

RECEIVER BUFFER REGISTER: This register which is part of the UART holds the character received from the external device prior to transfer to the Unibus.

TRANSMITTER STATUS REGISTER: This register provides the interrupt enable bit and the transmitter ready flag so that transmitter logic can be monitored and an interrupt intitiated. It also provides a maintenance bit and a break bit which generates a continuous space.

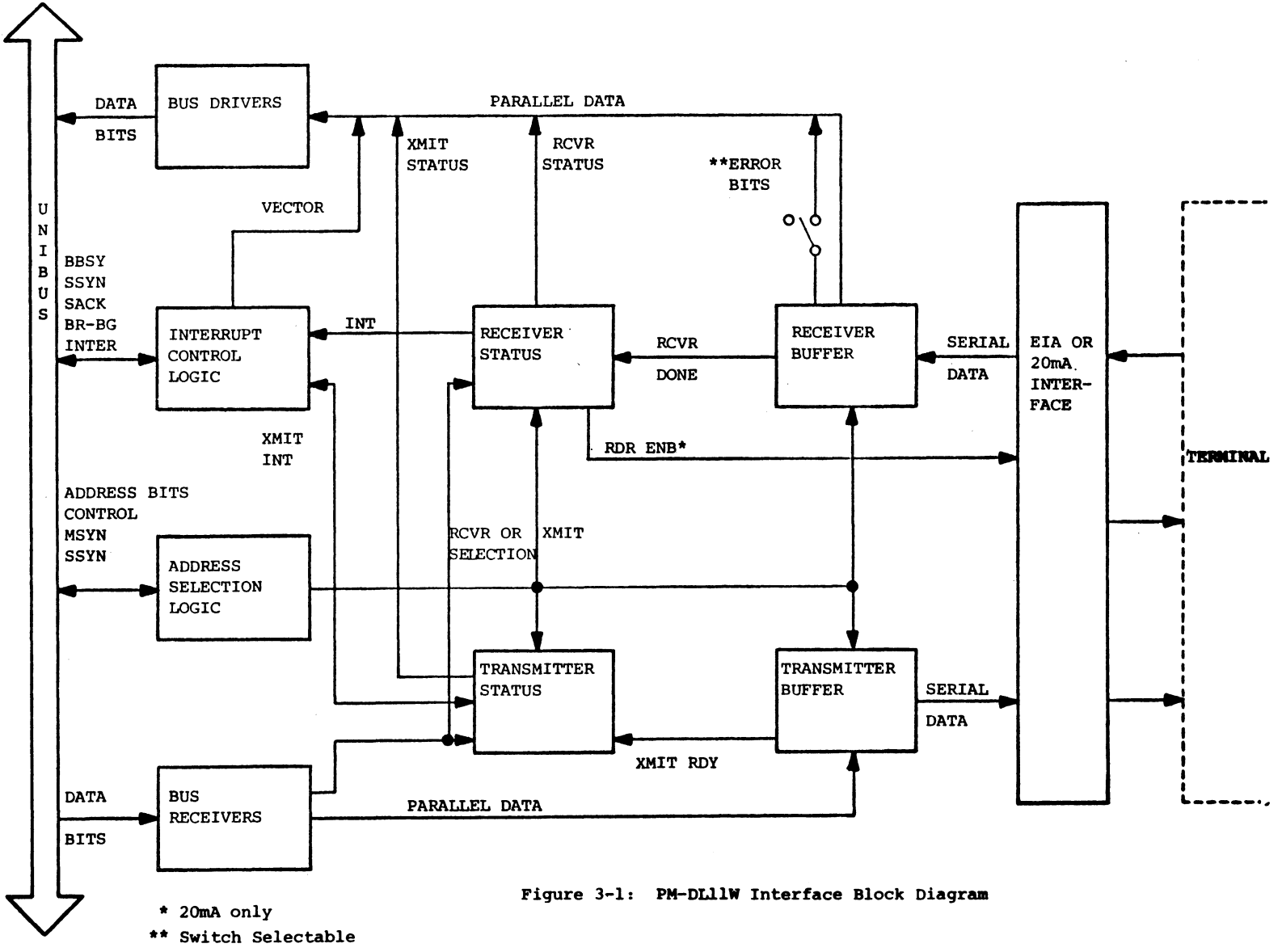


Figure 3-1: PM-DL11W Interface Block Diagram

TRANSMITTER BUFFER REGISTER: This register which is contained in the UART holds the character to be transferred to the external device.

BUS RECEIVERS: Parallel data from the Unibus is received by the bus receivers and then transferred to the appropriate device registers.

BUS DRIVERS: The parallel data from the registers, UART, or vector is gated onto the Unibus by the bus drivers.

3.2 LINE TIME CLOCK

A 50 or 60 cycle AC input generated by the power supply is monitored by the PM-DL11W line time clock circuit. This signal, designated LTC, generates an interrupt each 16 2/3ms for 60 cycle current and each 20ms for 50 cycle current. The program can enable or disable LTC interrupts by setting the LTC INT ENB bit of the clock status register word.

Figure 3-2 shows a simplified block diagram of the line time clock. The line time clock status register provides the interrupt enable bit and the line clock monitor bit to allow program monitoring of the line clock signal or timed interrupt sequences to be initiated as desired. The other functional units in the diagram are identical to those described for the serial interface.

3.3 INTERRUPTS

The PM-DL11W has two interrupt channels, one for the receiver and transmitter section, and one for the line time clock. The receiver and transmitter section may be strapped to operate on BUS REQUEST 4-7 (BR4-BR7) priority levels. The line time clock is fixed at BUS REQUEST 6 (BR6) priority level.

The PM-DL11W can be used as a console interface card by selecting vector address 60_8 and 64_8. If the unit is used as a communications interface other than a console interface, the vector addresses are assigned in the range of 300_8 to 777_8. Vector addresses are selected using a switch. The vector interrupt for the line time clock is 100.

3.4 DATA FORMAT

Figure 3-3 depicts the format of the eleven bit data word. The data word consists of a start bit, five to eight data bits, a parity bit, and one, one and a half, or two stop bits.

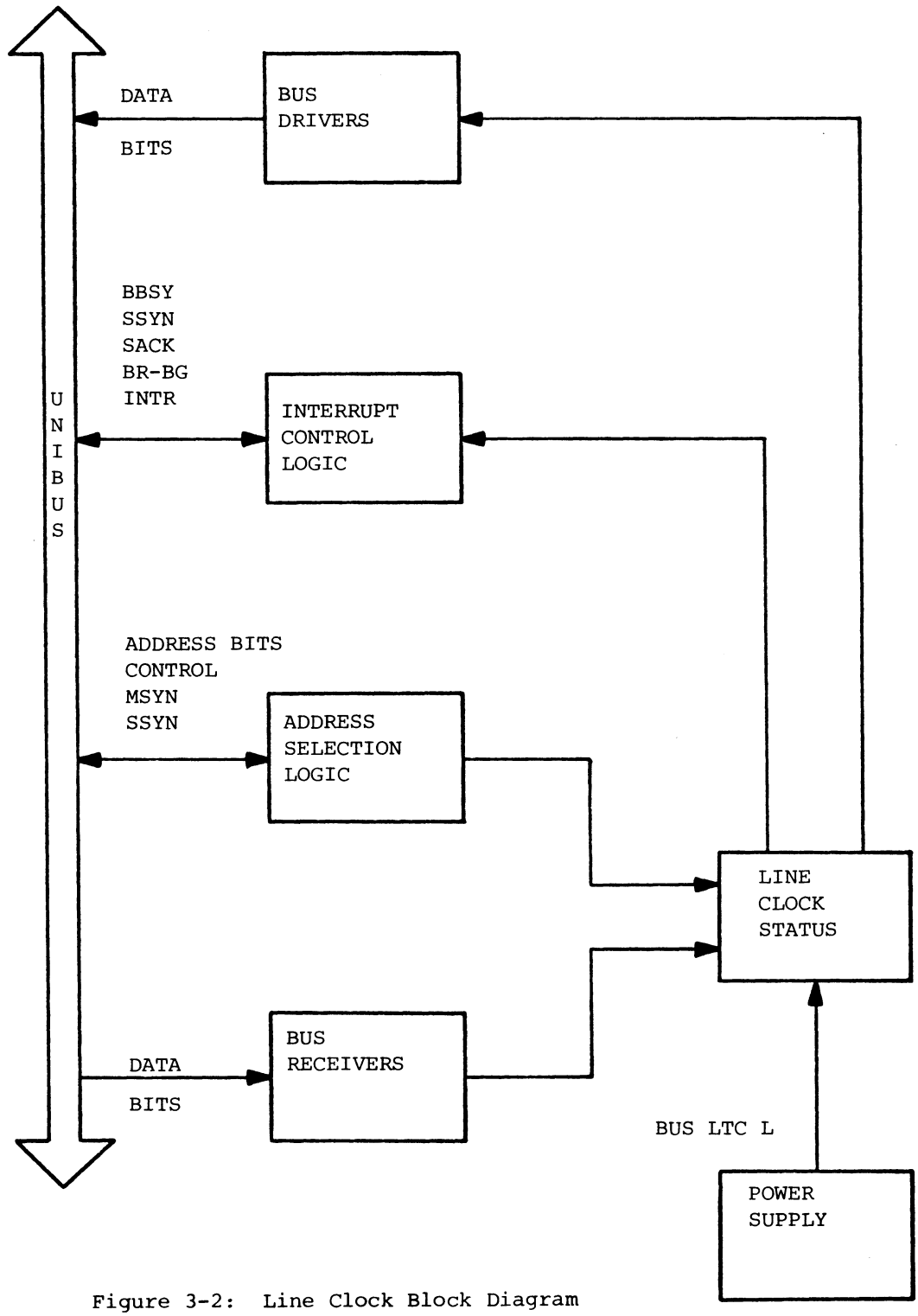


Figure 3-2: Line Clock Block Diagram

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701320
SCALE	REV A	SHEET 3-4

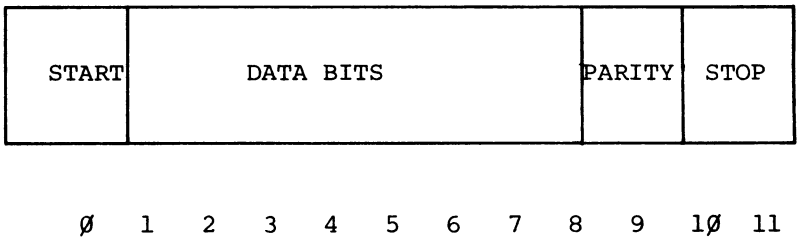


Figure 3-3: Data Word Format

Each field of the data word is described in the following:

BIT		DESCRIPTION
Ø	START	Indicates to the interface receiver logic that serial data is ready to be loaded into the reader buffer register.
1-8	DATA BITS	From five to eight data bits may be used. When fewer than eight bits are used, they are left adjusted to the lowest significant bit position.
9	PARITY	When set, the parity bit enables parity checking functions.
1Ø-11	STOP	Stop bits indicate the end of the data word. One, one and one half or two stop bits may be selected.

3.5 DEVICE REGISTERS

Software control of the PM-DL11W is accomplished via device registers. The registers and corresponding addresses are:

Receiver Status Register	76XXXØ
Receiver Data Buffer	76XXX2
Transmitter Status Register	76XXX4
Transmitter Data Buffer	76XXX6

Each of the registers is described below.

3.5.1 RECEIVER STATUS REGISTER

This register contains status indicators for the PM-DL11W receiver logic. The format of the receiver status register bit assignments is shown in Figure 3-4.

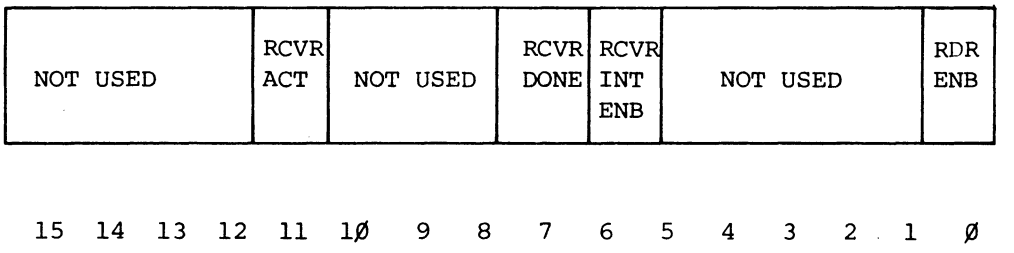


Figure 3-4: Receiver Status Register Bit Format

BIT		DESCRIPTION
0	READER ENABLE	Write only. This bit advances the paper tape reader of an ASR teletype (20mA current loop) and clears bit 7. Reader enable is cleared when a valid start bit is detected or by the INIT signal. Setting this bit clears bit 7.
1-5	NOT USED	
6	RECEIVER INTERRUPT ENABLE	Read/Write. Alows an interrupt when bit 7 is also set. Bit 6 is cleared by the INIT signal.
7	RECEIVER DONE	Read only. Bit 7 is set when data is ready for transfer to the Unibus. If bit 6 is set, receiver done causes an interrupt. It can be cleared by setting bit 0, referencing the Receiver Data Buffer, or by the INIT signal.

8-1Ø	NOT USED	
11	RECEIVER ACTIVE	Read only. When set, this bit indicates that the receiver is busy. It is set when a start bit is detected. It is cleared at the leading edge of the receiver done signal or by the INIT signal.

3.5.2 RECEIVER DATA BUFFER

The receiver data buffer holds the data character received from an external device prior to transfer to the Unibus. It also contains four read only error indicator bits as described below.

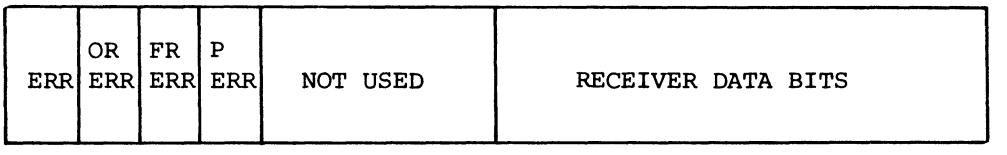


Figure 3-5: Receiver Data Buffer Bit Format

BIT		DESCRIPTION
Ø-7	RECEIVED DATA BITS	Read only. These bits contain the data from the external device.
8-1Ø	NOT USED	
12	RECEIVE PARITY ERROR	Read only. This bit is set when a parity error is detected. If the non-parity option is selected, this bit is always zero.
13	FRAMING ERROR	Read only. This bit is set if the word read does not contain a valid stop bit. It is also used to detect a break in transmission or a break caused by pressing the BREAK character on the keyboard.

14	OVERRUN	Read only. This bit is set if the RCVR DONE bit (bit 7 of the Receiver Status Register word) is not reset before the following character is read.
15	ERROR	Read only. This bit indicates whether any of the above errors have been detected. It is set if bits 12, 13, or 14 are set.

NOTE: Error bits 12-15 may be disabled via a switch on the card.

3.5.3 TRANSMITTER STATUS REGISTER

The transmitter status register provides status indicators for the transmitter logic. It also contains a maintenance bit which can be set by a program to facilitate maintenance and a BREAK bit which if enabled (SW1) generates a continuous space.

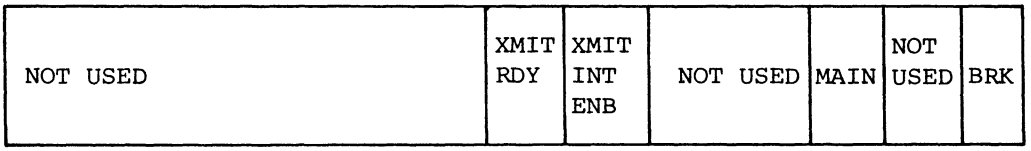


Figure 3-6: Transmitter Status Register Bit Format

BIT		DESCRIPTION
Ø	BREAK	Read/Write. When set, this bit transmits a continuous space. It is cleared by the INIT signal. This bit may be disabled by a switch on the card.
1	NOT USED	
2	MAINTENANCE	Read/Write. When set, this bit disables the serial line input to the receiver and connects it to the serial output of the transmitter causing the PM-DL11W to be bypassed for maintenance purposes. Bit 2 is cleared by the INIT signal.

3-5	NOT USED	
6	TRANSMITTER INTERRUPT ENABLE	Read/Write. This bit allows an interrupt sequence for the transmitter if bit 7 is also set. It is cleared by the INIT signal.
7	TRANSMITTER READY	Read only. This bit sets when the Transmitter Data Buffer is ready to accept another word (INIT is generated). It is cleared when the Transmitter Data Buffer is loaded. When set, it initiates an interrupt if bit 6 is also set.

3.5.4 TRANSMITTER DATA BUFFER

This register holds the data prior to its transmission to an external device. The format of the data depends upon the switch settings on the PM-DL11W board. Figure 3-7 shows the bit format for seven bits of data.

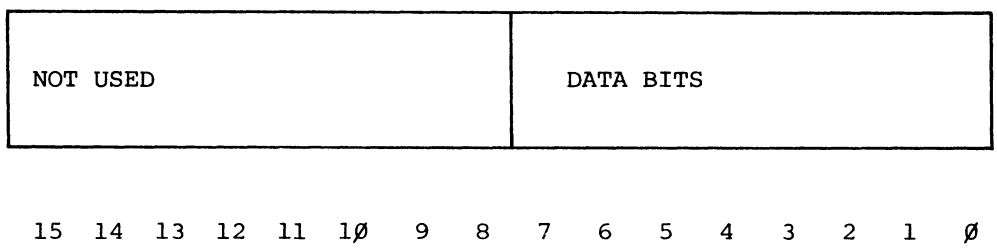


Figure 3-7: Transmitter Data Buffer Bit Format

BIT		DESCRIPTION
Ø-7	DATA BITS	Write only. This field contains the data bits which are ready for transmission to an external device.
8-15	NOT USED	

3.5.5 CLOCK STATUS REGISTER

The clock status register contains the interrupt enable bit and the line clock monitor bit which allows program monitoring of the line clock signal and initiation of timed interrupts. Figure 3-8 shows the bit format for the clock status register word.

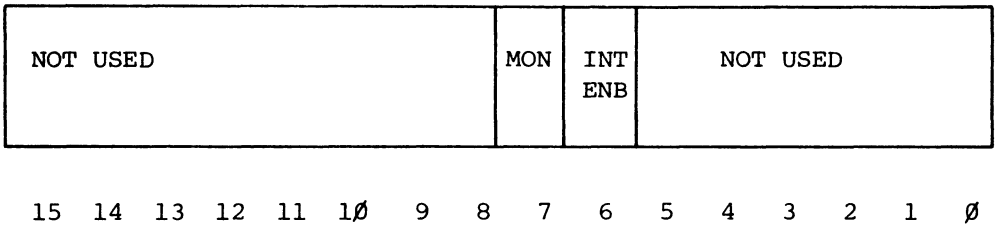


Figure 3-8: Clock Status Register Bit Format

BIT		DESCRIPTION
Ø-5	NOT USED	
6	INTERRUPT ENABLE	Read/Write. When set, this bit allows an interrupt if bit 7 is also set.
7	MONITOR	Read/Clear. This bit is set by the line frequency clock signal LTC. It can be cleared by the programmer and is reset by the INIT signal.

3.6 PDP-11/20 MOD - MICRO 1 MOD

During operation in most PDP-11 computers when an CPR occurs right after an interrupt has been requested, the NPR will block the bus grant to the interrupting device. When this happens the CPU waits a short time for the interrupting device to respond. When no response happens, the CPU cancels the interrupt grant and services the NPR. In a PDP-11/20 or a Micro 1 (LSI-11 based system) when an interrupt is started it must be finished. If no response is given to the bus grant, the CPU will time out and trap.

The -101 version of the DL11W takes care of this problem. The etch between W1 and W2 on the solder side of the board must be cut.

Section 4

Maintenance and Troubleshooting

This section contains maintenance and troubleshooting information. The drawings in the appendix are provided for further reference.

4.1 PRINTED CIRCUIT BOARD CLEANING

The printed circuit contacts should be cleaned when dust or dirt has built-up on the surfaces. Instant Contact Cleaner, alcohol, and freon have been approved for cleaning contacts. When printed circuit contacts must be cleaned, hold the card so the contacts are pointed down and thoroughly saturate the contact area. While the contacts are still wet, scrub with a soft natural bristle brush.

CAUTION

Under no circumstances should
an eraser or other abrasive be
used on gold plated contacts.

To remove dust from printed circuit boards, a soft brush should be used. Clear, oil-free, pressurized air (5 psi max) can be sprayed over the board.

4.2 TROUBLESHOOTING

In the case of an apparent malfunction, do the following:

1. Reset each switch to be sure that it is properly seated.

2. Make sure that the strapping plug is installed and oriented properly (See Section 2).

3. Make sure that the I/O cable is installed correctly and check it for any broken wires.

If the malfunction persists, it is recommended that the board be returned to the factory for repair.

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