SC12/C

(RK06/RK07 COMPATIBLE)

DISK CONTROLLER

TECHNICAL MANUAL

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INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC12/C Disk Controller. In addition, this manual provides diagnostics and application information.

1.2 OVERVIEW

1.2.1 General Description

The SC12/C Disk Controller is a one board imbedded controller for PDP-11 computers manufactured by Digital Equipment Corporation. This controller can be used to interface any large disk having a Storage Module Drive (SMD) interface. The SC12/C controller emulates the RK611 disk controller manufactured by Digital Equipment Corporation for use with RK06 and RK07 disk drives.

1.2.2 SC12/C Emulation of RK06 and RK07

The RK611 provides a convenient controller architecture for a wide variety of modern technology type disks. It is supported by all DEC operating systems and is easy to program.

The SC12/C controller can handle two disk drives of the same or different sizes. The controller configures each drive from the information in a configuration PROM. This technique permits up to 64 different switch selectable combinations of disk drive configurations on the two controller ports.

1.3 FEATURES

1.3.1 Microprocessor Design

The SC12/C design incorporates a unique 8-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various sizes.

1.3.2 Packaging

The SC12/C is constructed on a single, quad-size, multi-layer PC board which plugs directly into the CPU chassis or an expansion chassis. No cabling is required between the computer and the disk controller. The controller obtains its power from the chassis in which it is mounted.

1.3.3 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk data logic. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is operational. If the controller fails the self-test, it leaves the LED on and the controller cannot be addressed from the CPU.

1.3.4 Buffering

The controller contains a 1K x 8 high-speed RAM buffer. It is used to store the device registers of the controller plus a full 512 byte data sector. This buffering permits multiple sector reads with a 3-to-1 sector interlace format. Buffer operations eliminate the possibility of a data late condition and permits the controller to be operated at low bus priorities.

1.3.5 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) capable of correcting single error bursts of up to 11 bits in length and detecting bursts of longer length. The controller determines the location of the error and the pattern so that the software may correct the data after it is transferred to memory. A 32-bit CRC is employed with the header of every sector.

1.3.6 Option and Configuration Switches

DIP switches are used to configure the controller for various disk sizes, Unibus addresses and options. It is possible to select one of 64 possible combinations of disk characteristics for the two drives which can be handled by the controller, inculuding mixtures of disk sizes and drive type codes.

1.3.7 Dual-Port Capability

The SC12/C controller does not support programmable dual port capability. Those disk drives that have dual-port hardware may be used in a dual-port configuration if the port select switch is in the Channel I only or Channel II only position. The middle (programmable) position creates errors if two controllers access the drive at the same time.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Media Compatibility

In all cases, the headers written on the drives are not standard RK06/RK07 headers. In addition a 3-to-1 sector interleave is generated by the hardware formatter. Packs may be formatted using software commands, or by utilizing the hardware formatting capability of the extended command set. Disk packs formatted with an SC12/C controller are media compatible with Emulex SC02/C controllers but not with RK06/RK07 packs.

1.4.2 Disk Mapping

Depending upon the type and size of the disk drive, one to eight logical units may be mapped on it. Various mapping organizations are used; most of which do not leave direct 1:1 correlation between the logical and physical addresses.

1.4.3 Diagnostics

The controller executes the following standard DEC RK06 diagnostics:

ZR6K - RK06 Functional Controller*
ZR6L - RK06 Formatter*
ZR6M - RK611/06 Subsystem Verify*
ZR6N - RK611/06 Subsystem Verify*
ZR6P - RK611/06 Performance Exerciser
ZR6A - RK611 Diskless, Part 1*

The diagnostics marked with an asterisk require certain patches to correct coding problems or bypass unsupported maintenance functions.

1.4.4 Operating Systems

The SC21/C controllers are compatible with DEC operating systems without modifications.

Table 1-1
RK611/RK06/RK07 Disk Subsystem Characteristics

	Specifications	
Characteristics	RK06	RK07
Platters/Drive	2	2
MBytes/Logical Unit	13.8	27.4
Blocks/Drive	27,126	53,790
Tracks/Cylinder	3	3
Cylinders/Drive	411	815
Sectors/Track	22	22
Data Bytes/Sector	512	512
Drives/Controller, Max	8	8
Speed,RPM	2400	2400
Bit Density, (BPI)	4040	4040
Data Rate, (KBYTES/SEC)	204.8	204.8

TABLE 1-2
General Specification

Functional	
Emulation	DEC RK06 and RK07
Media Format	3-to-1 sector interlace
Drive Interface	SMD
Drive Ports	2
Error Control	32-bit ECC for data and 32-bit CRC for headers. Correction of single data error burst of up to 11 bits.
Sector Size	256 words (512 bytes)
Sectors/Track	Selectable for each physical drive
Tracks/Cylinder	Selectable for each physical drive
Cylinders/Drive	Selectable for each physical drive
Drive Type Code	Selectable RK06 or RK07 for each physical drive
Computer Interface	Unibus
Vector Address	210 Standard, 150 Optional
Priority Level	Level 5
Data Bufferring	1 Sector (256 words)
Data Transfer	High speed DMA operation
Self-Test	Extensive internal self-test on powering up

TABLE 1-2 (Cont.)
General Specification

Functional	
Indicator	Activity/Error/Status LED
Unibus Addresses	Standard: 777440-777476 Alternate: 776700-776736
Design	High-speed bipolar microprocessor using 2901 bit-slice components
Physical	
Packaging	One Quad-sized board
Mounting	Any SPC slot in CPU or expansion box
Connectors	One 60-pin A cable flat connector and two 26-pin B cable connectors. (Flat cable type.)
Electrical	
Unibus Interface	DEC approved line drivers and receivers
Drive Interface	Differential line drivers and receivers. A cable accumulative length to 35 feet. B cable length to 25 feet.
Power	+5V, 5%, 5 Amp. max.

2.1 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC12/C controller is shown in Figure 2-1. The controller is organized around a 8-bit high-speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with two 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 1K words is implemented with twelve 1K x 4 PROM's.

The controller incorporates a 1K x 8 high-speed RAM buffer which is used to store the controller's device registers and one sector (512 bytes) of data buffering.

The A Cable Register (ACR) provides the storage of all A cable signals going to the disk drives. The inputs from the selected drive are testable by the microprocessor.

Serial data from the drive is converted into 8-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data access from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC Shift Register is used to generate and check the ECC for the data field. The same register is also used in a 32-bit CRC mode for the headers. The actual ECC polynomial operation is done independent of the microprocessor, but the determination of the error position and error pattern is done under the control of the microprocessor.

The Unibus interface consists of 18 address lines and 16 bi-directional data lines. The Unibus also carries interrupt vector address data, data control signals, and control signals for granting and receiving bus matership. The Unibus interface is used for programmed I/O, CPU interrupts, and data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all DMA operations and transfers data between the Unibus data lines and the buffer.

2.2 PHYSICAL DESCRIPTION

The SC12/C controller consists of a single quad-size board which plugs directly into a PDP-11 chassis.

2.2.1 Connectors

2.2.1.1 A Cable Connector

The 60-pin flat cable connector labeled J3 at the top edge of the board is for the A cable which daisy-chains to all the drives for control and status. Pin 1 is located on the left side of the connector.

2.2.1.2 B Cable Connector

The two 26-pin flat cable connectors labeled J1 and J2 are for the radial B cables to each of two physical drives which may be attached to the controller. Pin 1 is located on the left side of the connector. The two B cable ports are all identical and any drive may be plugged into any connector.

2.2.1.3 Test Connectors

Connectors J4 and J5 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.2 Switches

There are three sets of switches labled SW1-SW3. SW1 is a four pole DIP 'piano-type' switch accessible from the PC board edge. Locating SW1 such that it is accessible to the operator while the controller is imbedded in a LSI type chassis, makes the selection of common options such as hardware format simpler to perform.

The other two sets of switches SW2 and SW3 provide controller address decoding selection, option selection and drive configuration selection. (See Appendix A for a complete description of the switch functions.)

2.2.3 LED Indicator

There is an LED indicator mounted between the connectors at the top of the board. The controller executes an extensive self-test when powering up. The microprogrammed organization of the controller permits most logic other than the interface circuitry to the disk to be validated before the controller becomes ready. The LED lamp is turned on as the controller starts its self-test and is turned off only when the controller successfully completes the test. If a malfunction is detected by the built-in diagnostics, the LED remains on and the controller will not respond to program I/O. The LED blinks at approximately a one second rate if the self-test is successful but no drive is seen on-line. The LED also functions as an activity indicator during read and write operations.

2.2.4 Firmware PROM's

There are twelve PROM sockets, used for the control memory, located along the left edge of the board. The sockets are labeled ROM 0 through ROM 11 in a discontinuous physical order. The numbers on the top of the PROM ICs are Emulex part numbers, which identify the unique pattern of the PROM. When inserting PROMs in the board, the ID numbers are placed in the same sequence as the PROM numbers on the board beside each socket.

2.3 INTERFACES

2.3.1 Disk Interface

The controllers's disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD interface and is compatable with these drives electrically and in timing.

The following defines the electrical interface and the recommended cables.

2.3.1.1 A Cable

The 60-conductor A cable is daisy-chained to all drives and terminated at the last drive. The signals in this cable are listed in Table 2-1 along with their function when the control tag (Tag 3) is asserted. The A cable should be 30 twisted pair flat cable with an impedance of 100 ohms and an accumulative length of no greater than 35 feet.

Spectra-Strip P/N 455-248-60 flat cable or its equivalent is recommended. It is possible to order A-Cable assemblies from Emulex that are made up in one of four lengths:

EMULEX P/N	LENGTH (FT.)
SU1111201	8.0
SU1111203	15.0
SU1111205	25.0
SU1111207	35.0

2.3.1.2 B Cable

The 26-conductor B cable is radial to all drives and contains the data and clock signals. The signals and grounds in this cable are listed in Table 2-1. The B cable should be 26 conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length must not be greater than 25 feet.

3M-P/N 3476/26 flat cable or its equivalent is recommended. It is possible to order B-cable assemblies from Emulex that are made up in one of four lengths:

EMULEX P/N	LENGTH (FT.)
SU1111202	8.0
SU1111204	15.0
SU1111206	25.0

2.3.2 Unibus Interface

The controller interfaces to the PDP-11 or VAX11-780 Unibus via a Small Peripheral Controller (SPC) connector. The Unibus consists of 18 address lines and 16 bi-directional data lines, plus control signals for data and interrupt vector address transfer and for becomming bus master. The signal connections of the controller to the Unibus are shown in Table 2-2.

2.3.2.1 BR (Interrupt) Priority Level

The controller is hardwired for BR5. The other three Bus Grant signals are jumpered through.

2.3.2.2 Register Address

The register address and the number of registers assigned to the controller are decoded by a PROM at U104. The selections available are determined by configuration switch SW1 as discussed in Appendix A.

2.3.2.3 DCLO and INIT Signals

The DCLO and INIT signals both perform a controller clear. The self-test is performed only if DCLO has been asserted.

2.4 DISK FORMAT

2.4.1 Disk Organization

The formatting of a disk and the mapping of one or more logical drives onto a physical drive varies with the drive size. Some of this information is supplied by the configuration PROM. The rest is computed based upon configuration PROM information. In all cases, the headers actually written on the drives are not standard RK06/RK07 headers. In addition, a 3-to-1 sector interleave is generated by the hardware formatter. Disk packs formatted with an SC12/C controller are media compatible with Emulex SC02/C controllers but not with RK06/RK07 packs.

Table 2-1
Disk Drive Connections

Pins Lo/Hi	Signal	(Tag 3 Function)	From/To
A Cable:			
22,52	Unit Select Tag		To
23,53	Unit Select bit 0		To
24,54	Unit Select bit 1		To
26,56	Unit Select bit 2		To
27,57	Unit Select bit 3		To
4,34	Bit 0	(Write Gate)	To
5,35	Bit 1	(Read Gate)	To
6,36	Bit 2	(Servo Offset Plus)	To
7,37	Bit 3	(Servo Offset Minus)	To
8,38	Bit 4	(Fault Clear)	To
9,39	Bit 5	(AM Enable)	To
10,40	Bit 6	(Return to Zero)	To
11,41	Bit 7	(Data Strobe Early)	To
12,42	Bit 8	(Data Strobe Late)	To
13,43	Bit 9	(Release)	To
30,60	Bit 10		To
14,44	Open Cable Detect		To
15,45	Fault		From
16,46	Seek Error		From
17,47	On Cylinder		From
18,48	Index		From
19,49	Unit Ready		From
20,50	Not Used		From
21,51	Busy (dual-port only)		From
25,55	Sector		From
28,58	Write Protected		From
29	Power Sequence Hold		To
59	Power Sequence Pick		To
B Cable:			
8,20	Write Data		To
6,16	Write Clock		To
2,14	Servo Clock		From
3,16	Read Data		From
5,17	Read Clock		From
10,23	Not Used		From
22,9	Unit Selected		From
12,24	Not Used		From
13,26	Not Used		From

Table 2-2
SPC Unibus Connections

Column	C		D		E		F	
Pin	1	2	1	2	1	2	1	2
A	NPGIN	+5V		+5V		+5V		+5V
B	NPGOUT					-15V		-15V
C	PA	GND		GND	A12	GND		GND
D		D15		BR7	A17	A15	BBSY	
E		D14		BR6	MSYN	A16		
F		D13		BR5	A02	C1		
H	D11	D12		BR4	A01	A00		
J		D10			SSYN	C0	NPR	
K		D09		BG7IN	A14	A13		
L		D08	INIT	BG7OUT	A11			
M		D07		BG6IN			INTR	
N	DCLO	D04		BG6OUT	A08			
P		D05		BG5IN	A10	A07		
R		D01		BG5OUT	A09			
S	PB	D00		BG4IN				
T	GND	D03	GND	BG4OUT	GND		GND	SACK
U		D02			A06	A04		
V	ACLO	D06			A05	A03		

2.4.2 Mapping

Depending upon the type and size of the disk drive, one to eight logical units may be mapped on it. The controller can handle a maximum of eight logical units distributed across a maximum of two physical disk drives. A logical drive may not be mapped across a physical unit boundary.

The controller firmware multiplies the logical address out to obtain a block address which is then divided by the physical drive configuration constants to provide an address for the physical drive. For this reason a 1:1 correspondence between logical and physical addresses will most likely not exist.

2.4.3 Sector Format

Each sector contains a detached two-word header and a 256 word data field. The header field is terminated with a two vertical check characters and the data field is terminated with a 32-bit ECC. The controller attempts corrections only on the data field, never on the header. Each field is preceeded by at least 11 bytes of zero's and an 8-bit SYNC byte. The second header check character is not visable to the software which allows the header to be compatible with existing RK06/RK07 software.

In detail, each sector is organized as follows:

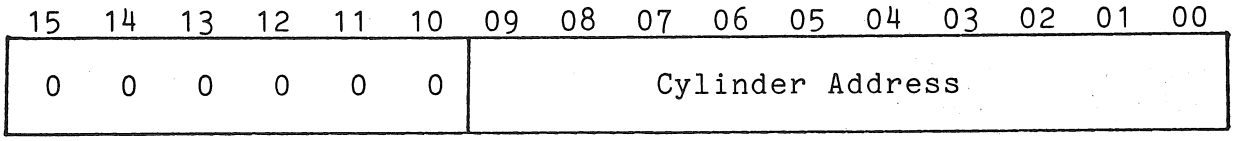
----------Sector Length 610 Bytes----------

Preamble	Sync	Header	CRC	Preamble	Sync	Data Field	ECC	Recovery
--27(17)*--		----8----		-----16------		---512----	-4-	--8(2)*--

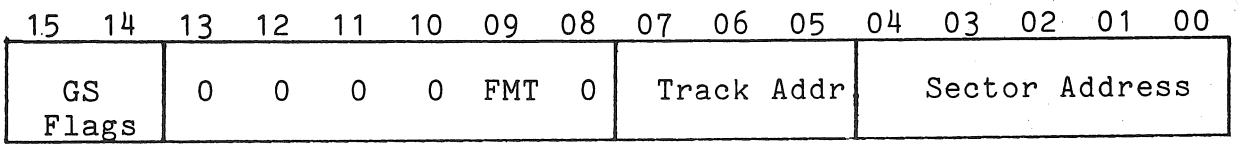
*When different than removable media format configuration, numbers for fixed media format configuration are shown in parenthesis.

Figure 2-1
Sector Format

Header Word 1:



Header Word 2:



Header Word 3:

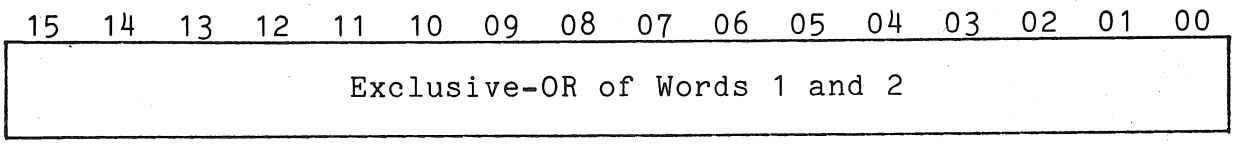


Figure 2-2
Header Format

2.4.3.1 Header Field

The header preamble is used to synchronize the Phase Locked Oscillator (PLO) in the drive to the data on the pack. The SYNC byte is used by the controller to synchronize to the data bytes and their boundaries, and by the drive to synchronize to the phase of the data stream. The two header data words are organized as follows:

Word #1 - Logical cylinder address, right justified.

Word #2 - Logical track and sector addresses, in low byte, sector in bits 4-0, track in bits 7-5. Flags in high byte, bits 15 and 14 are good sector flags, bit 9 is the 20 sector format flag, and bits 13, 12, and 10 are used to flag a replaced track.

To insure compatibility with RK611 controller software, only one of the check character bytes, which are identical, is available to the user. The other is written and checked entirely under firmware control to add to header integrity.

2.4.3.2 Data Field

The data field preamble and SYNC bytes have the same functions as the header preamble and SYNC bytes. The data field itself is always 256 words long. Any unused portion of the sector will be zero filled during a write operation. The 32-bit ECC is generated during a write, and is used during a read to check the validity of the data. Any single error burst anywhere in the data field of 11 bits or less can be corrected. The error pattern and position are located by the controller, the software may then perform the correction of the data after it is transferred to memory.

2.4.3.3 Postambles

The postambles provide areas for turning off the write amplifiers, for turning on read amplifiers, and for switching from read-to-write. Write splices will exist within all of these areas. The sector pulse postamble will also include a head-scatter area on removable media drives.

2.4.3.4 Recovery Area

The recovery area along with the preceeding postamble is required for head - scatter tolerances on removable media drives.

2.5 GENERAL PROGRAMMING INFORMATION

2.5.1 Deleted Commands

The SC12/C emulates the RK611 controller in its responses to all normal commands and register modifications except the diagnostic mode commands. The diagnostic mode commands (DMD bit in RKMR1 set) will cause the controller to go busy for approximately 40 microseconds after which the controller will become ready and will request an interrupt if interrupts enabled as in other commands; however, the command function will be ignored and not executed.

2.5.2 Extended Commands

The SC12/C will execute an extended set of commands not found on the RK611 controller. To execute any of the extended commands, an enable flag must be set prior to issuing the command. To set the enable flag (flag exists only in firmware register), the Spare Register must contain a 1 in bit 15 and a 0 in bit 14 as the RKMR3 register is written (normally a read-only register) with all ones. The enable flag is cleared by a controller reset, subsystem clear, bus INIT, or by executing any command. The following commands are effective only if the enable flag is set. Attempting any extended command except "27" without the enable flag set will result in the illegal function (ILF) bit of RKDS being set along with the controller error (CERR) bit of RKCS1.

1. Hardware Format

The hardware format command (code 27 in RKCS1) will cause the entire logical drive to be formatted. All headers are written and the data fields are written with the bad sector file format which includes the pack ID number. The number entered into the Spare Register (177462) will be used for the pack ID. The word count, Disk Address Registers and Bus Address Registers are not used in this command. The controller will become ready and will interrupt the processor (if enabled) when finished.

2. Logical Write Protect

This command serves many functions, one of which is to logically write protect a logical drive. This command is executed by writing a "33" command into RKCS1 after which bits 7-0 of the Spare Register will be copied and used as the write protect switches for drives 7-0 respectively. A set bit will cause a drive to be write protected; a reset bit will cause the drive to be not write protected only if the physical disk unit which the drive is mapped onto is also not write protected.

A second function of this command is to load a firmware Switch Register. When the command is executed, bits 13-8 of the Spare Register (177462) are copied to an internal firmware Switch Register. The Switch Register bits are cleared by writing into them with this command or whenever a power-up sequence occurs on the controller. Only one switch (bit 9) is used presently. Its function when set, is to limit the number of disk revolutions before a header search may abort to one revolution. Normally the search is continued for four revolutions except for write check commands, for which it is limited to one revolution also.

A third function of this command is to fill the data silo (177464) with the first 255 words of the Firmware Register block which contains the Controller Registers and configuration constants. Successive reads of the silo may then enable software to read this information for diagnostic purposes.

As with other commands, the controller will become ready and interrupt the processor (if enabled) when its function is completed.

3. Read Unit Headers

This command is used primarily to verify tracks of headers written to implement the track replacement function. It is executed by writing a "35" command in RKCS1. It differs from a standard read header command in that an entire track of headers (physical unit track) is read to the silo with

one command. The headers are in order starting with the one after the index pulse and following the three to one interlace pattern until the last header is read. The RKDC and RKDA Registers must be loaded prior to this command with the desired physical cylinder and track to be read, as in the special write header command.

4. Write Unit Headers

This command is executed by writing a "37" command into RKCS1. Its primary function is to write headers to implement the track replacement function. It is similar to a normal write header command except that physical unit addresses are used instead of logical drive addresses. Before issuing the command, the RKDC Register must contain the physical cylinder address, the RKDA Register must contain the physical track address (no sector data - just 10 bits of right justified track address), and the RKWC and RKBA Registers must point to a memory block with the data to be written in the headers and with enough data for an entire physical disk track of headers.

To implement the track replacement function, the track to be replaced must be filled with headers of the following pattern:

1st Word - new physical cylinder address

2nd Word - new physical track address with bits 13, 12, and 10 additionally set to flag the track replace mode

3rd Word - exclusive "OR" of words one and two

The replacement track must then be written using this command with the normal header format as would be found on the replaced track.

BLANK

This section describes the step-by-step procedure for installation of the SC12/C Disk Controller in a PDP-11 system.

3.1 INSPECTION

A visual inspection of the board is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROM's should be examined carefully to insure that they are firmly and completely seated in the sockets.

3.2 DISK DRIVE PREPARATION

The disk drive must be configured for the proper number of sectors, and have an ID plug or address selection switches properly configured.

3.2.1 Sectoring

See Appendix A, Configuration Selection, for the correct sector count settings for the disk drives in use. The exact method of entering the sector count differs from one drive manufacturer to another and the particular drive manual should be consulted for the exact procedure.

3.2.2 ID Plug

An ID plug in the range of 0-1 should be placed in the drive. Be careful that the drives do not have the same number. Some drives have their address selected by means of switches on one of the logic cards and do not use an ID plug.

3.3 CONTROLLER SETUP

Several configuration setups must be made on the controller before inserting it into the chassis. These are made by SW1,SW2 and SW3.

3.3.1 Address Selection

Switch three (SW3) a six pole DIP switch is setup as follows:

SW3-1: OFF (Not used)

SW3-2: ON (standard controller address range of 177440-177476)

SW3-3: OFF (Alternate controller address range of 176700-176736)

SW3-4: OFF (Not used)

SW3-5: OFF (Not used)

SW3-6: OFF (when OFF, addressing of 2K of microprogram memory is allowed for the SC12/C emulation)

3.3.2 Configuration Selection

The first six switch pole positions, of the ten pole DIP switch SW2, are used to form one of 64 binary numbers that correspond to a selected drive configuration. SW2-1 is the least significant bit and SW2-6 is the most significant bit. Refer to appendix A SC12/C Configuration Selection for detailed switch setting instructions.

The seventh pole SW2-7 is used to select the interrupt vector. When set, vector 150 (octal) is selected; when reset, vector 210 (octal) is selected.

The eighth pole SW2-8 when set, enables carriage offset commands to be issued to the physical drive to recover marginal data.

The ninth and tenth poles, SW2-9 and SW2-10, are used in conjunction with SW2-1 through SW2-6 to select configurations and are explained in Appendix A in the SC12/C Configuration Selection Section.

3.3.3 Card Edge Switches

Switch 1 (SW1) is a four pole DIP 'piano-type' switch mounted on the outer card edge between connectors J2 and J3. It is accessible while the controller is imbedded in the host computer.

SW1-1: Used to reset the hardware and firmware in the controller.

SW1-2: Not used.

SW1-3: Causes a header check error to be reported as a header with good sector flags reset (bad sector) instead of as a header with a bad checksum.

SW1-4: If set at power-up, will cause all drives to be logically write protected during the power-up sequence.

3.4 PHYSICAL INSTALLATION

3.4.1 SPC Slot Selection

The controller may be placed in any SPC slot along the Unibus without regard to NPR priority. The controller contains adequate buffering to prevent data lates and will automatically get off the bus if any other device is waiting for the Unibus. If the system contains a Unibus repeater, the controller will not give priority to devices which are on the CPU side of the repeater when the controller is on the far side of the repeater. This may require

that the controller be placed on the CPU side of the repeater or that all DMA devices be on the far side of the repeater.

3.4.2 NPG Signal Jumper

The NPG signal jumper between pins CA1 and CB1 on the backplane must be removed so that the NPG signal passes through the controller.

3.4.3 Mounting

The controller board should be plugged into the PDP backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the board with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly in the throat of the connector before attempting to seat the board by means of the extractor handles.

3.5 CABLING

The subsystem cabling of the drives and controller is shown in Figure 3-1.

3.5.1 A Cable

The 60-wire A cable should be plugged into the connector on the A board of the controller and wired to the first drive. If a second drive is used, it is then daisy-chained to it. The last drive on the A cable must have a terminator installed. This part is available from the drive manufacturer. The terminator is generally plugged into one of two A cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin 1 of the board connector is on the left. Pin 1 of the cable connector has a notch on the connector body to identify it. Twist and flat cable will have brown-brown twist followed by red-brown twist on the pin 1 edge of the cable. The recommended cable part numbers is discussed in Section 2.3.1.1.

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.

3.5.2 B Cable

Each drive must have a 26-wire B cable wired from the drive to one of the B ports of the controller. It makes no difference which B port connection is used by a drive. No external terminators are used with the B cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe. The recommended cable part number is discussed in section 2.3.1.2.

NOTE: Observe the same caution on connector reversal given in paragraph 3.5.1.

3.5.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

3.6 TESTING

3.6.1 Self-Test

When power is applied to the CPU, the controller automatically executes a built-in self test. This self test is not executed with every bus INIT but only on powering up. If the self test has been executed successfully, the LED on the top edge of the controller board will be OFF or flashing. The LED flashes when the controller cannot properly address at least one drive after successfully executing its self test. This will occur if the A and B cables are not properly plugged in, a drive is not powered up with a code plug, or two drives have an identical code plug. If the LED is ON steadily the controller did not pass its self test and the controller cannot be addressed from the CPU.

3.6.2 Register Examination

After powering up the CPU and noting that the LED indicator is not ON steadily, a quick check should be made to ensure that the controller registers can be read from the computer console. The Control Status Register (RKCS1) 177440 will contain 000200 if the controller is ready. To determine the on line status of the selected drive check the Device Status Register (RPDS) 177452 (see section 4. If the CPU has a console emulator all the registers of the controller should be examined.

3.6.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing headers and bad sector file data in all sectors of the disk. This command does not verify the data or headers.

If the drive is on line, the formatting is carried out as follows:

1. Perform a subsystem clear by depositing 000040 into RKCS2 (177450).

2. Select the drive to be formatted by depositing the drive number in the least significant bits of RKCS2 (177450).

3. Deposit a number to be used as a pack ID in the Spare Register (177462); bit 15 of this number must be set, and bit 14 must be reset. 70000X , where X = LUN *)

4. Deposit a pack acknowledge command (3_8 for RK06 or 2003_8 for RK07) in RKCS1 (177440).

5. Deposit all ones in RKMR3 (177476) which is a "read-only" register, to enabled extended command set.

6. Deposit a hardware format command (27_8 for RK06 or 2027_8 for RK07) in RKCS1 (177440) to start formatting. The operation will finish in a couple of minutes with the RDY bit set in RKCS1.

DIAG.
S1C18A-FORM.
S1C19A-Pref.

*) bit 15 shows up in Serial Number when running formatter S1C18A: e.g. 000010000X

X = LUN as above

if this is '0' the Formats will not work !!!

BLANK

Section 4
CONTROLLER REGISTERS

There are 16 device registers in the controller. These are used to interface the controller to the computer. The registers are loaded and/or read under program control in order to initiate selected disk commands, and monitor status and error conditions.

NOTE - The registers must be written with word operations.

4.1 CONTROL/STATUS REGISTER 1 (RKCS1) 777440

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CERR CCLR	DI	DTC PAR	CFMT	CTO	CDT	A17	A16	RDY	IE	0	F3	F2	F1	F0	GO

The RKCS1 register can be read or written via program control and is used to store the current disk command code and operational status of the controller. In addition, the register can initiate command execution and controller clear operation.

Combined Error/Controller Clear (CERR/CCLR) - Bit 15

As a Combined Error (CERR) indicator, bit 15 is set by the controller to indicate that a subsystem error has occurred. However, when the bit is set via program control, a controller initialize (CCLR) operation is enabled which clears the controller, and results in the clearing of bit 15 itself. Thus, if the bit is internally set (CERR) by an error that is followed by an external set (CCLR) to initialize the controller, bit 15 will be cleared. However, since only controller errors will be initialized by CCLR, any error originating in a drive will remain set in the drive.

NOTE: When using a BIC instruction on the RKCS1 register, ensure that a 1 is set in bit 15 of the mask. If this is not done, and CERR is set, a CCLR will occur, and the RK611 will be cleared. For example, to clear the Interrupt Enable (IE) bit (bit 6 in RKCS1), the following instruction format is recommended:

```
BIC #100100, @RKCS1
```

Drive Interrupt (DI) - Bit 14

Drive Interrupt is a read-only bit which is set to differentiate between a drive-initiated interrupt and a controller-initiated interrupt.

The DI bit is set when any drive sets its Attention (ATN0-ATN7) bit (8-15 in RKAS/OF). Thus, if the Interrupt Enable (IE) bit is set, the setting of the DI bit in conjunction with Controller Ready (RDY), bit 7 in RKCS1, indicates a drive-initiated interrupt. The

DI bit is reset by Unibus Initialize (INIT), Subsystem Clear (SCLR), or by the execution of Drive Clear commands to all drives asserting Attention.

Drive-To-Controller Parity Error (DTC PAR) - Bit 13

The DTC Parity Error is a read-only bit that is set on the termination of a command if Parity Test (bit 4 of RKMR1) is set. This bit is for diagnostic compatibility only.

Controller Format (CFMT) - Bit 12

This bit must alway be reset to indicate 22 sector format, which is all the controller emulates of the RK06.

Controller Time-Out (CTO) - Bit 11

Controller Time-Out is a read-only error bit that is set to indicate that GO, bit 0 in RKCS1, has been set for approximately 800 ms. Since this interval exceeds the time required to execute the longest possible drive operation (i.e., a Seek from cylinder 410 to cylinder 0 followed by a 65K word data transfer), the set condition of this bit indicates that the last command has not been completed due to a malfunction.

Controller Drive Type (CDT) - Bit 10

This bit specifies the type of drive that will be selected by the controller. To specify RK06 Disk Drives, the bit must be reset.

Extended Bus Address (A16, A17) - Bits 8, 9

The Extended Bus Address bits reflect Unibus upper address bits 16 and 17, and as such are an extension of the 16-bit RKBA register which contains the memory address required for the current data transfer.

Controller Ready (RDY) - Bit 7

Controller Ready (RDY) is a read-only bit. The bit can be externally set via conventional initialization (INIT, CCLR, SCLR), or internally set upon completion of a command. The RDY bit is reset when GO, bit 0 in RKCS1, is set.

Interrupt Enable (IE) - Bit 6

When the Interrupt Enable (IE) bit is set, the controller will be allowed to interrupt the processor at the end of a command execution or by any ATN being asserted. An interrupt is generated by writing 1's into IE and RDY at the same time.

Function Code (F3-F0) - Bits 4-1

The configuration of the Function Code bits (F3-F0), in conjunction with the setting of the GO bit, allows the selected drive to respond to the following command control configuration.

01	Select Drive	21	Read Data
03	Pack Acknowledge	23	Write Data
05	Drive Clear	25	Read Header
07	Unload	27	Write Header
11	Start Spindle	31	Write Check
13	Recalibrate	33	*Set Logical Write Protect
15	Offset	35	*Reset Logical Write Protect
17	Seek	37	*Set Logical Write Protect

Go (GO) - Bit 0

When the GO bit is set, the disk command Function Code (F4-F0) is executed. With the GO bit set, only two other device register bits can be set (Diagnostic Mode excepted), as follows:

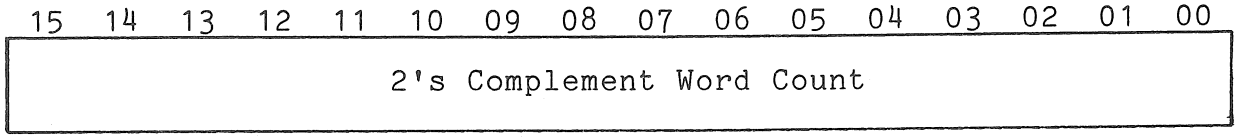
- Controller Clear (CCLR), bit 15 in RKCS1, may be set via program control in order to initialize (general clear and preset) certain device registers within the controller. However, any status and/or error conditions set in the drives are not effected.

- Subsystem Clear (SCLR), bit 5 in RKCS2, may be set via program control in order to initialize both the controller and all of the drives.

When command execution is completed, the GO bit is reset and the controller is ready to accept a new command. However, the GO bit cannot be set if the Combined Error (CERR) bit is set. When CERR is set, the execution of a command can only occur following the initiation of a CCLR.

These commands are illegal and will set the ILF bit in the RKER register unless an enabling procedure is performed before each issuance of the command. To enable these commands, location 177462 (spare register) must contain a one in bit 15 and a zero in bit 14 while location 177476 (RKMR3) is written with all ones.

4.2 WORD COUNT REGISTER (RKWC) 777442



The RKWC is loaded with the 2's complement of the number of data words to be transferred to or from main memory. The register is incremented by 1 after each word transferred, and accommodates a

maximum transfer of 65,356 words. The data transfer stops when the RKWC reaches zero. The RKWC is not cleared by INIT or controller clear.

4.3 BUS ADDRESS REGISTER (RKBA) 777444

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Bus (Memory) Address															

The RKBA register is initially loaded with the low-order 16 bits of the Unibus address of the main memory starting location for a data transfer. The low-order bit (0) is always forced to a 0. The RKBA register is incremented by 2 after transfer of a word to or from memory,if BAI (bit 4, RKCS2) is not set. Overflow of this counter increments A16 and A17 in RKCS1.

4.4 DISK ADDRESS REGISTER (RKDA) 777446

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Track Address			0	0	0	Sector Address				

The RKDA is used to address the sector and track on the drive to or from which the data transfer is desired. It contains a 5-bit sector address counter which is incremented by one at the end of every sector transferred. After reaching a maximum count of 21, it resets to 0. The register also contains a 3-bit track address counter which is incremented everytime the sector address counter reaches maximum count. When this counter reaches maximum count of 2, it reset to 0 and causes the RKDC register to be incremented by one.

4.5 CONTROL/STATUS REGISTER 2 (RKCS2) 777450

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MDS	0	OR	IR	SCLR	BAI	0	U2	U1	U0

The RKCS2 register can be read or written via program control and is used to store the current drive select code, subsystem operational status, and Silo control information. In addition, the register can initiate a Subsystem Clear (SCLR) operation.

Data Late Error (DLT) - Bit 15

This bit is not set during data transfers because of the full sector buffering used in the controller. It can only be set by accessing RKDB without the OR bit in RKCS2 set.

Write Check Error (WCE) - Bit 14

Write Check Error is a read-only error bit that is set to indicate that a data word read from the disk during the execution of a Write Check command did not compare with the corresponding data word contained in main memory. If a write check error is detected and the BAI bit is not set, the RKBA register will contain the memory address of the next data word location (mismatched word address plus two).

Unibus Parity Error (UPE) - Bit 13

Unibus Parity error is a read only bit that is set if a parity error occurs in the Unibus memory while the controller is performing a Write or Write Check command. When the error occurs, the RKBA register contains the address of the word following the word with the parity error (if BAI is not set).

Non-Existent Drive (NED) - Bit 12

Non-existent Drive is a read-only bit that is set when the program issues a command with the GO bit in RKCS1 set to a drive which is not emulated or is located on a physical unit which is not currently available at one of the controller ports.

Non-Existent Memory (NEM) - Bit 11

Non-existent Memory is a read-only bit that is set when the controller is performing an NPR transfer and the memory does not respond within 10 microseconds. The memory address displayed in RKBA is the address of the word following the memory location causing the error.

Programming Error (PGE) - Bit 10

Programming Error is a read-only error bit that is set if any controller register is written (bits for CCLR and SCLR excepted) while the GO bit in RKCS1 is set.

Multiple Drive Select (MDS) - Bit 9

Multiple Drive Select is a read-only error bit that is set when the controller detects two or more physical disk units responding to the same address.

Output Ready (OR) - Bit 7

Output Ready is a read-only bit that is set to indicate that a word is in the Silo output buffer. The bit is cleared by conventional initialization (INIT, CCLR, SCLR), or by the setting of the GO (bit 0 in RKCS1).

Input Ready (IR) - Bit 6

Input Ready is a read-only bit that is set to indicate that the Silo input buffer is ready to accept a word. Conversely, the bit is reset to indicate that the Silo is full and cannot accept a word. The IR bit is also set by conventional initialization (INIT, CCLR, SCLR), or by the setting of the GO (bit 0 in RKCS1).

Subsystem Clear (SCLR) - Bit 5

When the SCLR bit is set via program control, the controller is cleared and all status for the connected drives is initialized.

Bus Address Increment Inhibit (BAI) - Bit 4

When the BAI bit is set, the RKBA register is prevented from incrementing during data transfers. This is primarily a diagnostic aid.

Unit Select (U2-U0) - Bits 2-0

The Unit Select bits select one of eight logical drives. These are read/write bits.

4.6 DRIVE STATUS REGISTER (RKDS) 777452

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SVAL	CDA	PIP	0	WRL	0	0	DDT	DRY	VV	0	SL	ACLO	OFS	0	DRA

The RKDS register is a read-only register that is used to store the operational status of the selected drive. However, information obtained from the drive is not necessarily current or correct unless bit 15 (SVAL) is set.

Status information bits set in the RKDS register can be cleared by conventional initialization (INIT, CCLR, SCLR). However, a Controller Clear (CCLR) operation does not affect status or error condition bits that are currently set in the drives. In addition, a Unibus Initialize (INIT) or Subsystem Clear (SCLR) operation can only reset status or error bits in a drive if the associated status or error condition no longer exists.

Status Valid (SVAL) - Bit 15

Status Valid is a read-only bit that is set to indicate that the bits in both the Drive Status (RKDS) and Error (RKER) registers have been updated for the selected drive. The bit is cleared by conventional initialization (INIT, CCLR, SCLR), initiating a new command (writing into RKCS1), selecting a new drive (writing into RKCS2), or whenever at Attention signal is asserted by the selected drive for a drive status change.

Current Drive Attention (CDA) - Bit 14

Current Drive Attention is a read-only bit that is the logical equivalent of the Drive Status-Change (DSC) bit in the drive defined by the unit select in RKCS1. The assertion of attention indicates that the selected drive has completed a Seek, Offset, Recalibrate, Start Spindle, or Unload command, that the drive has been taken off-line or put on-line by the operator, or that a fault condition exists in the drive.

Positioning-in-Progress (PIP) - Bit 13

Positioning-in-Progress is a read only bit that is set to indicate that the head carriage on the logical drive is in motion.

Write Lock (WRL) - Bit 11

Write Lock is a read-only bit that is set if the selected drive is write protected. A drive may be physically or logically write protected.

Disk Drive Type (DDT) - Bit 8

Disk Drive Type is a read-only bit that is internally conditioned to indicate the type of drive selected. This bit is set to indicate an RK07 drive or reset to indicate an RK06 drive. This bit must compare with the condition of Controller Drive Type, bit 10 in RKCS1, before any command may be executed.

Drive Ready (DRY) - Bit 7

Drive Ready is a read-only bit that is set to indicate that the selected drive is up to speed and the heads are properly positioned over a valid cylinder. Under these conditions, the drive is prepared to receive a command.

Volume Valid (VV) - Bit 6

Volume Valid is a read-only bit that is set to indicate that the Volume Valid flip-flop has been set in the selected drive by a Pack Acknowledge command. The set condition of the bit ensures the program that the cartridge and the unit number plug have not been changed since the last command was issued to the drive, and power has not been removed. The bit is reset when the cartridge, the unit number plug, or ac power is removed from the physical disk unit.

Speed Loss (SL) - Bit 4

This bit is a read-only bit which is always reset for the SC12/C emulation.

Drive AC Low (ACLO) - Bit 3

Drive AC Low is a read-only bit that is always reset.

Offset (OFS) - Bit 2

Offset is a read-only bit that is set to indicate that the selected drive is in Offset mode.

Drive Available (DRA) - Bit 0

Drive Available is a read-only bit that is always set in single port configurations.

4.7 DRIVE ERROR REGISTER (RKER) 777454

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IDAE	COE	0	BSE	ECH	DT	FMTE	DPE	NXF	SKI	ILF

The RKER register is a read-only register that is used to store the error status of the selected drive. However, error information obtained from the drive is not immediately available to program control until the information is validated by the setting of SVAL (bit 15 in the RKDS register), which indicates that a complete status message frame has been received.

Error bits set in the RKER register can be cleared by conventional initialization (INIT, CCLR, SCLR). However, a Controller Clear (CCLR) operation does not affect error bits that are currently set in the drive. In addition, a Unibus Initialize (INIT) or Subsystem Clear (SCLR) operation can only reset error bits in a drive if the associated error condition no longer exists.

Data Check (DCK) - Bit 15

Data Check is a read-only bit that is set to indicate that a data error was detected when the current sector was read.

Drive Unsafe (UNS) - Bit 14

Drive unsafe is a read-only bit that is set to indicate a fault has occurred in the physical unit. This bit is also set if more than one unit responds to a unit address.

Operation Incomplete (OPI) - Bit 13

Operation Incomplete is a read-only bit which is set when a command involving header search cannot find the header.

Drive Timing Error (DTE) - Bit 12

Drive Timing Error is a read-only bit which is set when either the header or data sync pattern is not found. It is also set if a sector or index pulse is found in the sector's data field, or if there are not enough sectors on a physical unit during a firmware format operation.

Write Lock Error (WLE) - Bit 11

Write Lock Error is a read-only bit that is set to indicate that an attempt was made to write on a write protected drive.

Invalid Disk Address Error (IDAE) - Bit 10

Invalid Disk Address Error is a read-only bit that indicates that the address in RKDA or RKDC was invalid at the beginning of a command which used one or both of these registers.

Cylinder Overflow Error (COE) - Bit 9

Cylinder Overflow Error is a read-only bit that is set to indicate that a data transfer attempted to go beyond the last cylinder on a logical disk drive.

Bad Sector Error (BSE) - Bit 7

Bad Sector Error is a read-only bit that is set to indicate that a data transfer has been attempted to or from a sector that has at least one of the two Good Sector Flags (Header Word 2, bits 14 and 15) reset, indicating a bad sector.

Error Correction Hard (ECH) - Bit 6

Error Correction Hard is a read-only bit that is set to indicate that a data error detected by the Error Correction Code (ECC) logic in the controller cannot be corrected using ECC.

Drive Type Error (DT) - Bit 5

Drive Type Error is a read-only bit that is set when the drive type status bit returned from the selected drive does not compare with the CDT bit (bit 10) in RKCS1.

Format Error (FMTE) - Bit 4

Format Error is a read-only bit that is always zero for the SC12/C.

Control-to-Drive Parity Error (DPE) - Bit 3

Controller-to-Drive Parity Error is a read-only bit that is set when a command is issued to the controller with the PAT bit (bit 4) in RKMR1 set.

Non-Executable Function (NXF) - Bit 2

Non-Executable Function is a read-only bit that is set to indicate that a Seek or a Write command has been received by the selected drive while Volume Valid was reset.

Seek Incomplete (SKI) - Bit 1

Seek Incomplete is a read-only bit that is set whenever a seek error occurs in the physical disk unit, or a seek (explicit or implied) to track 3 or 7 is received by a logical unit.

Illegal Function (ILF) - Bit 0

Illegal Function is a read-only bit that is set to indicate that an illegal command (33_8, 35_8, 37_8) has been loaded into RKCS1.

4.8 ATTENTION SUMMARY/OFFSET REGISTER (RKAS/OF) 777456

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATN 7	ATN 6	ATN 5	ATN 4	ATN 3	ATN 2	ATN 1	ATN 0	OF 7	OF 6	OF 5	OF 4	OF 3	OF 2	OF 1	OF 0

The RKAS/OF register can be read or written via program control and as such is used to store the head offset value required by an Offset command, and the current condition of the Attention signal line that is monitored for each drive.

Attention (ATN7-ATN0) - Bits 15-8

The eight attention bits correspond to the eight drives. Each bit is the equivalent of the Drive Status-Change bit associated with each drive. Thus the clearing of this flip-flop clears the ATN bit in the register. The condition of the Drive Status-Change flip-flop for the selected drive is also shown in DSC (bit 14 in A0 Status).

4.9 DESIRED CYLINDER REGISTER (RKDC) 777460

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	Cylinder Address									

The RKDC register can be read or written via program control, and is used to store the address of the desired cylinder. Following an initial load, the value in the RKDC register will be incremented by one whenever the track address value in the RKDA register overflows during a data transfer.

4.10 SPARE REGISTER (SPARE) 777462

The spare register may be written and read back. In the SC12/C emulation the spare register is used for the Pack ID number for firmware format operations, and to setup extended commands.

4.11 DATA BUFFER REGISTER (RKDB) 777464

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Data Buffer															

The RKDB register can be read or written via program control. Reading from the register empties the Silo, while writing into the register fills the Silo. Both the RKDB register and the Silo are cleared by conventional initialization (INIT, CCLR, SCLR).

4.12 MAINTENANCE REGISTER 1 (RKMR1) 777466

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	1	0	0	1	0	0	0	0	DMD	PAT	0	0	MS1	MS0

The RKMR1 register can be read or written via program control, and is primarily used to select the particular A and B status messages.

Diagnostic Mode (DMD) - Bit 5

When Diagnostic Mode bit is set, the controller is effectively disconnected from all of the drives. This mode is not supported by the SC12/C emulation.

Parity Test (PAT) - Bit 4

When the Parity Test bit is set, the controller will simulate even parity on status and control messages from and to the drives for diagnostic compatibility.

Message Select (MS1, MS0) - BIts 1-0

These bits define one of the four pairs of 16-bit status messages (A0-A3 and B0-B3) that can be displayed in RKMR2 and RKMR3. The select bits are cleared by initialization or by loading a command (other than Select Drive) into RKCS1.

4.13 ECC POSITION REGISTER (RKECPS) 777470

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	ECC Position												

The Error Correction Code (ECC) Position register is a read-only register that contains the position of the error pattern as determined by the ECC correction procedure. The error position is the number of bit positions from the beginning of the sector to the right most bit position of the error pattern stored in RKECPT. If the detected error is not correctable using ECC, the ECH error bit in RKER will be set.

4.14 ECC PATTERN REGISTER (RKECPT) 777472

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	ECC Pattern										

The Error Correction Code (ECC) Pattern register is a read-only register that contains the 11-bit error correction pattern obtained from the ECC correction procedure. A 1 in the error pattern indicates a bit of the data in memory from the last read sector which is in error. The error pattern may straddle two 16-bit words in memory. The bit displacement to the right most bit of the pattern is determined by the bit count in RKECPS.

4.15 MAINTENANCE REGISTER 2 (RKMR2) 777474

RKMR2 is a read-only register that displays the "A" status messages for the slected drive. The particular A status is selected by MS1 and MS0 in RKMR1.

Each status message has an odd parity bit in Bit 15 (for diagnostic compatability only) and the Unit No. of the drive in the low-order three bits.

4.15.1 A0 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	DSC	PIP	SO	WL	OFO	FMT	DT	DRY	VV	DRA	0	0	Unit No.		

Drive Status-Change (DSC) - Bit 14

The bit is the OR of any status change due to: completion of a position command, loading or unloading of the heads or any fault condition. The bit is cleared by a Drive Clear command as well as a subsystem clear.

Positioning in Progress (PIP) - Bit 13

This bit is set when a command is being executed that involves head movement.

Spindle On (SO) - Bit 12

This bit is set when the drive is cycled up.

Write Lock (WL) - Bit 11

This bit is set when the drive is in a write lock condition.

Offset On (OFST) - Bit 10

This bit is set to indicate that the logical drive's heads are in an offset condition.

Format (FMT) - Bit 9

This bit is 0 to indicate 22 sector (16 bit per word) format.

Drive Type (DDT) - Bit 8

This bit is a 0 for an RK06 drive, a 1 for an RK07 drive.

Drive Ready (DRDY) - Bit 7

This bit is set when the drive is cycled up, the heads are loaded and positioned over a cylinder, no unsafe condition exists, and the physical disk unit is on-line and ready.

Volume Valid (VV) - Bit 6

This bit is set by the Pack Acknowledge command. It is reset by taking the disk unit off-line.

Drive Available (DRAV) - Bit 5

This bit is always set in single port configurations.

4.15.2 A1 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	HU	RTZ	HL	REV	FWD	SOK	CP	DL	BH	HH	SSP	0	Unit No.		

Heads Unloading (UNLD) - Bit 14

This bit is set during an Unload command to indicate that the heads are unloading.

Return-to-Zero (RCAL) - Bit 13

This bit is set while a recalibrate operation is underway.

Heads Loading (LOAD) - Bit 12

This bit is set during a Load command and is cleared when the unit is cycled up.

Reverse (REV) - Bit 11

This bit indicates that the head carriage is moving toward the spindle.

Forward (FWD) - Bit 10

This bit indicates that the head carriage is moving away from the spindle.

Speed O.K. (SPOK) - Bit 9

This bit is set as long as the drive is cycled up.

Cartridge Present (CRTG) - Bit 8

This bit is always set in an existing drive.

Door Latched (DLTCH) - Bit 7

This bit is always set in an existing drive.

Brushes Home (BHOME) - Bit 6

This bit is always set in an existing drive.

Heads Home (HHOME) - Bit 5

This bit is set whenever R/W UNSAFE condition (bit 14 of message B0) is set, or the drive is cycled down.

Servo Signal Present (SRVSG) - Bit 4

This bit is asserted as long as the drive is cycled up.

4.15.3 A2 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	0	0	Cylinder Difference/Offset Position										Unit No.		

This status message contains the difference between the current cylinder position the that specified by the RKDS; or the complement of the offset magnitude, if in offset mode.

4.15.4 A3 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	Firmware Rev Number MSD							LSD	Drive No.				Unit No.		

This status message contains the "drive serial number" which consists of the logical drive number for the LSB and the firmware revision number for the most significant two bits.

4.16 MAINTENANCE REGISTER 3 (RKMR3) 777476

RKMR3 is a read-only register that displays the "B" status messages for the selected drive. The particular A status is selected by MS1 and MS0 in RKMR1.

Each status message has an odd parity bit in bit 15 (for diagnostic compatability only) and the status I.D. in the low-order two bits.

4.16.1 B0 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	RWU	0	SPL	WLE	SKI	PE	NXF	FLT	ACU	IAE	0	0	0	0	0

Read/Write Unsafe (UNS) - Bit 14

This bit is set when a Fault is detected in the disk unit or when more than one disk unit responds to a given address.

Drive-off-Track (DROT) - Bit 13

Always zero for SC12/C emulations.

Speed Loss Error (SPLS) - Bit 12

This bit is never set in the SC12/C emulation.

Write Lock Error (WLE) - Bit 11

This bit is set if an attempt is made to write on the disk when the logical drive or physical disk unit is write protected.

Seek Incomplete Error (SEKI) - Bit 10

This bit is set whenever a Seek Error is set in the disk unit, or a seek (implied or explicit) is issued to track 3 or 7 on a logical drive.

Controller-to-Drive Parity Error (CDPE) - Bit 9

This bit is set when a command is issued with the Parity Test (bit 4 of RKMR1) set.

Non-Executable Function (NEXF) - Bit 8

This bit is set when a Seek or write command is attempted with the Volume Valid not set. It is reset with Drive Clear or a subsystem clear operation.

Fault (FALT) - Bit 7

This bit is the OR of all the error conditions in this register.

AC Low (ACLOW) - Bit 6

This bit is never asserted for the SC12/C emulation.

Invalid Address Error (IDA) - Bit 5

This bit is set when the address in RKDC or RKDA is not valid (too large).

4.16.2 B1 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	SU	0	0	SSE	0	IE	0	0	0	0	SE	0	0	0	1

Servo Unsafe (UNSF) - Bit 14

Always reset in SC12/C emulation.

Seek Limit (SKLIM) - Bit 13

Always reset in SC12/C emulation.

Seek No-Motion (SKNOM) - Bit 12

Set when seek incomplete error occurs (see RKER bit 2).

Servo-Signal Error (SSE) - Bit 11

Set when drive unsafe condition detected (see RKER bit 14).

Tribit Error (TBE) - Bit 10

Never set in SC12/C emulation.

Index Error (INDXE) - Bit 9

Never set in SC12/C emulation.

Multiple Head Select (MHS) - Bit 8

Never set in SC12/C emulation.

Head Fault (HFLT) - Bit 7

Set when unsafe condition exists (see RKER bit 14).

Write Gate - No Transitions (WGNT) - Bit 6

Never set for SC12/C emulation.

No Write Gate (NWGT) - Bit 5

Never set for SC12/C emulation.

Sector Error (SERR) - Bit 4

Never set for SC12/C emulation.

4.16.3 B2 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	0	0	Cylinder Address									0	0	1	0

This status message contains the current logical cylinder address of the positioner.

4.16.4 B3 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	0	0	0	Track Addr			Sector Addr					0	0	1	1

This status message contains the track and sector address of the drive after last data transfer command to the drive.

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Operations are initiated on the drive selected by the unit select bits in RKCS2 by loading the function code and GO bit into RKCS1. The function code specifies a specific command. The commands can be divided into three categories: data transfer commands, positioning commands, and housekeeping commands. Commands and their corresponding function codes (always odd since the bit must be asserted to execute the command) are described below:

5.1 DATA TRANSFER COMMANDS

These commands involve data transfers to or from the disk and are designated by function codes 21 through 31.

All data transfer commands have seek and sector search functions implied. When the desired cylinder does not equal the current cylinder during the execution of the data transfer, a seek will be issued to the desired cylinder. The controller will then search the desired track for the desired sector and, when found, will start the data transfer. On all commands except the Write Header command (which is the format operation) and Read Header command, a match of the sector header must be made before the data transfer is started.

The desired sector, track and cylinder addresses are updated after the transfer of a sector. Therefore, at the end of a transfer, the disk is set up to transfer the next sequential sector. This allows multiple sector transfers and spiral transfers across tracks and cylinders. When the desired cylinder address changes during a transfer, the implied seek is performed and is termed a mid-transfer seek.

The data transfer commands are described below:

5.1.1 Read Data (21)

This command reads the 256-word data field from the selected sector and transfers the data to memory. When the sector data transfer is complete, the ECC is checked to Insure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction procedure. Assuming no data errors, the word count in RKWC is checked; if not zero, the data transfer operation is repeated with the next sector.

5.1.2 Write Data (23)

This command writes the 256-word data field of the selected sector with words obtained from memory. A two word ECC is appended to each sector. If the word count in RKWC goes to zero during the

sector, the rest of the sector is 0 filled. After a sector transfer the word count in RKWC is checked, and if not zero, the data transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit.

5.1.3 Read Header (25)

This command transfers the three words of the first header encountered into the Silo and then sets RDY. The three words may be read by examining RKDB three times.

5.1.4 Write Header (Format Operation) (27)

This command writes one logical track with headers. Data for the three word headers are obtained from memory. The data field and the ECC are zeroed. (Actual header is four words, the fourth being an extra check character; however, this is performed entirely by firmware and is not apparent to the software.)

5.1.5 Write Check Data (31)

This command reads data from the selected drive and compares it on a word by word basis with that obtained from memory. If the data fails to compare, the WCE status bit is set and the command is terminated immediately.

5.2 POSITIONING COMMANDS

Positioning commands are mechanical movement commands used to position the heads over the disk pack and take milliseconds to complete. Upon initiating the positioning commands, the controller will set the PIP bit. Upon completion of the positioning operation, the controller resets the PIP bit. The positioning commands are described below:

5.2.1 Recalibrate (13)

This command causes the drive positioner to position the heads over cylinder 0. A Return-to-Zero is automatically performed whenever a Seek Error is detected.

5.2.2 Offset (15)

This command directs the selected drive to offset its heads a specific distance from the track center-line. The direction os the offset is determined by OS7 in RKAS/OF register and sets the OF0 mode bit for the drive. The actual offset is done when the data transfer takes place.

5.2.3 Seek Command (17)

This command causes the heads to be moved to the cylinder address specified by the contents of RKDC. When the controller sees the

Seek command with the GO bit set, it sends the cylinder address to the corresponding drive. Upon completion of the seek operation, the ATN is set.

5.3 HOUSEKEEPING COMMANDS

Housekeeping commands are used to place drive logic into a known or initialized state and usually takes only a few microsecondd to execute. The housekeeping commands are listed below:

5.3.1 Select Drive (1)

This command selects a drive and obtains the status information defined by MS1 and MS0 in RKMR1.

5.3.2 Pack Acknowledge (3)

This command sets the VV bit for the command controller. This command must be issued before any data transfer or positioning command can be given if the pack has gone off-line and then on-line. It is primarily intended to avoid unknown pack changes on a dual controller drive.

5.3.3 Drive Clear (5)

This command is used to clear all error flags in the selected drive, provided that the error(s) are no longer present. In addition, the command resets the Status-Change flip-flop for the drive.

5.3.4 Unload (7)

This command simulates the unloading of the heads if they are presently loaded in the selected drive. This operation can only be completed when the operator manually unloads the physical unit.

5.3.5 Start Spindle (11)

This command simulates the starting of the spindle and the loading of the heads on the selected drive if the drive is presently in the unloaded state. This operation will be complete when the operator causes the drive to cycle up.

5.4 EXTENDED COMMANDS

These commands are special to the SC12/C emulation and are not found on the RK611 controller. The special commands are enabled by writing key word(s) in the spare register and RKMR1. The commands may then be executed as other commands by writing to RKCS1 with the GO bit set. The extended command enable sequence must be executed before each extended command given.

To enable the extended command set, the spare register (177462) must contain a one in bit 15 and a zero in bit 14 as the RKMR3

register is written with all one's. The enable is removed with the execution of any command, a bus INIT, subsystem clear, or controller clear.

The following special commands may be executed, after performing extended command enable operation. If the commands are issued without performing the enable operation, the "27" command will result in the execution of the standard track format operation, while the "33", "35", or "37" commands will cause the ILF (Illegal function) bit to set in RKER.

5.4.1 Format Drive (27)

This command, normally a write header, when enabled to be an extended command will cause the entire drive to be hardware formatted. The data wich was written in the Spare Register prior to the command will be used for the pack ID number and all blocks will be written with the bad sector block format.

5.4.2 Write Protect (33)

This command has multiple functions. The first is to logically write lock or unlock the logical drives. When the command is issued, the bits 7-0 of the Spare Register are used as the write lock switches for drives 7-0 respectively. A set bit will cause the drive to be write protected. A reset bit will remove the protect state, providing the physical unit on which the drive is mapped is not write protected.

The command also fills the data buffer (silo) with the first 255 words of the hardware buffer (see symbol table) which contains the controller registers, configuration constants, and firmware registers. Successive reads of the silo will then enable software to read the drive size and configuration information, etc. for diagnostic purposes.

The command also loads a firmware switch register when executed. Bits 13-8 of the Spare Register are copied and saved as the Switch Register. Presently only one switch is used (bit 9) which limits number of disk revolutions to one during a header search before the search is aborted. Normally, search is attempted for four revolutions, except for write check commands, for which it's also limited to one revolution.

5.4.3 Read Unit Headers (35)

This read header command differs from the normal read header command in that an entire track of headers (physical unit track) is read to the silo in one command. The headers are in order starting with one after the index pulse. (The interlace pattern is followed such that consecutive headers are not physically adjacent.)

The RKDC and RKDA registers must be loaded prior to this command with the desired physical cylinder and track to be read, as in the write unit headers command.

5.4.4 Write Unit Headers (37)

This write header command is used to write headers in conjunction with the track replacement function. It is similar to the normal write header command except that physical unit addresses are used instead of logical drive addresses. Before issuing the command, the RKDC Register must contain the physical cylinder address; the RKDA Register must contain the physical unit track address (no sector, just ten bits of track address) and the Bus Address and Word Count Registers must point to a memory block with the correct amount of data for the number of headers-per-track on the physical unit.

To write over a bad track, the header data should be as follows:

1st Word - New physical cylinder address.

2nd Word - New physical track address plus bits 13, 12, and 10 set to indicate track replace mode.

3rd Word - Exclusive "OR" of words one and two.

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APPENDIX A

SC12/C CONFIGURATION AND OPTION SELECTION

A.1 INTRODUCTION

To allow the user of the SC12/C the greatest amount of flexibility in selecting disk drives for his system, the SC12/C supports a wide variety of disk types and offers a number of other user selectable options. This appendix is designed as a quick refernece to the various switches and jumpers which make this flexibility possible. For more deatiled information about user selectable options see the Installation chapter in this manual.

A.2 DRIVE CONFIGURATION

The SC12/C unit is capable of controlling a wide variety of disk drives of various sizes and types. The various drives that are supported are defined by the Configuation PROM. Table A-1 is a list of the drive types and sizes that are supported. The user may choose between the available options by means of configuation switch SW2. The correct switch settings for each of the various configurations are given in Table A-2.

A.2.1 Single Drive Installations

To find the configuration setting that is suitable for your single disk drive installation, use the following process. Note that all configurations require that the drive be hard sectored as noted in the Sec column of Table A-1. See the manufacture's drive installation manual for instructions.

1. Locate your drive type and size in Table A-1. Note down the configuation code(s) assigned to your drive. Note also the cylinder (Cyl), track (Trk) and sector (Sec) figures for the drive.

2. Find the configuration number for your drive in the CONF NO. column of Table A-2. If there is more than one number for an individual drive, start with the smallest. Note that for each configuation row, specifications are given for two physical drives, Unit 0 and 1.

3. When you find the proper row, compare the Physical Drive cylinder, track and sector figures for Unit 0 in Table A-2 with the numbers you noted down from Table A-1. They must match. If they do not, go on to the next higher configuration number, etc, until you find a match.

4. When you find a match, set the Configuration Switches (SW2) as indicated in Table A-2. (Generally, there is more than one match. In such cases, look at the Logical Unit and Drive Type column for each configuration where a match was found. Choose the Logical configuation you like best, and set the Configurations Switches accordingly.)

A.2.2 Dual Drive Installations (same type drive)

To find the configuration setting that is suitable for your dual disk drive installation (drives same size and type), use the following process. Note that all configurations require that the drives both be hard sectored as noted in the Sec column of Table A-1. See the manufacture's drive installation manual for instructions.

1. Locate your drive type and size in Table A-1. Note down the configuation code(s) assigned to your drives. Note also the cylinder (Cyl), track (Trk) and sector (Sec) figures for the drives.

2. Find the configuration number for your drives in the CONF NO. column of Table A-2. If more than one number was given for the drives, start with the smallest. Note that for each configuation row, specifications are given for two physical drives, Unit 0 and 1. The physical cylinder, track and sector numbers for Unit 0 and 1 in that row must match. If they do not, go on to the next configuration number.

3. When you find the proper row, compare the Physical Drive cylinder, track and sector figures for both Unit 0 and Unit 1 in Table A-2 with the numbers you noted down from Table A-1. They must match. If they do not, go on to the next higher configuration number, etc, until you find a match.

4. When you find a match, set the Configuration Switches (SW2) as indicated in Table A-2. (Generally, there is more than one match. In such cases, look at the Logical Unit and Drive Type column for each configuration where a match was found. Choose the Logical configuation you like best, and set the Configuration Switches accordingly.)

A.2.3 Dual Drive Installations (different drive types)

To find the configuration settings that are suitable for your dual disk drive installation (different drive size and type), use the following process. Note that all configurations require that the drives both be hard sectored as noted in the Sec column of Table A-1. See the manufacture's drive installation manual for instructions.

1. Locate your drive types and sizes in Table A-1. Note down the configuation code(s) assigned to each drive. Note also the cylinder (Cyl), track (Trk) and sector (Sec) figures for each drive.

2. Once you have located and noted your drive configuation codes, compare the codes for each drive to one another. There must be at least one match if that drive combination is supported. Note that for all configurations that support different drive sizes, the configuration code does not have a letter suffix.

3. Consult Table A-2. Find the configuration number that both drives have in common in the CONF NO. colum . If more than one number was given for the drive, start with the smallest.

4. For each configuation row, specifications are given for two physical drives, Unit 0 and 1. The two sets of numbers will be different. Compare the physical cylinder, track and sector numbers for each unit with the corresponding numbers from Table A-1. The physical drive that matches the numbers for physical unit 0 becomes unit 0. The physical drive whose numbers match physical unit 1's becomes unit 1.

5. If there is more than one configuration supported, look at the Logical Unit and Drive Type column for each configuration where a match was found. Choose the Logical configuation you like best, and set the Configuration Switches (SW2) accordingly.

TABLE A-1
DRIVES SUPPORTED

Mfg. - Model	Cyl	Trk	Sec	Configurations
AMPEX 165	823	10	35	12, 12A, 17, 23
AMPEX 165-210	1024	10	35	20
AMPEX 9160	1645	5	35	21, 21A
AMPEX DFR-932,946,996 -	-	-	- SAME AS CDC 9448-32,64,96	
BALL BD160	1645	5	35	20
BASF 6172	614	3	23	7, 7B
BASF 6173	614	5	23	7, 7A
CENTURY T82	815	5	35	12, 12B
CENTURY T82RM	823	5	35	12, 12B
CDC 9448-32	823	2	35	0B, 1, 1B, 2, 2B
CDC 9448-64	823	4	35	0, 3B, 23, 24, 24B
CDC 9448-96	823	6	35	0B, 1, 1A, 2, 3, 3A, 15, 25, 25B

continued next page.

TABLE A-1, cont.

Mfg. - Model	Cyl	Trk	Sec	Configurations
CDC 9448-32	823	2	33	4, 4A
CDC 9448-64	823	4	33	16, 16A, 24, 24A
CDC 9448-96	823	6	33	4, 4A, 25, 25A
CDC 9762	823	5	35	12, 12B
CDC 9730-80	823	5	35	12, 12B
CDC 9730-160	823	10	35	12, 12A
FUJITSU 2311	589	4	35	10, 10B, 11, 11B
FUJITSU 2312	589	7	35	11, 11A
KENNEDY 5300-70	700	5	35	5, 5B, 15
MEMOREX 612-56	350	8	35	22, 22B
MEMOREX 612-84	350	12	35	22, 22A
PRIAM 3350	561	3	32	5, 5A
PRIAM 3350	561	3	35	6, 6A, 6B, 27
PRIAM 2050	526	3	23	7, 7B
PRIAM 3450	526	5	23	7, 7A, 10, 10A
SLI Sheyenne 3	656	5	19	13, 13A, 13B
SLI Sheyenne 4	656	7	19	14, 14A, 14B, 26

TABLE A-2
DRIVE CONFIGURATIONS

CONF	SW2-								Physical				Logical		
NO.	10	9	6	5	4	3	2	1	Unit	Cyl	Trk	Sec	Unit(s) =	Dr Type	Rev
0	0	0	0	0	0	0	0	0	0	823	4	35	0,1,2,3 =	RK06	A
									1	823	4	35	4,5,6,7 =	RK06	A
0A	0	C	0	0	0	0	0	0	(SAME AS CONF NO. 0)						
0B	C	C	0	0	0	0	0	0	0	823	6	35	0,1,2,3,4,5 =	RK06	
									1	823	2	35	6,7 =	RK06	A
1	0	0	0	0	0	0	0	C	0	823	6	35	0,1 = RK06	2,3 = RK07	A
									1	823	2	35	4,5 =	RK06	A
1A	0	C	0	0	0	0	0	C	0	823	6	35	0,1 = RK06	2,3 = RK07	A
									1	823	6	35	4,5 = RK06	6,7 = RK07	A
1B	C	C	0	0	0	0	0	C	0	823	2	35	0,1 =	RK06	A
									1	823	2	35	2,3 =	RK06	A
2	0	0	0	0	0	0	C	0	0	823	6	35	1,0,2,3,4,5 =	RK06	A
									1	823	2	35	6,7 =	RK06	A
2A	0	C	0	0	0	0	C	0	(SAME AS CONF NO. 2)						
2B	C	C	0	0	0	0	C	0	0	823	2	35	1,0 =	RK06	A
									1	823	2	35	2,3 =	RK06	A

continued next page.

TABLE A-2, cont.

CONF	SW2-								Physical				Logical	
NO.	10	9	6	5	4	3	2	1	Unit	Cyl	Trk	Sec	Unit(s) = Dr Type	Rev
3	0	0	0	0	0	0	C	C	0	823	6	35	1,0 = RK06 2,3 = RK07	A
									1	823	4	35	4,5,6,7 = RK06	A
3A	0	C	0	0	0	0	C	C	0	823	6	35	1,0 = RK06 2,3 = RK07	A
									1	823	6	35	4,5 = RK06 6,7 = RK07	A
3B	C	C	0	0	0	0	C	C	0	823	4	35	1,0,2,3 = RK06	A
									1	823	4	35	4,5,6,7 = RK06	A
4	0	0	0	0	0	C	0	0	0	823	6	33	1,0,2,3,4,5 = RK06	A
									1	823	2	33	6,7 = RK06	A
4A	0	C	0	0	0	C	0	0	0	823	6	33	0,1,2,3,4,5 = RK06	A
									1	823	2	33	6,7 = RK06	A
4B	C	C	0	0	0	C	0	0	(SAME AS CONF NO. 4)					
5	0	0	0	0	0	C	0	C	0	561	3	32	0 = RK07	A
									1	700	5	35	1,2 = RK07	A
5A	0	C	0	0	0	C	0	C	0	561	3	32	0 = RK07	A
									1	561	3	32	1 = RK07	A
5B	C	C	0	0	0	C	0	C	0	700	5	35	0,1 = RK07	A
									1	700	5	35	2,3 = RK07	A
6	0	0	0	0	0	C	C	0	0	561	3	35	0 = RK07	A
									1	561	3	35	1,2 = RK06	A
6A	0	C	0	0	0	C	C	0	0	561	3	35	0 = RK07	A
									1	561	3	35	1 = RK07	A
6B	C	C	0	0	0	C	C	0	0	561	3	35	0,1 = RK06	A
									1	561	3	35	2,3 = RK06	A
7	0	0	0	0	0	C	C	C	0	526	5	23	0 = RK07	A
									1	526	3	23	1 = RK06	A
7A	0	C	0	0	0	C	C	C	0	526	5	23	0 = RK07	A
									1	526	5	23	1 = RK07	A
7B	C	C	0	0	0	C	C	C	0	526	3	23	0 = RK06	A
									1	526	3	23	1 = RK06	A
10	0	0	0	0	C	0	0	0	0	526	5	23	0,1 = RK06	A
									1	589	4	35	2 = RK07 3 = RK06	A
10A	0	C	0	0	C	0	0	0	0	526	5	23	0,1 = RK06	A
									1	526	5	23	2,3 = RK06	A
10B	C	C	0	0	C	0	0	0	0	589	4	35	0 = RK07 1 = RK06	A
									1	589	4	35	2 = RK07 3 = RK06	A
11	0	0	0	0	C	0	0	C	0	589	7	35	0,1 = RK07 2 = RK06	A
									1	589	4	35	3,4,5 = RK06	A
11A	0	C	0	0	C	0	0	C	0	589	7	35	0,1 = RK07 2 = RK06	A
									1	589	7	35	3,4 = RK07 5 = RK06	A
11B	C	C	0	0	C	0	0	C	0	589	4	35	0,1,2 = RK06	A
									1	589	4	35	3,4,5 = RK06	A

continued next page.

TABLE A-2, cont.

CONF NO.	SW2- 10	9	6	5	4	3	2	1	Unit	Physical Cyl	Trk	Sec	Logical Unit(s)	=	Dr Type	Rev
12	0	0	0	0	C	0	C	0	0	823	10	35	0,1,2,3,4	=	RK07	A
									1	815	5	35	5,6 = RK07		7 = RK06	A
12A	0	C	0	0	C	0	C	0	0	823	10	35	0,1,2,3,4	=	RK07	A
									1	823	6	35	5,6,7	=	RK07	A
12B	C	C	0	0	C	0	C	0	0	815	5	35	0,1 = RK07		2 = RK06	A
									1	815	5	35	3,4 = RK07		5 = RK06	A
13	0	0	0	0	C	0	C	C	0	580	5	20	0	=	RK07	A
									1	580	5	20	1,2	=	RK06	A
13A	0	C	0	0	C	0	C	C	0	580	5	20	0	=	RK07	A
									1	580	5	20	1	=	RK07	A
13B	C	C	0	0	C	0	C	C	0	580	5	20	0,1	=	RK06	A
									1	580	5	20	2,3	=	RK06	A
14	0	0	0	0	C	C	0	0	0	656	7	20	0 = RK07		1 = RK06	A
									1	656	7	20	2,3,4	=	RK06	A
14A	0	C	0	0	C	C	0	0	0	656	7	20	0 = RK07		1 = RK06	A
									1	656	7	20	2 = RK07		3 = RK06	A
14B	C	C	0	0	C	C	0	0	0	656	7	20	0,1,2	=	RK06	A
									1	656	7	20	3,4,5	=	RK06	A
15	0	0	0	0	C	C	0	C	0	700	5	35	0,1	=	RK07	A
									1	823	6	35	2,3 = RK06		4,5 = RK07	B
15A	0	C	0	0	C	C	0	C	(SAME AS CONF NO. 5B)							
15B	C	C	0	0	C	C	0	C	0	(SAME AS CONF NO. 1A)						
16	0	0	0	0	C	C	C	0	0	823	4	33	1,0,2,3	=	RK06	B
									1	823	4	33	4,5,6,7	=	RK06	B
16A	0	C	0	0	C	C	C	0	0	823	4	33	0,1,2,3	=	RK06	B
									1	823	4	33	4,5,6,7	=	RK06	B
16B	C	C	0	0	C	C	C	0	(SAME AS CONF NO. 16)							
17	0	0	0	0	C	C	C	C	0	823	10	35	0,1,2,3,4	=	RK07	B
									1	823	2	35	5,6	=	RK06	B
17A	0	C	0	0	C	C	C	C	(SAME AS CONF NO. 12A)							
17B	C	C	0	0	C	C	C	C	(SAME AS CONF NO. 1B)							
20	0	0	0	C	0	0	0	0	0	1024	10	35	0,1,2,3,4,5	=	RK07	B
										823	2	35	6,7	=	RK06	B
20A	0	C	0	C	0	0	0	0	0	1024	10	35	0,1,2,3,4,5	=	RK07	B
									1	1024	4	35	6,7	=	RK07	B
20B	C	C	0	C	0	0	0	0	(SAME AS CONF NO. 1B)							
21	0	0	0	C	0	0	0	C	0	1645	5	35	0,1,2,3,4	=	RK07	B
									1	823	2	35	5,6	=	RK06	B
21A	0	C	0	C	0	0	0	C	0	1645	5	35	0,1,2,3,4	=	RK07	B
									1	1645	3	35	5,6,7	=	RK07	B
21B	C	C	0	C	0	0	0	C	(SAME AS CONF NO. 1B)							

continued next page.

TABLE A-2, cont.

CONF NO.	SW2-10	9	6	5	4	3	2	1	Unit	Physical Cyl	Trk	Sec	Logical Unit(s) = Dr Type	Rev
22	0	0	0	C	0	0	C	0	0	350	12	35	0,1 = RK07 2 = RK06	B
									1	350	8	35	3 = RK07 4 = RK06	B
22A	0	C	0	C	0	0	C	0	0	350	12	35	0,1 = RK07 2 = RK06	B
									1	350	12	35	3,4 = RK07 5 = RK06	B
22B	C	C	0	C	0	0	C	0	0	350	8	35	0 = RK07 1 = RK06	B
									1	350	8	35	2 = RK07 3 = RK06	B
23	0	0	0	C	0	0	C	C	0	823	10	35	0,1,2,3,4 = RK07	B
									1	823	6	35	5 = RK06 6,7 = RK07	B
23A	0	C	0	C	0	0	C	C	(SAME AS CONF NO. 12A)					
23B	C	C	0	C	0	0	C	C	(SAME AS CONF NO. 3 A)					
24	0	0	0	C	0	C	0	0	0	823	4	33	1,0,2,3 = RK06	D*
									1	823	4	35	5,4,6,7 = RK06	D*
24A	0	C	0	C	0	C	0	0	0	823	4	33	1,0,2,3 = RK06	D*
									1	823	4	33	5,4,6,7 = RK06	D*
24B	C	C	0	C	0	C	0	0	0	823	4	35	1,0,2,3 = RK06	D*
									1	823	4	35	5,4,6,7 = RK06	D*
25	0	0	0	C	0	C	0	C	0	823	6	33	1,0 = RK06 2,3 = RK07	D*
									1	823	6	35	5,4 = RK06 6,7 = RK07	D*
25A	0	C	0	C	0	C	0	C	0	823	6	33	1,0 = RK06 2,3 = RK07	D*
									1	823	6	33	5,4 = RK06 6,7 = RK07	D*
25B	C	C	0	C	0	C	0	C	0	823	6	35	1,0 = RK06 2,3 = RK07	D*
									1	823	6	35	5,4 = RK06 6,7 = RK07	D*
26	0	0	0	C	0	C	C	0	0	656	7	19	0 = RK07 (1319 CYL)	E*
									1	656	7	19	1 = 4K07 (1319 CYL)	E*
26A	0	C	0	C	0	C	C	0	(DO NOT SELECT)					
26B	C	C	0	C	0	C	C	0	(DO NOT SELECT)					
27	0	0	0	C	0	C	C	C	0	561	3	35	0 = RK07 (891 CYL)	E*
									1	561	3	35	1 = RK07 (891 CYL)	E*
27A	0	C	0	C	0	C	C	C	(DO NOT SELECT)					
27B	C	C	0	C	0	C	C	C	(DO NOT SELECT)					

NOTES: C = Closed (ON), O = Open (OFF)
*Rev D and above configurations requires SC12/C Rev B or above emulation PROMs.

A.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC12/C can be user selected. The functions of the switches that select those options are defined in Tables A-3, A-4 and A-5, below.

TABLE A-3
OPTION SWITCH SETTINGS

Option Sw	Open	Closed	Function
SW1-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW1-2			Not used[1]
SW1-3	Disable	Enable	Header check error to be bad sector
SW1-4	Disable	Enable	Drives to be write-locked on power-up

[1]All unused switches MUST BE OFF.

TABLE A-4
CONFIGURATION SWITCH SETTINGS

Config Sw	Open	Closed	Function
SW2-1			Drive Configuration[2]
SW2-2			Drive Configuration[2]
SW2-3			Drive Configuration[2]
SW2-4			Drive Configuration[2]
SW2-5			Drive Configuration[2]
SW2-6			Drive Configuration[2]
SW2-7	210	150	Interrupt vector address
SW2-8	Disable	Enable	Head offset capability
SW2-9			Drive Configuration[2]
SW2-10			Drive Configuration[2]

[2]See Table A-2 for settings

TABLE A-5
ADDRESS SWITCH SETTINGS

Address Sw	Open	Closed	Function
SW3-1			Not used[1]
SW3-2		777440	Standard Unibus Address[3]
SW3-3		776700	Alternate Unibus Address[3]
SW3-4		776300	Alternate Unibus Address[3]
SW3-5		772040	Alternate Unibus Address[3]
SW3-6	Disable	Enable	1k Microcode Address Range (normally open)

[1]All unused switches MUST BE OFF.
[3]Only one address may be selected. All other address switches MUST BE OFF.

APPENDIX B

DIAGNOSTIC MODIFICATIONS

B.1 ZR6A-CO RK611 Diskless Diagnostic - Part 1 - (Aug 77) - S1C20A

Location	From	To
12542	1404	404
13432	1404	404
14316	1404	404
15202	1404	404

B.2 ZR6K-EO RK06 Functional Controller Diagnsotic (Feb 78)-S2C11A

Location	From	To
6304-6306	12737,62	137,6540
20606-20610	12737,12	137,22050
25612-25614	12737,5	137,26312
26372-26374	12737,12	137,30212
11346-11350	12737,12	137,11710
12042-12044	12737,12	137,12352
35110	42777	2
10630	104431	104435
10710	104423	104435
11272	104424	104435
12022	104425	104435
12432	104431	104435
12540	104431	104435
12570	104424	104435
22202	104424	104435
22374	104424	104435
22474	104424	104435
22656	104431	104435
24326	104431	104435
22132	104431	104435
30332	104426	104435
32162	104427	104435
11230	104431	104435
11772	104431	104435
37040	000020	000400

B.3 ZR6M-DO RK611/06 Subsystem Verify-Part 1 (Feb 78)-S1C22A

Location	From	To
55730-55732	5737,177572	137,56060
26044-26046	5037,5532	240,240

B.4 ZR6N-DO RK611/06 Subsystem Verify-Part 2 (Feb 78)-S1C23A

Location	From	To
23252	177145	177400
23262-23264	1002,5260	62760,100
57744-57746	5737,177572	137,60074
30602-30604	5037,5532	240,240

B.5 ZR6L-CO RK06 Formatter (Feb 78) - SIC18A

Location	From	To
20734	3670	4670
22030	3670	4670
31672	6	5
31676	12	0
31726	3660	4660
23576	104411	207
22056	10114	10124
22060-22062	104412,207	137,27536
27534	1457	457
27536-27540	52737,4	12714,17777
27542-27544	6364,105737	104412,207
2032-2034	44004,46413	46050,45563
2036-2040	47712,50310	0,0
27734-27736	104104,42737	104055,4737
27740-27742	2,6364	22024,240

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What features are most useful?_____

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