Teletype Corporation
Circuit Description

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SECTION I - GENERAL TECHNICAL INFORMATION (Basic Function)

1. The 610080 Console Logic Card (CC080) is a double sided circuit card, 5-1/2" x 12", containing Teletype MOS circuit packs, commercial integrated circuit packages and discrete components. The console frame, the keyswitch channels and all keyswitches mount to this card.

2. The CC080 assembly provides the following features:

2.1 Sense up to 67 keys depressed by an operator.

2.2 Generate and transmit codes for up to 58 keys.

2.3 Generate alternate codes, when required, when shift or control keys are depressed.

2.4 Generate characters repeatedly with a universal repeat key.

2.5 Provide 5 Light Emitting Diode (LED) indicators controlled and powered by an external source.

2.6 Provide a "CAPS LOCK" mode for selectively shifting only alpha characters.
Teletype Corporation
Circuit Description
4080CD
Issue 2
Sheet 3

SECTION II - DETAILED DESCRIPTION

1. ASSOCIATED DOCUMENTS - 410080 Assembly Drawing, 40800D Schematic Diagram.

2. THEORY OF OPERATION

2.1 Keyswitches and Sense Amplifiers (FS-1, Sheet B1)

2.1.1 Each capacitive keyswitch is connected to a single input of a Sense Amplifier M.A1, M.BA or M.BL4. The Sense Amplifier determines the logic state applied to an input by comparing the charging time of the keyswitch connected to an input to the charging time of a Reference Capacitor (C2, C10 or C15) which is connected to input 0. Charging current for the Sense Amplifier is provided by Reference Resistors R86, R27 or R30 connected to each Sense Amplifier's sourcing pin ($\Sigma$) and returned to VG2.

2.1.2 When power is first applied to 4080CD, the Keyswitch Logic MLAS initializes all Sense Amplifiers by transmitting two consecutive pulses, Master Reset (MR) and SRZ. The 1/0 leads are active when at VG. The MR and SRZ pulses, which last for one complete clock cycle each, initiate Master Reset and Synchronizing functions. The Synchronizing pulse forces the Sense Amplifiers to the Reference Input (0) to begin a scan. ($V_{H} \geq V_{SS} + 4V$).

2.1.3 The Sense Amplifiers charge their associated Reference Capacitor to measure a reference charging time. Subsequently, the Keyswitch Logic transmits Data Enable (DE) pulses which advance the Sense Amplifiers to their first keyswitch inputs and places the keyswitches under test. Each Sense Amplifier determines the state of the keyswitch by determining that the keyswitch charges faster or slower than the reference capacitor.

2.1.4 After 12 clock cycles the Keyswitch Logic transmits another Data Enable pulse. The Sense Amplifiers respond by transmitting two Data Bits (active to VG5 when $\Sigma$ is at VG2). Data Bit 1 will be active at VG5 when the keyswitch being sensed is first encountered as 'depressed'. Data Bit 2 will be active at VG5 as long as the keyswitch continues to be depressed. This action continues until the Sense Amplifiers have tested all inputs (21 keyswitches). The Keyswitch Logic transmits a number of extra Data Enable pulses (ignored by the Sense Amplifiers) while internal logic functions are being performed. The Keyswitch Logic then re-transmits the SYNC pulse and the scan cycle repeats.

2.2 Keyswitch and Interface Logic (FS-2, Sheet B2)

2.2.1 The Keyswitch Logic (MLAS) controls the operation of the Sense Amplifiers (see Section 2.1.3 and 2.1.4) and provides coded output to the interface.

2.2.2 When power is first applied to 4080CD, Capacitor C8 is discharged. During the time that it is charging (through R22) the Keyswitch Logic will send Master Reset and SYNC pulses to the Sense Amplifiers. In addition, the Serial Send Data output will be held at VG. After C8 has charged beyond the threshold of the Power-On-Reset Input (PORIN), the Keyswitch Logic will transmit only SYNC and Data Enable pulses to the Sense Amplifiers and normal operation of the 4080CD can begin.

2.2.3 Once each scan the Keyswitch Logic transmits a SYNC pulse to establish synchronization. After the SYNC pulse and a timing interval the Keyswitch Logic transmits a series of Data Enable pulses, one pulse per 12 clock cycles. The Sense Amplifiers respond to each Data Enable pulse by transmitting the two data bits corresponding to their input under test. Data Bits are valid on the two consecutive $\Sigma$ periods following the Data Enable pulse, when $\Sigma$ is at VG2.

2.2.4 After all keyswitches have been tested the scanning cycle repeats. A test signal, end of scan (EOS/ALARM) is provided for use as a timing reference. EOS is active to VG5 for 8.9 microseconds with a repetition rate of 4.57 milli-seconds. End of Scan is active twenty-four $\Sigma$ periods after the SYNC pulse.

2.2.5 When a keyswitch has been sensed as 'depressed' the Keyswitch Logic will determine if it is to be sent as a character or to modify the code of the previous keyswitch (i.e., if the switch is Caps Lock, Shift, Control, or Repeat). If the c.e. is to be sent it will appear as Mark-space data on the Serial Send Lead. This lead (pin 6 at J1) is normally marking (at $V_{CC} + 0.7 V$). The high level of both Serial Send Data and Repeat Mode (RPM) is limited to VCC by CR2, CR3, CR8 and R7. The code consists of 11 bits: one start bit, 8 code bits, one parity bit and one stop bit. The low level (space) is $< V_{CC} + 0.7 V$. One bit time = 163 us. Output impedance for both Serial Data and RPM shall be $< 500$ ohms in either logic state.

2.2.6 Repeat Mode (RPM) is $V_{CC} + 0.7 V$, as long as the Repeat key is not depressed. When the Repeat key is depressed, the Repeat Lead of MLAS goes to VCC and RPM (pin 7 of J1) goes to $V_{CC} + 0.7 V$. RPM will return to $V_{CC}$ when the Repeat key is released. If any other keyswitch is depressed while the Repeat key is depressed, the character associated with that keyswitch will be sent once per scan (4.57 ms).

2.2.7 Switches SQ, S1, and S2 are normally open D.C. contact latching switches. The depressed (latched) state connects the corresponding pin in J1 to $V_{CC}$. S3 and S4 are normally open D.C. Contact switches. When S3 or S4 is depressed, the corresponding pin in J1 is connected to $V_{SS}$.

2.2.8 Light Emitting Diodes (LED's) in the indicating keyswitches are controlled by their respective pins in J1. On current shall be $> 10$ ma but $< 15$ ma.

2.3 Clock Generation and Drivers (FS-3, Sheet B3)

2.3.1 The 560 KHz. clock from pin 12 of J1 is divided by 5 by MLB3. The QH (pin 8) output of MLB3 is a 560 Hz cycle waveform at 112 KHz. repetition rate. R28, R29, C11 and C12 de'ay appropriate edges of the 112 KHz signal and are recombined in MLB1 and MLB2 to produce a non-overlapping $\Sigma$ and $\Sigma$ pre-drive signals at pins 11 of MLB1 and MLB2. The non-overlap time is 1.3 us min to 1.2 us max for both non-overlaps.
2.3.2 The predrive signals are coupled to MLA4 by C6 and C7. R14 and R15 limit the current levels. CR9, R34 and CR9, R35 insure a proper voltage swing for the Clock Driver. Clock Driver MLA4 is a high voltage dual inverter. R16 and R17 prevent inductive ringing of the fast transitions on $0_1$ and $0_2$. R12 and R13 bias the outputs of MLA4 slightly "LOW" to prevent clock excursions above $V_{cc}$. The high clock levels (for $0_1$, $0_2$, $0_1L$ and $0_2L$) shall be $V_{cc}$ but ($V_{cc}$-1.7V). The low $0_1$ and $0_2$ levels shall be $V_{cc2}$-1.2V).

2.3.3 R18 and R19 limit current so that CR5 and CR6 can clamp $0_1L$ and $0_2L$ to $V_{cc1}$. $0_1L$ and $0_2L$ are the clocks to MLA5 which requires a lower clock voltage than the other MOS devices. The low $0_1L$ and $0_2L$ levels shall be $V_{cc1}$ but ($V_{cc1}$-1V).

2.4 Power Distribution (PB-4, Sheet B4)

2.4.1 Zener Diode CR1 reduces the -12V by 3.9V, so as to make $V_{cc2}$ approximately -10V with respect to $V_{cc}$. Voltage to Pin 4 of MLA5 is fixed at one diode drop more negative than $V_{cc1}$ by CR7 and R33.

2.4.2 Capacitors C3, C4, C5 and C13 are filter capacitors for the various power supplies.

2.5 Power Requirements

$+12V \pm 10\%$ at 160 ma. max.
$+5V \pm 10\%$ at 100 ma. max.
$-12V \pm 10\%$ at 160 ma. max.

Maximum power dissipation = 4.5 W.

2.6 Temperature Ranges:

Operation: $40^\circ F$ to $110^\circ F$ at 2% to 95% Relative Humidity

Storage: $-50^\circ F$ to $150^\circ F$
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SECTION I - GENERAL TECHNICAL DATA

1. PURPOSE

1.1 The 430700 and 430780 Power Supplies are designed to provide the DC power required to operate the basic Model 43 VSR Set consisting of the Model 43 Printer, OFCON, Controller, and Terminal Data Unit (TDU) or Terminal Auxiliary Unit (TAU). Line input power may be 115 VAC ± 10%, 48/62 hertz or 165 VDC ± 10%. Four regulated DC output voltages are produced; +5V, +12V -12V, -24V. The 430780 provides additional power for sets with extra logic load requirements.

1.2 The input and output ratings are as follows:

Input: 115VAC ± 10%, 58/62 Hz - 0.9 amp for the 430700 and 1.0 amp for the 430780.

Output: +5 VDC ± 5% - 0.75A for the 430700, .80A for 430780.
+12 VDC ± 5% - 0.4A for the 430700, .60A for 430780.
-12 VDC ± 5% - 0.6A for the 430700, .70A for 430780.
-24 VDC - 8%, .409% - 1.0A (AVERAGE)

Logic level total power output of 430780 PSU is not to exceed 18 watts without additional External Cooling.

1.3 All circuitry for the 430700 and 430780 Power Supplies is contained on the 410700 or 410702 Power Supply Card respectively. This card and associated heats sinks, brackets, and covers are assembled to form the 430700 or 430780 Power Supply unit which is mounted in the cabinet rear frame. Line power is applied to the unit through a cable having a three terminal connector. A line fuse is provided in the cabinet rear frame adjacent to the ON/OFF switch. The output is available through a 10 pin connector located at the top edge of the circuit card in the supply.

2. OPERATION

2.1 The 430700 and 430780 Power Supplies are of the "Off-the-Line" Switching Regulator type utilizing a "Ringing Choke" design to accomplish power conversion at a nominal frequency of 20 KHz. This design provides a relatively high power conversion efficiency, and minimizes the size and weight of the supply.

2.2 The AC line voltage is directly converted to DC by a bridge rectifier connected directly to the AC input and filtered by a capacitor on the output side of the bridge rectifier. The primary of a power transformer is connected to the DC source in series with a primary switching transistor. In operation, the transistor is driven into conduction for a controlled period of each cycle during which the current in the primary increases. During the remainder of the cycle, the transistor is non-conducting, but the energy stored in the primary inductance is transferred to four secondary windings. The secondaries each contain a semiconductor diode which provides half wave rectification.

2.3 The +5V, +12V and -12V outputs are derived from three separate windings which drive integrated circuit voltage regulators. These regulators are of the linear type.

SECTION II - DETAILED DESCRIPTION AND THEORY OF OPERATION

1. GENERAL

1.1 Operating Modes

1.1.1 During normal operation, the 430700 and 430780 Power Supplies Function as a fixed frequency, pulse width modulated switching regulator. However, whenever power is initially applied, the oscillator and control circuitry which are on the secondary side of the main power transformer, T1, are not operational. An auxiliary mode of operation is provided which is operational only during start-up while the oscillator and control circuitry are non-operating. In this auxiliary mode, the primary switching transistor is driven by an extra winding on transformer T1 which is connected such that positive feedback is provided to its base. This results in a blocking oscillator like mode of operation during start-up.

1.1.2 Operation of the Power Supply in the power-up mode results in energy transfer to the secondary windings so that the oscillator and control circuitry, which are powered from the unregulated voltage which drives the +12V Regulator, will commence operation. With a low secondary voltage, the control circuitry provides a maximum pulse width which is constrained to be slightly less than 50% of a cycle. Whenever the oscillator drive has gained sufficient amplitude to reliably drive the primary switching transistor, the blocking oscillator action is automatically terminated and operation continues under oscillator driven control.
1.2 Features

1.2.1 An RFI filter is included in the AC line input to reduce conducted interference resulting from the use of a switching regulator "Off-the-Line".

1.2.2 In-rush currents on start-up are controlled by the use of a series line resistance and by a current limited drive on start-up.

1.2.3 AC line transient protection has also been provided which both tends to limit peak voltages as well as suppress the transfer of the transient to the secondary circuits.

1.2.4 An Output voltage detector circuit is included which will light an LED indicator only whenever all four secondary output voltages are present, although not necessarily within tolerance. This indicator may be viewed for maintenance purposes without removal of the unit.

1.2.5 The +45V, +12V, and +12V logic voltages are protected against accidental load shorts. Upon removal of the short, the power supply will either recover or shut off. To reset following a shut off, input power must be removed for at least 15 seconds. The +45V output is also protected against print head driver shorts by means of a fuse in the output.

1.2.6 All outputs are protected against sustained overvoltages. Detecting circuitry monitors each output and in the event of a fault, the oscillator drive is immediately removed so that the secondary circuits are no longer powered. Reset is accomplished by removing input power for 15 seconds.

2. POWER UP MODE

2.1 AC Line Input (FS-1)

2.1.1 Nominal input voltage (115 VAC) is applied to connector J202. The hot side of the line is applied to terminal #1. Protective earth ground is applied to terminal #2, and line neutral to terminal #3 of J202.

2.1.2 An RFI filter, FL1, reduces conducted interference entering and leaving the power supply.

2.1.3 Thermistor RT1 and RT2 are in the hot side of the line to limit initial inrush current into capacitor C1. Initial resistance of RT1 and RT2 is 2.5 ohms each which after the supply is operational reduces to approximately 1.0 ohm due to self heating.

2.1.4 The transient protector RV1 is a voltage clamping device to limit the potential applied to primary circuits of the power supply. RV1 avalanches at approximately 150 VAC (RMS), limiting the voltage applied to other devices.

2.2 AC Line Rectifier

2.2.1 AC to DC rectification occurs through the full wave bridge consisting of the four diodes CR1, CR2, CR3 and CR4. Capacitor C1 filters the DC.

2.2.2 The anodes of CR3 and CR4 and the negative end of C1 are connected to a common bus for all primary circuits. This bus is not to be confused or connected with any ground bus on the secondary circuits unless the power supply is floated through an isolation transformer. Grounding of the primary bus might cause destruction of diode CR3, as well as thermistor RT1.

2.3 Blocking Oscillator Operation (FS-2)

2.3.1 Upon initial application of DC voltage to R3, current flows to charge C2. The time constant of R3 and C2 delays the start-up until capacitor C1 is fully charged.

2.3.2 The voltage across C2 biases the base of Q1 into the active region by applying DC potential through R8, terminal (J, H) of P2 and diode CR11. This causes current to flow into the base of Q1 tending to turn it on. As Q1 turns on, terminal L of P1 is forced toward primary bus common. Since coil P1 is tightly coupled to P2 an equivalent potential is applied across P2 according to the dot notation shown. R15 is a base bias resistor for Q1.

2.3.3 A portion of P2 is tapped at J to act as a source to further drive the base of Q1 toward saturation. Regenerative action occurs because of positive feedback driving Q1 into saturation.

2.3.4 Base drive into Q1 is limited by resistor R8. The Q1 collector current ramps up due to the magnetizing inductance of TL. This current is limited by the gain hFE of Q1. For constant current base drive, Q1 remains in saturation until IC exceeds hFE times Iβ.

2.3.5 As Q1 comes out of saturation voltage across J-H is reduced, lowering the base drive to Q1. Regenerative action occurs forcing Q1 off. Q1 remains off until the energy in TL collapses via dumping energy into the secondaries (S1, S2, S3, S4). The cycle then repeats itself until the pulse width modulator mode takes over.
2.4 Snubbing Circuit (PS-2)

2.4.1 The snubbing network consisting of coil P2 and diodes CR14 and CR12, clamp the collector of transistor Q1 during turn off to twice the DC supply voltage. During turn off terminal L of P1 exceeds the potential at terminal G due to the inductive kick of the transformer T1. The potential across terminals L-G is mirrored on terminals K-H by observing the dot notation polarity.

2.4.2 Upon turn off terminal K becomes more positive than +VDC in and is clamped by CR14. Terminal H becomes more negative than the +VDC bus common. This forces a clamping of coil P2 which reflects to coil P1 due to tight coupling. The voltage on the collector of Q1 is limited to that across P2 or twice VTN. Diode CR7 prevents capacitor C2 from being reversed biased.

3. OSCILLATOR DRIVEN MODE

3.1 20 KHz Square Wave Oscillator

3.1.1 During start-up, the secondaries of T1 receive a limited amount of power which results in an increasing rectified voltage. The oscillator is fabricated from one of the comparators in ML2 which derives its power from the regulated +12V supply. As the voltage increases to approximately 4 volts, oscillation commences.

3.1.2 If the oscillator output (Pin 2) has just switched to ground, the voltage at the non-inverting input (Pin 5) will be determined by the divider of R35 and R28 in parallel with R32. This voltage is 31% of the +12V supply. The voltage at the inverting input (Pin 4) discharges toward ground at a rate determined by R38 and C11. As this voltage drops to 31% of the +12V supply, the comparator output switches to the high state. Now, the voltage on Pin 5 is essentially determined by the divider of R28 in parallel with R35 and R32. This voltage is 62% of the +12V supply. The voltage at Pin 4 charges toward the +12V supply at a rate determined by R30 and R38 in series, and C11. As this voltage now reaches 62% of the +12V supply, the comparator output (Pin 2) switches to the low state.

3.1.3 Since the comparator switch points are a fixed ratio of the +12V supply, the frequency will be virtually independent of the actual voltage of the +12V supply. In fact, from approximately 4 to 40 volts, the frequency and duty cycle are essentially constant.

3.2 The Ramp Generator is fabricated from a second comparator of ML2. The inverting input (Pin 8) of ML2 is biased to approximately 50% of the +12V supply by a divider composed of R33 and R36. The output of the 20kOhm Square Wave Oscillator is connected to the non-inverting input (Pin 9). Whenever the oscillator output is low, the output (Pin 16) is held low in the high state. The voltage on capacitor C10 is held low during this time.

3.2.2 Whenever the oscillator output goes to the high state, the output of the ramp generator is unclamped. The voltage on C10 begins to charge toward the +12V supply by means of resistor R29. The voltage reaches approximately 3.5 volts during the time that the oscillator output is high. Whenever the oscillator output goes to the low state, C10 is discharged and the ramp voltage goes to a few tenths of a volt above ground.

3.3 Pulse Width Modulator (PS-4)

3.3.1 A third section of ML2 is used for a Pulse Width Modulator. The output of the ramp generator is connected to the non-inverting input (Pin 11) by means of resistor R39. The inverting input (Pin 10) is connected to a divider network consisting of R67 and R46 which derives a bias of approximately 0.6 volt from the +12V supply.

3.3.2 In the absence of any output from Pin 9 of ML3, the bias voltage of 0.6 volt appears on Pin 10 of ML2. Consequently, whenever the ramp generator output is low, the pulse width modulator output (Pin 13) will be low shunting any current flowing through R64. Whenever the ramp generator output exceeds the bias voltage, the pulse width modulator will go to a high state. Any current flowing through R68 will now be available to drive the base of transistor Q10.

3.3.3 CR21, 4 layer diode is connected to the +12V supply through resistor R66. This diode is non-conducting until the +12V supply exceeds approximately 8 volts, at which point the diode triggers into conduction with a drop of approximately 0.7 volt. During start-up, even though the oscillator is running and the pulse width modulator producing drive pulses, transistor Q10 will not receive drive pulses until CR21 becomes conducting.

3.3.4 Whenever an output is produced on Pin 9 of ML3 that exceeds the 0.6 volt bias, the pulse width of the output on Pin 13 of ML2 will be reduced. The pulse width modulator output will be in the high state for the time that the ramp generator output exceeds the voltage produced on Pin 9 of ML3.

3.3.5 Resistor R40 is connected between the ramp generator output and the non-inverting input to provide hysteresis and snap-action switching. Resistor R41 provides a base leakage path for transistor Q10.

3.4 Voltage Reference and Error Amplifier (PS-4)

3.4.1 The voltage reference and error amplifier is contained in ML3, a Type 723 Precision Regulator. The voltage reference, Upp (Pin 6), is nominally 7.15 volts with a ±5% tolerance. This voltage is applied to a precision divider consisting of R37 and R45 to provide a 3.57 volt reference which is applied to the inverting input (Pin 4) of the error amplifier.
3.4.2 The +42 volt rectified DC output is connected to a precision divider consisting of R49 and R50. The resulting voltage is applied to the non-inverting input (Pin 5) of the Error Amplifier. In operation, the voltage at Pin 5 is very close to that at Pin 4. Frequency compensation of the Error Amplifier is accomplished by connection of capacitor C15 between the compensation terminal (Pin 13) and the inverting input (Pin 4).

3.4.3 The DC gain of the Error Amplifier, ML3, is utilized to produce the control signal at Pin 9. Gain of the Error Amplifier is reduced by use of negative feedback from the direct output at Pin 10 through resistor R46. Capacitor C17 is used to by-pass any high frequency noise in proximity to the Error Amplifier.

3.5 Primary Power Conversion

3.5.1 As previously noted, the 20 KHz Oscillator will commence operation and produce drive pulses to the base of transistor Q10 whenever the +42V supply exceeds approximately 8 volts. At this point, the pulse transformer T2, in the collector of Q10 will be driven so as to produce a positive pulse of similar duration on its secondary. This pulse is connected through resistor R18 and diode CR10 to the base of the primary switching transistor, Q1.

3.5.2 The positive drive on the base of Q1 causes current to flow in the collector of Q1 and the primary winding (PM) of transformer T1. The current increases, linearly during the duration of the pulse, from its initial value to its final value which is dependent upon the pulse width as well as the DC supply voltage. Diode CR13 effectively prevents Q1 from reaching full saturation, reducing the storage time for Q1.

3.5.3 The positive pulses are also connected through diode CR9 which rectifies the signal to produce a DC signal on capacitor C4 and bleeder resistor R13. When the power supply begins operating in the oscillator driven mode, the DC signal is connected through diode CR8 and resistor R9, to the base of transistor Q1. The collector of Q1 is connected to the feedback winding used to provide the blocking oscillator action. Turning Q7 on will short the signal produced by the feedback winding and effectively inhibit blocking oscillator action. This control is automatically transferred from the start-up mode to the oscillator driven mode.

3.5.4 Whenever the drive to the base of Q10 is shutted by the Pulse Width Modulator, the drive pulse is terminated. The collector of Q10 rises from the saturated value of Q10 to a voltage above the +16V supply. This results in a negative pulse on the secondary of T2. This pulse is connected through resistor R22 to the base of transistor Q5. Transistor Q5 is turned on which effectively grounds the base of Q1. The stored base charges in Q1 is discharged through Q5 resulting in rapid turn-off of Q1.

3.5.5 When Q1 turns OFF, the energy which was stored in the magnetic core of T1, is transferred to the secondary windings. Each winding is driven in proportion to its relative turns ratio.

3.6 Feedback Regulation (FS-4)

3.6.1 As DC line power is transferred to the secondary circuits, the rectified secondary voltages increase. The +42V supply is sensed by means of diodes R49 and R50 and compared in the Error Amplifier with the voltage reference derived by divider R37 and R42. Whenever the sensed voltage exceeds the reference voltage, the Error Amplifier output (Pin 9) is increased which has the effect of reducing the pulse width supplied to drive Q1. As a result, the net energy transferred to the secondary is reduced. This also causes the rectified secondary voltages to decrease. Consequently, the +42V supply is regulated against line and load changes. In addition, the remaining three secondaries are also regulated against line changes and to some extent, load changes, to the degree that they are reflected in the +42V supply voltage.

3.6.2 The +42V supply is derived from a secondary winding of T1. The voltage on winding S1 is half-wave rectified by diode CR17 and filtered by capacitor C13. A bleeder resistor R26 is provided to discharge C13. L1 and L2 are added in the +407BD power supply to reduce EMI emissions. 3.6.3 The +42V supply is connected through fuse F1, a 1 amp fast acting device, to terminals 1 and 3 of connector J201. The return for the +42V supply is made through terminals 9 and 10 of J201. It is also connected to the logic supply secondary return.

3.7.1 The purpose of the optical coupler is to deactivate the blocking oscillator mode of operation following a normal start-up sequence, or upon detection of a +42V over-voltage condition. Over-voltage is detected by Diode CR20, Resistor R27, and ML1 Optical Isolator Diode. Under light loads, the secondary voltages may substantially exceed their ratings during this condition. The over voltage protective circuitry which functions by inhibiting the clock is not capable of inhibiting the blocking oscillator action.

3.7.2 Whenever the +42V supply voltage exceeds approximately 47 volts, a second diode, CR29 will conduct and drive the LED in optical isolator ML1. Resistor R27 limits the current through the diode.

3.7.3 The phototransistor in ML1 in conjunction with transistor Q3 forms a latch on the AC line side of the power supply. Whenever the latch is OFF, a voltage appears on the emitter of Q3 which is the result of a fixed drop across the zener diode CR5, and a divider consisting of R3 and R6. Capacitor C3 filters noise appearing on the emitter. As secondary voltages are developed by blocking oscillator action, a transition to the oscillator driven mode generates Positive Pulses at T2 transformer terminal 4, which are coupled to Q3 base and to the Phototransistor Pin 6, through CR9, R10 and R11. The Phototransistor conducts current thru resistor R12 which is connected to the base of Q3. This base current causes collector current to flow thru Q3 which, in turn, drives the base of the Phototransistor by means of resistor R11. Transistor Q3 becomes latched so that in the event of a failure in the oscillator control circuit, transistor Q7 will continue to be driven, which prevents the blocking oscillator from re-starting. Resistor R16 provides base stabilization for the Phototransistor, and capacitor C3 filters noise transients to prevent spurious triggering of the latch.
3.7.3 Zener diode CR5 is provided to permit the latch to clear whenever the rectified primary DC voltage drops below approximately 50 volts. This allows the power supply to automatically restart under the blocking oscillator mode of operation if the oscillator driven mode has also become inoperative.

3.8 Primary Circuit Overcurrent Protection (FS-2)

3.8.1 A resistor, R4, in the emitter of the primary switching transistor, Q1, senses the current conducted during each pulse drive period. If this current should exceed a safe level, the base drive current is shunted for the remainder of that drive pulse.

3.8.2 The voltage developed on R4 is applied through resistor R19 to capacitor C6 which acts to filter spurious transients, to R17 which is in series with the base of transistor Q8, and to the base of transistor Q4. Whenever the voltage developed is high enough to cause Q8 to conduct sufficient current through the collector resistor, R20, which is connected through diode CR13 to the drive pulse transformer T2, to bias transistor Q9 into conduction, a regenerative action is initiated. This allows current to flow through the emitter resistor, R21, of Q9. The current drives both the base of Q8 and the base of Q4. Whenever Q4 conducts, the base drive current to Q1 is shunted to the primary common, effectively terminating the primary switching transistor current pulse for that cycle. Whenever the drive pulse from transformer T2 terminates, transistors Q8, Q9 and Q6 are returned to their non-conducting state.

3.9 Primary Circuit Overvoltage Protection (FS-4)

3.9.1 In the event that a transient spike occurs on the AC line that exceeds the normal voltage range, circuitry has been provided which will maintain the primary switching transistor in the non-conducting state even through base drive pulses are being generated. This protection is accomplished by shunting the oscillator drive pulse during the transient.

3.9.2 Zener diode CR6 cathode is connected to the primary DC power, and anode to resistor R8. Whenever the DC voltage is high enough to exceed the zener diode voltage, current flows to the base of transistor Q2 by means of resistor R7, and the base of Q6 by means of resistor R15. Base bias resistor R5 serves to bypass leakage current for both Q2 and Q6.

4. LOGIC VOLTAGES (FS-3)

4.1 +5V Supply

4.1.1 The +5V supply is derived from a secondary winding of T1. The voltage on winding S4 is half wave rectified by diode CR16 and filtered by capacitors C7 and C18. This unregulated voltage, +9V, is applied to the base connection (B) of a linear regulator, ML5, which is a self-contained three terminal integrated circuit located on a common heat sink with ML6 and ML7. A capacitor, C19, on the output (E) of the regulator filters high frequency load transients.

4.1.2 The +5V supply is connected to terminals 5 and 6 of connector J201 on the power supply. Logic supply return is connected to terminals 9 and 10.

4.2 +12 Volt Supply

4.2.1 The +12V supply is derived from a secondary winding of T1. The voltage on winding S2 is half wave rectified by diode CR19 and filtered by capacitors C9 and C23. This unregulated voltage, +16V, is applied to the base connection (B) of a linear regulator, ML7, which is a self-contained three terminal integrated circuit located on a common heat sink with ML5 and ML6. A capacitor, C22, on the output (E) of the regulator filters high frequency load transients. The +16V supply is also used to drive the Error Amplifier.

4.2.2 The +12V supply is connected to terminal 7 of connector J201.

4.3 -12 Volt Supply

4.3.1 The -12V supply is derived from a secondary winding of T1. The voltage on winding S3 is half-wave rectified by diode CR18 and filtered by capacitors C8 and C21. This unregulated voltage, -16V, is applied to the collector connection (C) of a linear regulator, ML6, which is a self-contained three terminal integrated circuit located on a common heat sink with ML5 and ML7. A capacitor, C20, on the output (E) of the regulator, filters high frequency load transients.

4.3.2 The -12V supply is connected to terminal 8 of connector J201.

5. OUTPUT VOLTAGE INDICATOR (FS-3)

5.1 The +16 volts from the output of T1 transformer will turn on the L.E.D. indicator CR28 through R54.
6. FAULT PROTECTION ON SECONDARY

6.1 Short Circuit Protection

6.1.1 The +5V, +12V and -12V supply outputs are protected against short circuits to ground by means of the current limiting characteristics inherent in the integrated circuit voltage regulator which is in each of these outputs. Fault currents are limited to approximately 1.5 amperes. Whenever the fault is removed, the output voltage will either recover or shut off.

6.1.2 These regulators are also thermostatically protected so that in the event that their power dissipation in conjunction with the ambient temperature exceeds their limit, automatic shutdown occurs. Whenever the internal temperature decreases to a safe level, the device will reset and restore the output voltage.

6.1.3 The +42V supply is protected against overloads on the output by means of a 1 amp fast blow fuse, F1. Whenever this fuse opens, the Output Voltage Indicator will go dark even though the supply is otherwise functional.
CIRCUIT DESCRIPTION OF THE M#3 LOGIC CARD
410740-42 (BASIC KSR)

TABLE OF CONTENTS
CIRCUIT DESCRIPTION OF THE M#3 LOGIC CARD
410740-42 (BASIC KSR)

SECTION I - GENERAL TECHNICAL DATA
1. GENERAL DESCRIPTION
   1.1 The Basic M#3 Logic Card serves a threefold purpose in the M#3 Basic
       KSR. It provides the control logic for the operator console, line interface
       and printer functions; it provides the drivers for the printer mechanism;
       and it serves as a harness card into which all the printer subassemblies
       are connected.

   1.2 The Basic Card controls all information flow among the three terminal
       subassemblies - operator console (OPCON), line interface (TAI/TDU) and
       printer. It retains the present terminal state (e.g., LOCAL/TALK) and
       determines each new terminal state from incoming OPCON or TAI/TDU information.
       Three terminal modes are possible, namely Local, Terminal Ready or Data.

   1.3 The Basic Card also provides all the necessary timing and drive levels
       to cause proper operation of the various printer subassemblies.

   1.4 The 410740 and 410742 Basic Logic Cards are identical except as
       follows:

<table>
<thead>
<tr>
<th>LOGIC CARD</th>
<th>MACON (MLC4)</th>
<th>STRAP TO PROVIDE SPEED CONTROL ON OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>410740</td>
<td></td>
<td>NOT PRESENT</td>
</tr>
<tr>
<td>410742</td>
<td></td>
<td>ADDED TO CARD</td>
</tr>
</tbody>
</table>

Sheet 1

Sheet 2
2. FEATURES

2.1 Basic ESR Operational Features

The Basic Card, when part of the basic ESR set, can perform a number of operator accessible features activated from either OPCON or TAU/TDU data streams.

2.2 Set Configuration Features

An 8 position DIP switch pack is provided to configure the terminal for certain optional functions.

2.2.1 Printer Related Options

Two switches select maximum printer line length. The options available are 72, 80, and 132 column line lengths.

Two switches select graphic character font. The options available are TV, HE, and MU fonts.

2.2.2 Line Interface Related Options

One switch enables the automatic new line feature. This feature insures no loss of data received from the TAU/TDU in the event of improper line formatting.

One switch enables the sending of even parity to the TAU/TDU. When disabled the parity bit is forced marking.

One switch enables automatic disconnect of a call upon receipt of the ASCII EOT character.

2.2.3 Maintenance Related Option

One switch enables a printer test feature, causing the printer mechanism to continuously print its selected character font.

3. SWITCH OPTIONS

3.1 The following convention is used in the schematic wiring diagram and circuit description to designate each switch.

SPDA-SW4

SP = Refers to switch pack,
D4 = Refers to location D4 on the card assembly,
SW4 = Refers to the fourth switch of package SPDA.

3.2 Detailed Description

ON - Switch Closed (SW1 is always oriented toward center of card.)
OFF - Switch Open

<table>
<thead>
<tr>
<th>Designation</th>
<th>Function</th>
<th>Switch State (To Enable Function)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW1</td>
<td>Automatic New Line</td>
<td>OFF</td>
</tr>
<tr>
<td>SW2</td>
<td>Printer Test</td>
<td>ON</td>
</tr>
<tr>
<td>SW3</td>
<td>Vertical Parity Send</td>
<td>OFF</td>
</tr>
<tr>
<td>SW4</td>
<td>EOT Disconnect</td>
<td>OFF</td>
</tr>
<tr>
<td>D4</td>
<td>Line Length Select</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SW5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SW6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>72 Columns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 Columns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>132 Columns</td>
</tr>
<tr>
<td>SW7</td>
<td>Character Font Select</td>
<td>SF7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SW8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MU Font</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Undefined</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TV Font</td>
</tr>
</tbody>
</table>

4. SUPPORTING INFORMATION

NM3 Logic Board Schematic - 4740SD
OPCON Schematic, Circuit Description - 4080SD, 4080CD
Print Head Schematic - 4013SD

SECTION II - DETAILED DESCRIPTION

1. GENERAL

1.1 The voltage and current requirements of the 410740 AND 410742 CARDS ARE AS FOLLOWS:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Voltage Range</th>
<th>Avg. Current Drain</th>
</tr>
</thead>
<tbody>
<tr>
<td>+42V</td>
<td>+37.8V to +46.2V</td>
<td>1.0A (with printer load)</td>
</tr>
<tr>
<td>+12V</td>
<td>+10.8V to +13.2V</td>
<td>850 ma</td>
</tr>
<tr>
<td>+5V</td>
<td>+4.5V to +5.5V</td>
<td>550 ma</td>
</tr>
<tr>
<td>-12V</td>
<td>-13.2V to -10.8V</td>
<td>150 ma</td>
</tr>
</tbody>
</table>

Communications Interface

1.2 Other supply voltages developed on the card from the -12V supply have the following tolerances:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Voltage Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>-4V</td>
<td>-4.6V to -3.4V</td>
</tr>
<tr>
<td>-5V</td>
<td>-5.5V to -4.5V</td>
</tr>
</tbody>
</table>
2.3 The Printer Timing Logic (FS-3) controls all printer functions. It
receives parallel data from the Terminal Controller, decodes it and performs
the corresponding operation. The basic printer functions are character
print, carriage return, line feed, backspace, bell, margin set, margin clear
and margin release.

2.4 Functional blocks FS-3 and FS-4 contain the power devices which drive
the electromechanical subassemblies comprising the printer mechanism.

3. THEORY OF OPERATION

3.1 FS-1 Terminal Controller (See TO-1 Timing Diagram.)

3.1.1 General - Functional block FS-1 interfaces the 743 logic card to the
set of 740 and the TAU/TDU. It also provides the input data to the printer
timing logic and senses various switches for features and options.

3.1.1.1 The 410740 Card does not provide for an auxiliary port. It is used
with the TAU1 (410735 Terminal Auxiliary Unit) or TDU (410750 Terminal Data
Unit), or TTL Interface.

3.1.1.2 The 410742 Card provides for an auxiliary port. It is used with
the TAU2 (410754 Terminal Auxiliary Unit) or TTL Interface. The additional strap
between J107-17 and P301, Pin 4 provides a speed select signal output. A high
(+) signal output indicates 30 cps is selected and a low (0V) indicates
10 cps is selected.

3.1.2 OPCON Interface - Both a serial and a parallel data interface exist
between OPCON and logic board. The serial interface consists of a 560 Bits
clock, a repeat mode signal and a serial data signal. The repeat mode
signal (J107 pin 7) is active (character repeating) in the high state (VH)
and inactive in the low (VH). The serial data lead (J107 pin 6) is normally
marking at Vh. The transmission code used on this lead consists of eleven
bits - one start bit, eight data bits, one parity bit and one stop bit. The
spacing level is Vh. One bit time = 143 microseconds.

The B-C filters (R42, C14 and R43, C15) are present to minimize
noise picked up on the interface cable.

The parallel data interface consists of five DC contact switch leads
(J107 pins 14, 17, 18, 19, 20) and five LED drive signals (J107 pins 5, 9,
10, 11, 13).

The DC contact switches when depressed (closed) apply ground to the
respective inputs of a 7417 open collector buffer (ML23). When released
(open), 6.8K resistors (RP3) pull the buffer inputs to Vh. These buffers
in turn drive the MACON pack (ML04 - 8, 24, 25, 27, 31) with the non-inverted
switch state. Vh will be present on the corresponding ML04 pin when the
associated switch is open and Vh will be present when the switch is closed.

The printer test signal (ML04-24) is provided with an on-board DC
contact switch (SPFD-S12), wired 'ANDed' with ML23-4, that can enable printer
test independent of the OPCON.

The five LED drivers in MACON (ML04-36 thru 38) pull their respective
leads to Vh when activating an LED. The 1K resistors (R37-R64) limit the
LED forward current to 15 ma nominal.
3.1.3 Eleven parallel data leads (MLEO-9 thru 19) interface the MACON logic pack with the printer timing logic. The eight data leads transmit coded information to the printer timing logic. \( V_H \) represents a binary 1(0).

The Request Next Character signal (MLEO-19) is an input which goes to \( V_H \) when the printer timing logic is ready to accept more information. Otherwise it remains at \( V_L \).

The Load Data Printer signal (MLEO-9) drives momentarily (\( >2 \) microsec) to \( V_H \) when information is to be transferred (via data leads) to the printer timing logic. The trailing edge of this pulse causes Request Next Character to be set to \( V_L \).

Right Hand Margin is a bi-directional signal which, during normal operation, is an input to MACON (MLEO-19). This signal goes to \( V_H \) coincident with Request Next Character whenever the print mechanism is at the right hand margin. This signal is driven to \( V_H \) by MACON (MLEO) whenever the power is turned on with the interlock switch (J107 pin 14) open and the TEST SWITCH is not activated. It remains at \( V_L \) until the interlock switch is depressed.

3.1.4 The TAU/TDU interface is comprised of six lines from the MACON (MLEO) pack.

Two control lines provide the normal interface control to the line interface. Terminal Ready (MLEO-3) is active when driven to \( V_H \) by MACON, TAU/TDU Ready (MLEO-6) is active when driven to \( V_H \) by MLEO-4.

Two data lines provide the bi-directional asynchronous serial data path. Send Data (MLEO-39) is marking (spacing) when driven to \( V_H \) by MACON. Receive data is marking (spacing) when driven to \( V_H \) by MLEO-4.

Two test signals are provided for maintenance testing. Both Digital Loop (MLEO-5) and Analog Loop (MLEO-6) are active when driven to \( V_H \) by MACON.

A seventh signal, Duplex, is provided at the TAU/TDU interface for future use. It is identical to the signal on MLEO-31 except that no pullup to \( 45 \) is provided on the card.

3.1.5 Paper Out and Low Paper switches are connected to the logic card through J101. Each switch drives a 7417 buffer (MLEO-3, 5) with 9.8k input pullup resistors (R3, R6). The 7417 buffer drives MACON (MLEO-22, 28) to \( V_H \) when the corresponding switch is closed. Internal resistors in MACON pull these leads to \( V_L \) when the corresponding switch is open.

3.1.6 Three option switches (SPDN-SU1, SW3, SW4) are provided for Terminal Controller options.

When a switch is open the associated pin on MACON (MLEO-23, 26, 30) is pulled to \( V_H \). Closing the switch applies logic ground to the corresponding MACON pin.

3.2 PS-2 Printer Timing Logic (See TC-2 and TC-3 Timing Diagrams.)

3.2.1 General - Functional Block PS-2 receives 8 bit parallel information from the Terminal Controller and in turn generates all the necessary timing to produce the corresponding printer function. This functional block also provides the supply clock for the 4433 Basic SCR.

3.2.2 System Clock - The clock circuit consists of a crystal controlled oscillator and a divide-by-2 squaring circuit with power-on gating.

One half of the NOR gate pace (MLEI) provides the amplifier section for a series resonant oscillator circuit with a 1.12 MHz crystal in the feedback path. The output at MLEI-2 is buffered by another NOR gate with a disabling input (MLEI-12) provided for testing purposes. In normal operation resistor R46 keeps this gate enabled.

One flip-flop of a 74109 Pack (MLE2) is connected as an RS latch (not clocked). The presence of C20 on the CLEAR input (MLEO-15) sets this latch (MLEO-10) at \( V_H \) on power turn on. Approximately 100 microsec later C20 will have charged positive enough to reach the NOR gate input threshold (MLEI pins 4, 5) causing the latch preset (MLEO-11) to switch to \( V_H \) and setting MLEO-10 to \( V_H \) where it remains till power is removed. This circuit prevents erratic operation of the clock line during the power-up mode, when the oscillator is starting.

The second flip-flop of the 74109 pack is connected to divide the clock signal (from the oscillator) by two when the 'J' input (MLEO-2) is at \( V_H \). This gives a symmetric 560 Hz clock at MLEO-6 which swings from \( V_H \) to \( V_L \). Pullup resistor R36 is needed to attain this positive level. When the J input is at \( V_H \) the flip-flop output (MLEO-6) will be set to and remain at \( V_H \).

3.2.3 Terminal Controller Interface - Eleven parallel data lines interface the MLEO (MLEO) logic pack with the Terminal Controller (FS-1). These lines operate as described in Section 3.1.3.

3.2.4 Four option switches are provided for printer options. SPDN-SU7 and SW5 select one of three character fonts. SPDN-SU3 and SW6 select one of three line lengths.
3.2.5 Left Margin Sensor - A DC contact switch is provided on the print head assembly which, when depressed (open), allows the input of a 7417 buffer (MNC7-26 pin 9) to be pulled to \( V_{IH} \) by R13. The 7417 output transistor turns off and the MAPL Left Margin signal (MNC7-17) is internally pulled to \( V_{IH} \), indicating that the print mechanism is in the left margin position.

3.2.6 Velocity Encoder - This circuit is comprised of an optical switch, feedback amplifier and hysteresis amplifier which produce a pulse train with repetition rates proportional to the average carriage motor rotor velocity.

The phototransistor section of the optical switch (FS-2, A1) is connected in a common collector configuration. The emitter (J103 pin 1), with load resistor R3 drives both the feedback amplifier through R6 and the hysteresis amplifier (MNC8-9).

The feedback amplifier with elements R6 and C1 serves as both a low pass filter and current amplifier capable of driving the light emitting diode of the optical switch.

As the optical switch beam is interrupted by a rotating disk mounted on the carriage motor shaft, voltage pulses of approximately 600 microsec period and 1V to 3V peak-to-peak amplitude are developed at (MNC8-9). This repetition rate is too fast for the feedback amplifier (with low pass filter) to respond to, so no correction is made for this signal. However, all slower variations (including DC offsets due to parameter variations) are cancelled out by the action of the feedback amplifier driving the optical switch LED. Consequently, the desired velocity dependent signal is present at the output of the hysteresis amplifier (MNC8-9) centered about \( V_U \).

The hysteresis amplifier, with approximately 100 mV hysteresis, amplifies this input signal, supplying a velocity dependent pulse train to the MAPL pack (MNC7-18). This signal swings from \( V_{IH} \) to -5V (-1V, +5V).

3.2.7 Print Mechanism Driver Interface - Nine leads from the MAPL pack (MNC7-31 thru 39) supply the print commands to the nine print mechanism coil drivers. When a print command is to be given, MAPL drives the desired print level lead(s) to \( V_{IH} \) for a pre-programmed time. (See TC-2 timing diagram.)

3.2.8 One lead from the MAPL pack (MNC7-30) supplies the input to the bell driver. This lead is driven to \( V_{IH} \) for the duration of time required to ring the bell.

3.2.9 Line Feed Motor Driver Interface - Four leads from the MAPL pack (MNC7-26 thru 29) supply the stator timing for the four line feed motor phases. A fifth lead, the clamp switch (MNC7-21), controls a variable clamp in the kickback circuit of the phase 1 coil. To energize a stator coil MAPL drives the appropriate lead to \( V_{IH} \). (See TC-3 Timing Diagram.)

3.2.10 Carriage Motor Driver Interface - Four leads from the MAPL pack (MNC7-22 thru 25) supply the stator timing for the four carriage motor phase. To energize a stator coil MAPL drives the appropriate lead to \( V_{IH} \). (See TC-2 for typical stator timing during printing.)

7.3 FS-3 Print Head and Bell Drivers

3.1.1 General - Each print head driver consists of a CH05 pre-driver and Darlington power driver. The bell driver consists of a Darlington power driver only.

3.3.2 When the bell driver input (Q20-B) is driven to \( V_{IH} \) by MAPL the collector (Q20-C) goes to 1.5V nominal, driving approximately 175 ma through the bell coil. When MAPL releases the input, R26 pulls Q20-B to ground turning off the driver. Inductive kickback from the bell coil attempts to drive Q20-C highly positive. C32 however clamps the collector preventing it from going more positive than 43V nominal.

3.3.3 When a print level pre-driver (NL65, A7 or E8) input is driven to \( V_{IH} \) by MAPL, it in turn drives the base of its associated power driver (Q11-Q19) to \( V_{IH} \). The power driver then turns on to \( V_{IH} \) causing a current pulse in the associated print head coil. When MAPL releases the input, the pull down resistor (R27 through R35) brings the pre-driver input to \( V_{IH} \) causing the pre-driver to pull the associated power driver base to \( V_{IH} \), turning off the driver. The collector voltage rise due to the inductive kick of each head coil is clamped by diodes CR16 thru CR25 to 43V nominal.

3.4 FS-4 Line Feed Motor and Carriage Motor Drivers

3.4.1 General - Each driver for both the line feed and carriage motor coils consist of a CH05 pre-driver and Darlington power driver. In addition the line feed motor circuit contains a Darlington switch across the phase 1 coil to provide hard clamping of the inductive kick during the idle condition.

3.4.2 Line Feed Motor Circuit - To energize stator coil 4 (J102-1) MAPL drives the corresponding pre-driver input (NL65-9) to \( V_{IH} \), which in turn drives the associated power driver base (Q1-8) to \( V_{IH} \). This turn on the power driver to \( V_{IH} \) = 1.5V nominal causing current flow in the stator coil.
When the line feed mechanism is idle, MAX releases the clamp switch (MLAB-2) to Vgs. MLAB-6 drives G6 into saturation. This is turn pulls enough base current through R11 to turn on Q5. With Q5 on, stator coil is hard clamped (via C21 and Q5) to 6.4V nominal. During this idle state, the phase 1 drive signal is pulse width modulated at a 20 KHz rate. In conjunction with the hard clamp this provides a low level recirculating current in coil 1, keeping the motor in a detented position.

When stopping the line feed motor, MAX releases the clamp switch input which then is pulled to Vgs by R7. This causes Q6 and thus Q5 to turn off. In this condition, the clamping network for coil 1 is identical to that described above for the other coils.

3.4.3 Carriage Motor Circuit - The pre-driver and driver circuits for each stator coil (J104-1, 2, 3, 4) operate as described in 3.4.2 for the line feed motor. The coils are again zener clamped as described for the line feed motor. However, the zener in this case is in parallel with resistors R8 and R9, which help the zener dissipate the kickback energy. Because of this kick voltage, the zener clamp will remain below the zener clamp voltage till the current operates. The transistor is turned off for the duration of the interruption and provides a delayed Vgs potential only after the return of Vgs to 4.25 ± 0.250V. This delayed Vgs potential from Vgs and Vgs will force both MAX and NADCON into their respective POR routines.

3.5 PS-5 Voltage Distribution

3.5.1 The power on reset circuit is intended to function during two power states: a) At Vgs power up time it will provide a delayed Vgs potential and will ensure that the Vgs power supply has reached 4.25 ± 0.250V before turning Vgs on. b) At Vgs power interruption, Vgs = 4.25 ± 0.250V, the circuit will turn Vgs off for the duration of the interruption and provide a delayed Vgs potential only after the return of Vgs to 4.25 ± 0.250V. This delayed Vgs potential from Vgs and Vgs will force both MAX and NADCON into their respective POR routines.

Precision resistors Rg9 and Rg8 form a voltage divider which determines the voltage at which Vgs must be before MLAB-1 will switch states. Based upon the assumption that Vgs holds slightly longer or preceding Vgs, the Vgs trip voltage is set at 4.25 ± 0.250V. The power up sequence is as follows: Vgs (-75V) precedes or is coincident with Vgs (50V) which causes MLAB-1 to track the rising positive supply voltage. Vgs then causes the emitter of Q21, Vdp, to also track the rising Vgs voltage (Vgs = 0.95x[D76R31]). At such time Vgs reaches 4.25 ± 0.250V, the timing network of R33, C33, and C33 continues to hold the plus input voltage.

Capacitors C5 are a filter on the -42V used to average out the pulses energy requirements of the print mechanism.
### Sheet Index and Issue Control

**Sheet 1**

**Circuit Description of the**

61078 ASSY

M63 Terminal Auxiliary Unit (TAU 2)

<table>
<thead>
<tr>
<th>Revisions</th>
<th>Sheet Number</th>
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</thead>
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<td>Date</td>
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<tr>
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<td>10-20-78</td>
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**Sheet 2**

**Circuit Description of the**

61078 ASSY

M63 Terminal Auxiliary Unit (TAU 2)

<table>
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<th>Revisions</th>
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</tr>
<tr>
<td>1</td>
<td>10-20-78</td>
</tr>
</tbody>
</table>
SECTION I - GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 410754 Terminal Auxiliary Unit (TAU 2) card assembly serves as an interface between the Model 43 Keyboard Printer unit and external apparatus. The TAU 2 contains two interfaces; namely, a Line I/O and an Auxiliary I/O performing the following functions:

1.1.1 The Line I/O provides the necessary signalling and control conforming to EIA Standard RS 232C for operation with Bell System type 1C7 or 113 Data Sets to facilitate data exchange on a serial basis.

1.1.2 The Auxiliary I/O is EIA like that facilitates interfacing (the Keyboard Printer unit) to a local send/receive device such as a tape send/receive unit.

1.1.3 The Line and Auxiliary I/O also contain isolated send/receive 20/60 mA current interfaces that permit serial exchange of data to a remote or local send/receive unit having D.C. current interfaces.

1.1.4 It provides logic to control the respective interfaces.

1.1.5 The 410754 circuit card assembly is an integral part of the Model 43 set and is mounted in the rear of the unit. It is designed to operate in conjunction with a 410742 printer logic card.

2. GENERAL TECHNICAL DATA

2.1 Inputs and Outputs

The Inputs and Outputs can be segregated into four categories; namely, Terminal, Line or Data Set, Auxiliary, and Current I/O. See Figure 1.

2.1.1 Terminal Interface

2.1.1.1 The Terminal Interface consists of thirteen I/O leads of which seven are control leads, two are data leads, three are power input leads, and a logic ground lead.

2.1.1.2 The leads are terminated in a 20 pin male connector. Refer to Table 1-1.
2.1.1.2 (Continued)

TABLE 7-1
TERMINAL I/O
CONNECTOR - J301
LEAD DESIGNATION

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>DESCRIPTION</th>
<th>ABBR.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DATA SPEED INDICATOR</td>
<td>DSI</td>
</tr>
<tr>
<td>2</td>
<td>CHARACTERS PER SECOND</td>
<td>CPS</td>
</tr>
<tr>
<td>3</td>
<td>TERMINAL READY</td>
<td>TR</td>
</tr>
<tr>
<td>4</td>
<td>+5V</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>LOGIC GROUND</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>REQUEST TO SEND AUX (NOT TTL)</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>-12V</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>RING INDICATOR (NOT TTL)</td>
<td>RI</td>
</tr>
<tr>
<td>9</td>
<td>DUPLEX HALF/FULL</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>TAU READY</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>RECEIVE DATA</td>
<td>RD</td>
</tr>
<tr>
<td>12</td>
<td>SEND DATA</td>
<td>SD</td>
</tr>
</tbody>
</table>

2.1.1.3 Electrical Characteristics

The interface is compatible with low power TTL logic conforming to the following characteristics:

<table>
<thead>
<tr>
<th>STATE</th>
<th>DRIVER</th>
<th>TERMINATOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>MARK (OFF)</td>
<td>4.2 to 5.25V</td>
<td>4.2 to 5.25V</td>
</tr>
<tr>
<td>SPACE (ON)</td>
<td>0 to +0.4V</td>
<td>0 to +0.7V</td>
</tr>
</tbody>
</table>

Open terminator input condition - An open circuit input on a terminator of the interface is a MARK or Control Off condition.

2.1.1.4 Description of Terminal I/O Leads - Connector J301

a. Data Speed Indicator - Pin 2

To Terminal: Data Speed Indicator, when in the on condition, indicates to terminal that the data set is operating at 300 WPM. When in the off condition, the data set is operating at 100 WPM.

b. Characters Per Second - Pin 4

From Terminal: This signal is used to select auxiliary device baud rate whereby a high (1) selects a 30 character per second - 10 unit code and a low (0) is 10 characters per second 11 unit code.

c. Terminal Ready - Pin 5

From Terminal: A signal when "ON" allows the associated data set to manually or automatically switch over to the communication channel. The Terminal Ready signal indicates unit's capability to communicate on line.

d. Request To Send AUX - Pin 10

To Terminal: Request to send is used by the N63 Answerback. This is an EIA signal (not TTL) which has no control over the TAU 2.

e. Ring Indicator - Pin 12

To Terminal: Ring Indicator is also used by the N63 Answerback. This is an EIA signal (not TTL) which has no control over the TAU 2.

f. DUPLEX (HALF/FULL) - Pin 14

From Terminal: An operator control signal from the Keyboard Printer unit indicating Full or Half duplex operation. A (1) or "OFF" condition indicates half duplex operation and a (0) or "ON" indicates Full Duplex.

 g. TAU Ready - Pin 15

To Terminal: A signal to the TAU 2 indicating that the associated Data Set is capable of sending or receiving data. When "OFF" the Data Set Ready (CO), Data Carrier Detector (CF), and Clear To Send (CB) signals from the Data Set are in the "OFF" state.
2.1.1.4 (Cont.)

h. Receive Data - Pin 17

To Terminal: Serial binary data appears on this lead from the Data Set, or the auxiliary receive terminal.

i. Send Data - Pin 19

From Terminal: Serial binary data derived from the Keyboard appears on this lead at the selected baud rates.

j. Power Inputs:

+5V ± 10% 150 mA max. - Pin 7
+12V ± 10% 35 mA max. - Pin 13
-12V ± 10% 20 mA max. - Pin 11

Logic Ground - Pin 9

The CC754 card utilizes above D.C. voltages that are supplied by the Terminal Power Supply via specified pins. CR1 and CR2 are in series with the -12V, +12V to protect the LI66 EIA drivers.

2.1.1.5 Description of Line or Data Set I/O Leads - Connector J302. Refer to Table I-2

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>DESCRIPTION</th>
<th>ABBR.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PROTECTIVE GROUND (AA)</td>
<td>TO</td>
</tr>
<tr>
<td>2</td>
<td>TRANSMITTED DATA (BA)</td>
<td>TD</td>
</tr>
<tr>
<td>3</td>
<td>RECEIVE DATA (BB)</td>
<td>RD</td>
</tr>
<tr>
<td>4</td>
<td>REQUEST TO SEND (CA)</td>
<td>RTS</td>
</tr>
<tr>
<td>5</td>
<td>CLEAR TO SEND (CB)</td>
<td>CTS</td>
</tr>
<tr>
<td>6</td>
<td>DATA SET READY (CC)</td>
<td>DS R</td>
</tr>
<tr>
<td>7</td>
<td>LOGIC GND/ND (AB)</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>DATA CARRIER DETECT (CT)</td>
<td>CD</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>DATA SPEED INDICATOR (SCF)</td>
<td>DSI</td>
</tr>
<tr>
<td>13</td>
<td>TRANSMITTER CURRENT INT.</td>
<td>TCI-</td>
</tr>
<tr>
<td>14</td>
<td>TRANSMITTER CURRENT INT.</td>
<td>TCI+</td>
</tr>
<tr>
<td>15</td>
<td>RECEIVE CURRENT INT.</td>
<td>RC I-</td>
</tr>
<tr>
<td>16</td>
<td>RECEIVE CURRENT INT.</td>
<td>RC I+</td>
</tr>
<tr>
<td>17</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>DATA TERMINAL READY (CD)</td>
<td>DTR</td>
</tr>
<tr>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>RING INDICATOR (CE)</td>
<td>RI</td>
</tr>
<tr>
<td>22</td>
<td>DEVICE CONTROL</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td></td>
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<tr>
<td>24</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

( ) EIA STANDARD RS 232C LEAD DESIGNATION

The Data Set inputs and outputs comply with EIA Standard RS232-C whereby a signal level of +3 to +15V volts is a "space" or Control "ON" condition and a level of -3 to -15 volts is a "mark" or Control "OFF" condition.

The Line Interface also includes a send/receive current I/O having specific characteristics described below:

4. Transmitted Data (TO) - Pin 2
2.1.1.5 (Continued)

a. Receive Data (RX) - Pin 3
To TAU: Serial binary data is received on this lead from the associated Data Set at a specific bit rate corresponding to mark-space signals serially transmitted from a remote terminal via a Data Set.

b. Request to Send (RTS) - Pin 4
From TAU: A signal to the Data Set that when "ON" conditions it to transmit carrier and must remain on during the send interval. The RTS lead is permanently biased "OFF".

c. Clear to Send (CTS) - Pin 5
To TAU: A signal derived in the data set that when in the "ON" condition indicates the data set is ready to transmit data.

d. Data Set Ready (DSR) - Pin 6
To TAU: A signal from the Data Set that when "ON" indicates the data set is connected to the communication channel.

e. Data Carrier Detect (DCD) - Pin 8
To TAU: This signal goes "ON" when the data set is in the data mode and it has detected data carrier. When "OFF" the Receive Data lead is in the "MARK" hold condition.

f. Data Speed Indicator (DSI) - Pin 12
To TAU: This signal goes on when the data set is operating at 300 WPM. When the data set is operating at 100 WPM this lead goes off.

g. Ring Indicator (RI) - Pin 22
To TAU: This signal goes "ON" during the ringing cycle of a call.

2.1.1.6 Description of Auxiliary I/O leads - Connector J003
Refer to Table 1-3.

From TAU: A signal to the Data Set indicating condition of the terminal. A DTR "ON" signal allows the Data Set to switch over to the communication channel. With DTR "OFF", the data set will not remain in the data mode thus turning DSR "OFF". The DTR lead is controlled by the Keyboard Printer and/or the local auxiliary send/receive device.
<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>LEAD DESIGNATION</th>
<th>REV.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PROTECTIVE GROUND</td>
<td>TPA</td>
</tr>
<tr>
<td>2</td>
<td>TRANSMITTED DATA</td>
<td>EDA</td>
</tr>
<tr>
<td>3</td>
<td>RECEIVE DATA</td>
<td>RTA</td>
</tr>
<tr>
<td>4</td>
<td>REQUEST TO SEND</td>
<td>CTSA</td>
</tr>
<tr>
<td>5</td>
<td>CLEAR TO SEND</td>
<td>DSRa</td>
</tr>
<tr>
<td>6</td>
<td>DATA SET READY</td>
<td>CDA</td>
</tr>
<tr>
<td>7</td>
<td>LOGIC GROUND</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>CARRIER DETECT</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>TRANSMITTER CURRENT INT.-</td>
<td>TCIA</td>
</tr>
<tr>
<td>14</td>
<td>TRANSMITTER CURRENT INT.+</td>
<td>TCIA+</td>
</tr>
<tr>
<td>15</td>
<td>RECEIVE CURRENT INT.-</td>
<td>RCIA-</td>
</tr>
<tr>
<td>16</td>
<td>RECEIVE CURRENT INT.+</td>
<td>RCIA+</td>
</tr>
<tr>
<td>17</td>
<td>PRINTER ON/OFF</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>TERMINAL READY</td>
<td>TRA</td>
</tr>
<tr>
<td>21</td>
<td>CHARACTER PER SECOND</td>
<td>CPS</td>
</tr>
<tr>
<td>24</td>
<td>DEVICE CONTROL</td>
<td>DC</td>
</tr>
<tr>
<td>25</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TABLE 2-1.6**

<table>
<thead>
<tr>
<th>2.1.1.6 (Continued)</th>
</tr>
</thead>
</table>

Receive Data (RD) - Pin 3

- **b.** From TAU: Serial binary data is transmitted to the auxiliary device over this lead at the selected baud rate. In the idle state, this output is "MARK" hold.

- **c.** Request To Send (RTS) - Pin 4

  - *To TAU:* This signal is used by the 243 answeback, it has no control over the TAU.

- **d.** Control Leads - Pins 5, and 8

  - From TAU: The following output control leads, Clear to Send (CTS), and Carrier Detect (DCD) Pines 5 and 8 are connected together and biased to the "MARK" state.

- **e.** Data Set Ready (DSR) - Pin 6

  - From TAU: This signal will be on when the terminal is either in the local or the data mode. It will be off when the printer is in the auto-answer mode.

- **f.** Terminal Ready (DTR) - Pin 20

  - To TAU: A signal from the auxiliary device indicating the condition of the unit. A DTR "ON" indicates that the Auxiliary unit is capable of sending or receiving data. A DTR "OFF" condition is reflected on the Line output.

- **g.** Character Per Second - Pin 23

  - From TAU: A signal to the auxiliary unit used to select one of two operating speeds. A positive signal indicates 10 characters per second - 11 unit code and a negative signal 30 characters per second - 10 unit code.

- **h.** Printer On/Off - Pin 17

  - To TAU: A TTL level signal from the auxiliary unit that is used to blind the Printer RD input. A 5 volt signal inhibits the printer keeping a MARK hold on the terminal RD input.

- **i.** Device Control - Pin 24

  - A lead to permit control of the auxiliary device.

- **j.** Transmitter Current Interface (TCIA, TCIA-) - Pins 14 and 13.
2.1.1.6 (Continued)

j. From TAU: Isolated current interface for sending mark-space (current-no current) signals to an auxiliary receiver. The characteristics are identical to the Line current interface. Current source is supplied externally.

k. Receive Current Interface (RCI4+, RCI4-) - Pins 16 and 15
To TAU: Isolated current interface for receiving mark-space (current-no current) signals from an auxiliary transmitter. Refer to Paragraph 2.1.1.3 for line characteristics.

l. Auxiliary DC Current Operation - Connector Strapping
To operate the auxiliary current interface on the external cable plug for receptacle J303 the pins 2, 6 and 20 must be strapped together.

m. Signal Ground - Pin 7
Reference for terminal logic and auxiliary unit.

2.2 Size

2.2.1 The 410754 Card Assembly is 14 7/8" wide, 4" high and 1" deep. The unit is mounted on a support frame.

2.3 Temperature Range

2.3.1 Operating 40°F to 110°F at relative humidity of 25% to 95% non-condensing.

2.3.2 Storage temperature - 40°F to 150°F.

SECTION II - DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly Drawings 410754, 410742, and 410080.

1.2 Schematic Drawings 47546D, 47408D, 40808D.

1.3 Circuit Descriptions 4754CD, 4740CD, 4080CD.

1.4 Specification 62,255S

2. THEORY OF OPERATION

2.1 General

2.1.1 The 410754 Circuit Card Assembly (TAU) comprises circuitry which essentially converts TTL signal levels to Standard RS232-C or vice versa and TTL signal levels of 20/50 mA current signalling or vice versa. It also provides the necessary logic for steering input and output data signals based on Terminal conditions.

2.1.2 Refer to Sheet 3 of 47545D. There are three control leads emanating from the Terminal, namely; Terminal Ready (TR), Duplex and Characters per Second. The primary control lead is Terminal Ready which indicates whether the Terminal is in the LOCAL or LINE mode.

2.2 Local Mode Operation

2.2.1 In the LOCAL mode, the Terminal Ready lead is "OFF" which in turn holds Data Terminal Ready "OFF" to the associated Data Set. When the unit is in the LOCAL mode, the TAU permits the following Terminal manipulations assuming a LOCAL Send/Receive device such as a tape reader or punch is connected to the Auxiliary I/O.

a. Keyboard sends to printer.
b. Keyboard sends to printer and Aux. Receiver.
c. Aux. Send device transmits to Printer.
d. Aux. Send device transmits to Printer and Aux. Receiver.
e. Aux. Send device transmits to Aux. Receiver.

Note: The respective Send/Receive devices contain operating controls. Refer to Figure 2 for Local Terminal configurations.
With TR off, the input to MLA5-3 is high which in turn disables and gates MLA6-11 and MLA6-8. The TR "off" signal also holds Data Terminal Ready off to the Data Set via EIA Driver MLA5-6. With DTR off, the Data Set holds the Receive Data (RD) lead in the marking state. In the LOCAL mode, the operator can generate page copy by keyboarding to the printer.

Also, with TR off, the MAID gates, MLA6-4 and MLA6-3 are enabled allowing data to be transmitted from the keyboard to an Auxiliary Receiving device via the RD lead provided the Aux. Receive device is enabled.

Data can be received from a local Aux. Send device via lead J301-Pin 2 and subsequently forwarded to the Printer via the Terminal RD lead J301-Pin 17. Also, data can be transmitted from an Aux. Sender to an Aux. Receiver and Printer. The OR gate, MLA3-11 couples the data to the LOCAL RD lead.

Applying a ground signal to the Printer ON/Off lead, J301-Pin 17 results in a MARK hold on the Terminal RD lead, thereby inhibiting the Printer from receiving data.

In the Terminal manipulations, the characters per second output from the Terminal J301 Pin 4 provides a means of changing the operating speed (baud rate) of the Aux. Devices. This signal is derived from the Printer Keyboard Characters per Second switch whereby a negative, (Low) on J301-Pin 25 indicates 30 characters per second at 10 unit code and a positive (Hi) indicates 10 characters per second at 11 unit code.

In the LOCAL mode, the Aux. send and receive devices having current interface can be operated in a similar manner. Details concerning the current I/O is described in Paragraph 2.4. When operating in conjunction with devices having current interfaces, Pin J301-2 and J301-20 should be connected to positive voltage (Connect J303-2 J303-20 to 3). This places a "sparking" signal on EIA receiver MLA9-3 allowing the Aux. Receive current interface to modulate OR gate MLA7-8.

On Line Mode Operation

In the Line mode, the Terminal Ready lead from the set is "ON" presenting a low (OV) signal on J301-5. Therefore, the DTR signal is "ON" to the Data Set, a manual or automatic (incoming call) line connection can be made. When the Data Set handshaking is completed, the inputs; Data Set Ready, Clear to Send and Carrier Detect will all be on presenting a "TAU Ready" signal (Low on output MLA3-3) to the Terminal logic thus allowing the Terminal to send and receive data from the line. In this conditions, OR gates, MLA3-6 and MLA3-3 have lows (0 volts) on their respective inputs resulting in a low signal on OR gate MLA3-3.

From an EIA standpoint, the Auxiliary Interface looks like a Data Set to an Auxiliary device. The Auxiliary device controls the DTR lead applying a signal to the line receiver, MLA9-4 which when on permits a low signal on OR gate output MLA10-3. The DTR signal to the Data Set is modulated through this OR gate. The line receiver, MLA5-6 is biased to provide an "OFF" condition to OR gate MLA10-3 to satisfy an open circuit condition.
2.3.3 (Continued)

A Terminal TR or "Aux. DTR" Off signal presents a high to ML85-6 resulting in DTR going off to the Data Set. If the Data Set was in the Data mode, a line disconnect will take place.

2.3.4 When operating on line, the Duplex signal input J301-14 which originates in the Printer Keyboard enables or disables and gate ML86-6. In the Full duplex state, a low (0) appears on this gate input. The data from the local send device is inhibited from sending data to the printer since in full duplex mode, the Printer is connected directly to the line. The output of gate ML86-6 is held low.

2.4 20/60 mA Transmit and Receive Current Interface.

2.4.1 Refer to Sheet 4 of 47545D. The line current interface consist of transmitting and receiving current interfaces that are isolated from the logic by means of optical isolators ML85 and ML81 respectively.

2.4.2 Transmit Current Interface

2.4.2.1 The send current interface can be connected to a 20 or 60 mA signal line with a maximum open circuit voltage of 125 volts D.C.

2.4.2.2 The send circuitry converts a Mark (Hi) and Space (Lo) signal from ML85-11 to a current - no current interface by switching the optical isolator light emitting diode through transistor Q1. The Q1 transistor switches approximately 55 mA.

2.4.2.3 The LED controls the optical photo transistor which in turn drives transistor Q3. With the optical isolator off, transistor Q3 is off, therefore, no current is flowing in the loop between pins J302-14 & 13. A no current condition constitutes a spacing signal.

When the LED is switched on, the optical transistor is turned on, supplying base drive to transistor Q3 which in turn switches on. With Q3 switched on current is allowed to flow in the loop constituting a "Mark" signal.

2.4.2.4 The current must be supplied from an adjustable 20 or 60 mA external current source whereby the positive side of the line must be connected to J302-14 & the negative side to J302-13. The 150V Zener diode, C4, protects transistor Q3 from transient line voltages.

2.4.3 Receive Current Interface

2.4.3.1 When no current is flowing in the receive current interface, pins J302-14 & 15, the LED ML81-1 is off. Consequently, the optical transistor is off and a +5V signal is applied to CMOS inverter ML86-7 representing a line spacing condition.

2.4.3.2 With current flowing in on J302-Pin 16, the LED is turned on which causes the optical transistor to turn on thus applying a low (0 Volt) signal to CMOS inverter ML86-7 representing a line marking condition. On the receive interface diode CE3 serves as a protection device for optical LED and resistor Rg limits voltage applied across the diode.

2.4.3.3 To facilitate operation of the line current interface, on interface connector J302, Pins 3, 4, 5, 6 and 8 must be strapped together to enable logic.

2.5 Auxiliary Current Interface

2.5.1 Refer to 47545D, Sheet 4.

2.5.1.1 The characteristics of the Auxiliary 20/60 mA Current and Receive Interfaces are like the line current interfaces. Optical isolators ML87 and ML810 comprise the Auxiliary transmitting and receiving current interface respectively. A described in the line current 1/0 the loop current must be supplied from an external source. To operate the auxiliary current interface, on connector J303, Pins 2, 5 and 20 must be strapped.
<table>
<thead>
<tr>
<th>REV.</th>
<th>DATE</th>
<th>AUTH. NO.</th>
<th>ISSUE</th>
<th>SHEET NUMBER</th>
</tr>
</thead>
<tbody>
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<td>1</td>
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</tr>
<tr>
<td>2</td>
<td>8-3-78</td>
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<tr>
<td>3</td>
<td>7-27-78</td>
<td>26779</td>
<td>3</td>
<td>3 1 2 2 2 2 2 2 2 1 1 2 2 2 2</td>
</tr>
</tbody>
</table>

**NOTE:** The 410755 Assm is referred to as Terminal Auxiliary Unit (TAU). The 410755 Assm can be used in place of 430751 Assm. For the sake of convenience, the 410755 Assm is also referred to as Terminal Auxiliary Unit (TAU) in this Circuit Description.

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2. UNR MARK TECHNICAL DATA
2.1 INPUTS AND OUTPUTS
2.2 SIZE
2.3 TEMPERATURE RANGE

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1. ASSOCIATED DOCUMENTS
2. THEORY OF OPERATION
2.1 GENERAL
2.2 LOCAL MODE OPERATION
2.3 On LINE MODE OPERATION
2.4 20/60 MA TRANSMIT AND RECEIVE CURRENT INTERFACE
SECTION I - GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 410755 Terminal Auxiliary Unit (TAU) card assembly serves as an interface between the Model 43 Keyboard Printer unit and external apparatus. The TAU contains one interface, namely, a Line I/O interface performing the following functions:

1.1.1 The Line I/O provides the necessary signalling and control conforming to EIA Standard RS 232C for operation with Bell System type 103J or 113J, 113B Data Sets to facilitate data exchange on a serial basis.

1.1.2 The Line I/O also contains isolated send/receive 20/60 mA current interfaces that permit serial exchange of data to a remote or local send/receive unit having D.C. current interfaces.

1.2 The TAU provides logic to control the respective interface.

1.3 The 410755 circuit card assembly is an integral part of the Model 43 set and is mounted in the rear of the unit. It is designed to operate in conjunction with a 410740 printer logic card.

2. GENERAL TECHNICAL DATA

2.1 Inputs and Outputs

   The Inputs and Outputs can be segregated into three categories; namely, Terminal, Line or Data Set, and Current I/O. See Figure 1.

2.1.1 Terminal Interface

   2.1.1.1 The Terminal Interface consists of eleven I/O leads of which five are control leads, two are data leads, three are power input leads, and a logic ground lead.

   2.1.1.2 The leads are terminated in a 20 pin male connector. Refer to Table I-1.

---

2.1.1.2 (Continued)

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>LEAD DESIGNATION</th>
<th>ABBR.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DATA SPEED INDICATOR</td>
<td>DSI</td>
</tr>
<tr>
<td>2</td>
<td>ANALOG LOOP</td>
<td>AL</td>
</tr>
<tr>
<td>3</td>
<td>TERMINAL R/PAD</td>
<td>TR</td>
</tr>
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<td>4</td>
<td>+5V</td>
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</tr>
<tr>
<td>5</td>
<td>LOGIC GROUND</td>
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<td>-12V</td>
<td>RI</td>
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<td>7</td>
<td>RING INDICATOR (NOT TTL LEVEL)</td>
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</tr>
<tr>
<td>8</td>
<td>+12V</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>TAU READY</td>
<td>DR</td>
</tr>
<tr>
<td>10</td>
<td>RECEIVE DATA</td>
<td>RD</td>
</tr>
<tr>
<td>11</td>
<td>SEND DATA</td>
<td>SD</td>
</tr>
</tbody>
</table>

2.1.1.3 Electrical Characteristics

   The interface is compatible with low power TTL logic conforming to the following characteristics:

<table>
<thead>
<tr>
<th>STATE</th>
<th>DRIVER</th>
<th>TERMINATOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>MARK</td>
<td>+2.4 ≤ VMARK ≤ +5.25 Volts</td>
<td>+2.0 ≤ VMARK ≤ +5.25 Volts</td>
</tr>
<tr>
<td>OFF (1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPACE</td>
<td>0 ≤ VSPACE ≤ +0.4 Volts</td>
<td>0 ≤ VSPACE ≤ +0.7 Volts</td>
</tr>
<tr>
<td>OM (0)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Open terminator input condition - An open circuit input on a terminator of the interface is a MARK or Control OFF condition.
2.1.1.4 Description of Terminal I/O Leads - Connector J301

a. Data Speed Indicator - Pin 2

To Terminal: When in the on condition, indicates to the terminal that the data set is operating at 300 WPM. When in the off condition, the data set is operating at 110 WPM.

b. Analog Loop - Pin 3

From Terminal: When in the ON state AL indicates the data communications unit is to go into the analog test mode. At all other times, this lead will be OFF. To execute test when AL is ON, TR is turned on by DATA or AUTO ANSI and it is expected the Data Communications unit will turn on DR. When TR is turned OFF, AL will also go OFF.

c. Terminal Ready - Pin 5

From Terminal: A signal when "ON" allows the associated data set to manually or automatically switch over to the communication channel. The Terminal Ready signal indicates unit's capability to communicate on line.

d. Ring Indicator - Pin 12

To Terminal: Ring indicator is used by the 963 answerback. This is an EIA signal (not TTL) which has no control over the TAU.

e. TAU Ready - Pin 15

To Terminal: A signal from the Terminal Auxiliary indicating that the associated Data Set is capable of sending or receiving data. When "ON" the Data Set Ready (CD), Data Carrier Detector (CF), and Clear To Send (ON) signals from the Data Set are in the "ON" state.

f. Receive Data - Pin 17

To Terminal: Serial binary data appears on this lead from the Data Set.

2.1.1.4 (Continued)

b. Power Inputs:

+5V ± 10% 150 mA max. - Pin 7
+12V ± 10% 35 mA max. - Pin 13
-12V ± 10% 20 mA max. - Pin 11

Logic Ground - Pin 9

The 410755 card utilizes above D.C. voltages that are supplied by the Terminal Power Supply via specified pins.

2.1.2 Description of Line or Data Set I/O Leads - Connector J302. Refer to Table 1-2

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>ABBRV.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FRAME GROUND (AA)*</td>
</tr>
<tr>
<td>2</td>
<td>TRANSMITTED DATA (BA)</td>
</tr>
<tr>
<td>3</td>
<td>RECEIVE DATA (BB)</td>
</tr>
<tr>
<td>4</td>
<td>REQUEST TO SEND (CA)</td>
</tr>
<tr>
<td>5</td>
<td>CLEAR TO SEND (CE)</td>
</tr>
<tr>
<td>6</td>
<td>DATA SET READY (CO)</td>
</tr>
<tr>
<td>7</td>
<td>LOGIC GROUND (AB)</td>
</tr>
<tr>
<td>8</td>
<td>CARRIER DETECT (CF)</td>
</tr>
<tr>
<td>9</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>DATA SPEED INDICATOR (SCF)</td>
</tr>
<tr>
<td>13</td>
<td>TRANSMIT C/L-</td>
</tr>
<tr>
<td>14</td>
<td>TRANSMIT C/L+</td>
</tr>
<tr>
<td>15</td>
<td>RECEIVE C/L-</td>
</tr>
<tr>
<td>16</td>
<td>RECEIVE C/L+</td>
</tr>
<tr>
<td>17</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>DATA TERMINAL READY (CD)</td>
</tr>
<tr>
<td>20</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>RING INDICATOR (CE)</td>
</tr>
<tr>
<td>22</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>ANALOG LOOP</td>
</tr>
<tr>
<td>25</td>
<td>AL</td>
</tr>
</tbody>
</table>

* ( ) EIA STANDARD RS-232C LEAD DESIGNATION

2.1.2.1 The Data Set inputs and outputs comply with EIA Standard RS-232-C whereby a signal level of +3 to +250 volts is a "space" or Control "OFF" condition and a level of -3 to -25 volts is a "mark" or Control "ON" condition.
2.1.2.1 (Continued)

a. Transmitted Data (TD) - Pin 2

From TAU: Serial binary data is transmitted to the Data Set over this lead from the Terminal Keyboard or local send device at the selected baud rate. In the idle condition, the signal is "MARK" hold to the Data Set and cannot be modulated unless Terminal Ready from the Keyboard Printer unit is on.

b. Receive Data (RD) - Pin 3

To TAU: Serial binary data is received on this lead from the associated Data Set at a specific bit rate corresponding to mark-space signals serially transmitted from a remote terminal via a Data Set.

c. Request to Send (RTS) - Pin 4

From TAU: A signal to the Data Set that when "ON" conditions it to transmit carrier and must remain on during the send interval. The RTS lead is permanently biased "ON".

d. Clear to Send (CTS) - Pin 5

To TAU: A signal derived in the data set that when in the "ON" condition indicates the data set is ready to transmit data.

e. Data Set Ready (DSR) - Pin 6

To TAU: A signal from the Data Set that when "ON" indicates the data set is connected to the communication channel.

f. Data Carrier Detect (DCD) - Pin 8

To TAU: This signal goes "ON" when the data set is in the data mode and it has detected data carrier. When "OFF" the Receive Data lead is in the "MARK" hold condition.

g. Data Speed Indicator (DSI) - Pin 12

To TAU: This signal goes "ON" when the data set is operating at 300 WPM. When the data set is operating at 100 WPM this lead goes off.

h. Data Terminal Ready (DTR) - Pin 20

2.1.2.1 (Continued)

From TAU: A signal to the Data Set indicating condition of the terminal. A DTR "ON" signal allows the Data Set to switch over to the communication channel. With DTR "OFF", the data set will not remain in the data mode thus turning DSR "OFF".

i. Ring Indicator (RI) - Pin 22

To TAU: This signal goes "ON" during the ringing cycle of a call.

j. Logic Ground - Pin 7

Reference for external Data Set and terminal logic.

k. Analog Loop - Pin 25

From TAU: When in the ON state AL indicates the data communications unit is to go into the analog test mode. At all other times this lead will be OFF. When AL is ON and TR is ON, the data communications unit is expected to turn on DA (for data sets 103).

2.1.3 The line I/O also includes a Send/Receive current interface having characteristics described below:

a. Transmitter Current Interface (TCI+, TCI-) - Pins 14 and 13

From TAU: Isolated send current interface that converts mark-space signalling to current-no current signalling. The output can be inserted into an external 20 or 60 ma current source whereby the open circuit voltage must not exceed 125 VDC. The circuit is polarity sensitive applying the positive side of the line to PIN 14 and negative side to PIN 13.

b. Receive Current Interface (RCI+, RCI-) - Pins 16 and 15

To TAU: Input that can be connected to a 20 or 60 ma receive current signal line whereby current-no current signalling is converted to mark-space data signal. The circuit is polarity sensitive applying the positive side of the line to PIN 16 negative side to PIN 15.

2.1.3.1 Line DC Current Operation - Connector Strapping

When the Terminal is connected to the line using the send and receive current interface, the following pins 3, 4, 5, 6, and 8 on cable connector must be strapped together.
2.2 Size
2.2.1 The 41075S Card Assembly is 16 7/8" wide, 4" high and 1" deep. The unit is mounted on a support frame.

2.3 Temperature Range
2.3.1 Operating 440°F to 110°F at relative humidity of 2% to 95% non-condensing.
2.3.2 Storage temperature: -40°F to 150°F.

SECTION II - DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS
1.1 Assembly Drawings 41075S, 410740, and 410080.
1.2 Schematic Drawings 4755CD, 47408D, 4080SD.
1.3 Circuit Descriptions 4740CD, 4080CD.
1.4 Specification 62,1678

2. THEORY OF OPERATION
2.1 General
2.1.1 The 41075S Circuit Card Assembly comprises circuitry which essentially converts TTL signal levels to Standard 85232-C or vice versa and TTL signal levels to 20/60 ma current signalling or vice versa. It also provides the necessary logic for steering input and output data signals based on Terminal conditions.
2.1.2 Refer to 4755SD. There is one control lead emanating from the Terminal, namely: Terminal Ready (TR). Terminal Ready indicates whether the Terminal is in the LOCAL or LINE mode.

2.2 Local Mode Operation
2.2.1 In the LOCAL mode, the Terminal Ready lead is "OFF" which in turn holds Data Terminal Ready "OFF" to the associated Data Set.
2.2.2 The TR "off" signal holds Data Terminal Ready off to the Data Set via EIA Driver ML82-11. With DTR off, the Data Set holds the Receive Data (RD) lead in the marking state. In the LOCAL mode, the operator can generate page copy by keyboarding to the printer.

2.3 On Line Mode Operation
2.3.1 In the Line mode, the Terminal Ready lead from the set is "ON" presenting a low (OV) signal on P231-5. Therefore, the DTR signal is "ON" to the Data Set permitting line operation.
2.3.2 With DTR on to the Data Set, a manual-or-automatic (incoming call) line connection can be made. When the Data Set handshaking is completed, the inputs; Data Set Ready, Clear to Send and Carrier Detect will all be "on" presenting a "TAU Ready" signal (low on output ML41-8) to the Terminal logic thus allowing the Terminal to send and receive data from the line.
2.4.3.1 When no current is flowing in the receive current interface, pins J302-16 and 15, the LED MLA3-1 is off. Consequently, the optical transistor is off and a +5V signal is applied to CHOS inverter MLA3-3 representing a line spacing condition.

2.4.3.2 With current flowing in on J302-Pin 16, the LED is turned on which causes the optical transistor to turn on thus applying a low (0 Volt) signal to CHOS inverter MLA3-3 representing a line marking condition. On the receive interface diode CRL serves as a protection device for the optical LED and resistor RB limits voltage applied across the diode.

2.4.3.3 To facilitate operation of the line current interface, on interface connector J5, Pins 3, 4, 5, 6 and 8 must be strapped together to enable data logic.

2.4.4 A number of 43's could be serially connected on the current loop interface. If the power is turned off or accidentally lost on any one set, the whole system would run open loop. To prevent this condition the 43066 Modification Kit may be added to the 41075 TAU. The 43066 Modification Kit contains a +1079 Card Assembly (see 475SSBD-3). The coil of K1 is connected to the +12V and -12V supplies. The normally closed contacts of K1 are connected to the transmit current loop (pins 13 and 14 of J302). With power applied to the relay the contacts will remain open and the current loop will function normally. If power is lost the contacts will close, shorting the transmit current loop and preventing the whole system from running open loop.

2.4.5 20/60 MA Transmit and Receive Current Interface.

2.4.5.1 Refer to 475SSBD. The line current interface consists of transmitting and receiving current interfaces that are isolated from the logic by means of optical isolators MLA4 and MLA3 respectively.

2.4.5.2 Transmit Current Interface

2.4.5.2.1 The send current interface can be connected to a 20 or 60 MA signal line with a maximum open circuit voltage of 125 volts D.C.

2.4.5.2.2 The send circuitry contains a Mark (H1) and Space (L0) signal to a current-no current interface by switching the optical isolator light emitting diode through transistor Q1. The Q1 transistor switches approximately 35 mA.

2.4.5.2.3 The LED controls the optical photo transistor which in turn drives transistor Q3. With the optical isolator off, transistor Q3 is off, therefore, no current is flowing in the loop between pins J302-14 and 13. A no current condition constitutes a spacing signal.

When the LED is switched on, the optical transistor is turned on supplying base drive to transistor Q2 which in turn switches on. With Q2 switched on current is allowed to flow in the loop constituting a "Mark" signal.

2.4.5.2.4 The current must be supplied from an adjustable 20 or 60 mA external current source at 12V to 125 volts open circuit; the positive side of the line must be connected to J302-14 and the negative side to J302-13. The 150V Zener diode, CR2, protects transistor Q2 from transient line voltages.

2.4.5.3 Receive Current Interface
<table>
<thead>
<tr>
<th>DRAWING NO.</th>
<th>SHEET NO.</th>
<th>DESCRIPTION</th>
<th>ISSUE NUMBER</th>
</tr>
</thead>
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<tr>
<td>4013 SD</td>
<td>1</td>
<td>430650 WIRE MATRIX PRINT HEAD</td>
<td></td>
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<tr>
<td>4080 SD</td>
<td>ALL</td>
<td>OPCM (430101)</td>
<td>2 2 2 2 2 2 2</td>
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<tr>
<td>4700 SD</td>
<td>ALL</td>
<td>POWER SUPPLY</td>
<td>6 6 7 7 7 7 8 8 9 9 9 9 11 12 12 12 12 12 12</td>
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<tr>
<td>4710 SD</td>
<td>ALL</td>
<td>410740, 410742 LOGIC CARD</td>
<td>1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1</td>
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<td>4754 SD</td>
<td>ALL</td>
<td>TERM. AUX. UNIT W/AUX I/O (TAU2)</td>
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<tr>
<td>2080 SD</td>
<td>1</td>
<td>MODEL 43 RO &amp; KSR SETS</td>
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<td>4735 SD</td>
<td>ALL</td>
<td>TERM. AUX. UNIT (TAU1)</td>
<td></td>
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<tr>
<td>9100 WD</td>
<td>1</td>
<td>LOGIC SYMBOLS AND TRUTH TABLES</td>
<td>2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2</td>
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<tr>
<td>9612 WD</td>
<td>1</td>
<td>430550 PRT LED ASSEMBLY</td>
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<td>9635 WD</td>
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<td>AUXILIARY AND DATA TERMINAL,TDU(4320ABB,-F,-ABB)</td>
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<tr>
<td></td>
<td></td>
<td>CIRCUIT CARD ASSEMBLIES</td>
<td></td>
</tr>
<tr>
<td>410080</td>
<td>1</td>
<td>CONSOLE LOGIC</td>
<td>7 9 9 9 10 11 11 13 13 13 13 13 14 15 17 19 19 19 19 20 20 20</td>
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<tr>
<td>410700</td>
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<td>9 9 9 10 10 10 10 10 10 12 12 13 13 13 13 13 13 13 13 14 14 14</td>
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<tr>
<td>410700</td>
<td>2</td>
<td>POWER SUPPLY</td>
<td></td>
</tr>
<tr>
<td>410745</td>
<td>ALL</td>
<td>K.P. LOGIC(4320AAA,-B,-F,-K,-L,-ABB,-E)</td>
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<tr>
<td>410742</td>
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<td>K.P. LOGIC (4320AAA,-J,-K,-L,-ABB,-H)</td>
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<td>410754</td>
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<tr>
<td>410755</td>
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<td>TERM. AUX. UNIT (TAU1)</td>
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</tr>
<tr>
<td>410702</td>
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<td>POWER SUPPLY (4320ABB,-C,-E,-G,-H)</td>
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<tr>
<td>4060 CD</td>
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<td>410080 CONSOLE LOGIC CARD</td>
<td>2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2</td>
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<td>4700 CD</td>
<td>ALL</td>
<td>POWER SUPPLY</td>
<td>1 1 2 2 2 2 2 2 2 2 2 2 3 3 3 3 4 4 4 4 6</td>
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<td>4760 CD</td>
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</tr>
<tr>
<td>4755 CD</td>
<td>ALL</td>
<td>TERM. AUX. UNIT (TAU1)</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:** THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF WDP.
NOTE - 430803 CABLE ASSEMBLY IS SOLDERED TO AND IS PART OF 410013 CIRCUIT CARD ASSEMBLY
### Sheet Index

| SHEET NO. | A | B | C | D | E | F | G | H | I | J | K | L | M | N | O | P | Q | R | S | T | U | V | W | X | Y | Z |
| 1-5000   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### Supporting Information

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<thead>
<tr>
<th>CATEGORY</th>
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<tr>
<td>CONCEPT DESCRIPTION FOR 4700 SD AND 4700D POWER SUPPLIES</td>
<td>4700SD</td>
</tr>
<tr>
<td>ACTUAL WIRE DIAGRAM FOR 4700D REAR FRAMe ASSEMBLY</td>
<td>4700D</td>
</tr>
</tbody>
</table>

### Sheet Index Notes

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REVISED.
2. THIS SHEET INDEX WILL BE REVISED AND UPATED EACH TIME ANY SHEET OF THE DRAWING IS REVISED OR A NEW SHEET IS ADDED.
3. THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NO.
5. ISSUE DATES WILL BE SHOWN ON THE SHEET INDEX ONLY.

---

*NOTE:* 4700 SD 52A, 53A & 54A ARE USED FOR H0150, AND CUSTOMER I.D. 64 OR LATER OF 4700 SD. 4700 SD 62, 63 & 64 ARE USED FOR COST I.D. 48 OR EARLIER OF 4700.
FS-2
DC-DC CONVERTER
(PRIMARY CIRCUIT)
NOTE:
* WAVE FORMS MEASURED WITH POWER SUPPLY PLUGGED INTO AN ISOLATION TRANSFORMER AND (1.5V).
** WAVE FORMS MEASURED WITH RESPECT TO PROTECTIVE GROUND UNLESS OTHERWISE STATED.
TC-2
VOLTAGE-CURRENT WAVEFORMS
OSCILLATOR DRIVEN MODE

DC AND SQUARE WAVE
OSCILLATOR ML-2

+12V

0V

90 DEG.

RAMP GENERATION
ML-2-14

* 3.0V

0V

CONTROL VOLTAGE
ML-3-9

* 5V

0V

MOTOR KINEMATIC MODULATION
ML-13

* 1.0V

0V

PULSE TRANSFORMER DRIVE
ML-710/11

*50V

*30V

*10V

0V
### CONTENTS

<table>
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<th>SHEET INDEX</th>
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<th>SHEET NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1 2 3 4 5</td>
<td>6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28</td>
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<tr>
<td>PS-1 TERMINAL CONTROLLER</td>
<td>1 2</td>
<td>3 4 5 6 7 8 9</td>
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<tr>
<td>PS-2 TERMINAL CONTROLLER</td>
<td>1 2</td>
<td>3 4 5 6 7 8 9</td>
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<tr>
<td>PS-3 PRINT HEAD AND HELD DEVICES</td>
<td>1 2</td>
<td>3 4 5 6 7 8 9</td>
</tr>
<tr>
<td>PS-4 CARRIER MOTOR AND LUNED MOTOR OPTIONS</td>
<td>1 2</td>
<td>3 4 5 6 7 8 9</td>
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<td>PS-5 VOLTAGE DISTRIBUTION</td>
<td>1 2</td>
<td>3 4 5 6 7 8 9</td>
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<tr>
<td>NOTES</td>
<td>1 2</td>
<td>3 4 5 6 7 8 9</td>
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<tr>
<td>TC-1 TERMINAL CONTROLLER TIMING</td>
<td>1 2</td>
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<td>TC-2 PRINT CHARACTER TIMING</td>
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<td>TC-3 CARRIER RETURN-UNFEED TIMING</td>
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<td>3 4 5 6 7 8 9</td>
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<td>TC-4 TIMING DIAGRAM</td>
<td>1 2</td>
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### SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE ISSUED.
2. THIS SHEET INDEX WILL BE REFRESHED AND RE ISSUED EACH TIME A NEW SHEET IS ISSUED.
3. THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NO.
5. ISSUE DATES WILL BE SHOWN ON THE SHEET INDEX ONLY.

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<tr>
<td>BLOCK DIAGRAM</td>
<td>4740OSB</td>
</tr>
<tr>
<td>CIRCUIT DESCRIPTION</td>
<td>4740OSD</td>
</tr>
</tbody>
</table>

### APPROVALS

- M D LOGIC CARD
- (BASEC KDP)
- 4740OSD (2748)
NOTE: TIMING FOR RECEIVED CHARACTER FROM THE LINE IS SIMILAR TO ABOVE EXCEPT THE DATA BIT IS ABSENT AND THE NORMAL BIT TIME IS 3 TIMES.

(ROPS SELECTED OR 9 OR MORE ROOPS SELECTED)
FS-2
KEYSWITCH AND INTERFACE LOGIC

Notes:

1. Switch Keypad

<table>
<thead>
<tr>
<th>Switch</th>
<th>Open</th>
<th>Closed</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPS (G)</td>
<td>30</td>
<td>10</td>
</tr>
<tr>
<td>Duplex (E)</td>
<td>Half</td>
<td>Full</td>
</tr>
<tr>
<td>Parity (D)</td>
<td>On</td>
<td>Off</td>
</tr>
</tbody>
</table>

2. When the cover is open switch KS is UP (open), this signal will inhibit the printer from receiving data. Closing the cover will depress (close) the switch enabling the printer.
<table>
<thead>
<tr>
<th>SHEET INDEX</th>
<th>SHEET NO.</th>
<th>ISSUE NO.</th>
<th>SHEET NO.</th>
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<tbody>
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<td>SHEET INDEX, SUPPORTING INFORMATION</td>
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<td>2</td>
<td>41</td>
</tr>
<tr>
<td>FZ-2, KEYSENSE AND SENSE AMPLIFIERS</td>
<td>M1</td>
<td>2</td>
<td>42</td>
</tr>
<tr>
<td>FZ-3, KEYSENSE AND INTERFACE LOGIC</td>
<td>S2</td>
<td>1</td>
<td>43</td>
</tr>
<tr>
<td>FZ-4, CLOCK SELECTION AND DRIVERS</td>
<td>S3</td>
<td>2</td>
<td>44</td>
</tr>
<tr>
<td>FZ-4, POWER DISTRIBUTION</td>
<td>S4</td>
<td>1</td>
<td>45</td>
</tr>
<tr>
<td>NOTES</td>
<td>D1</td>
<td>1</td>
<td>46</td>
</tr>
<tr>
<td>TC-1, DATA INTERCHANGE TIMING</td>
<td>E1</td>
<td>1</td>
<td>47</td>
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<tr>
<td>TC-2, CLOCK TIMING</td>
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<td>48</td>
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<td>C31</td>
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<td>SAME AS C39</td>
<td>SAME AS R12</td>
<td>R40</td>
<td>319959</td>
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</table>
1. ALL VOLTAGES 115VAC.
2. TERMINAL DESIGNATIONS IN PARENTHESES ARE FOR REFERENCE AND ARE NOT MARKED ON COMPONENT.
3. ○ INDICATES FEMALE TERMINAL
   ● INDICATES MALE TERMINAL
4. ALL WIRE 18 AWG.
5. FUSE 1.0A SL-BL(PART NO. 113431)
### Sheet Index

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**Sheet Index Notes**

1. When changes are made in this drawing only those sheets affected will be revised.
2. This sheet index will be reprinted and updated (to include any new sheets) as a new issue is added.
3. The last complete column indicates the latest issue number of the sheet index.
4. Sheets that are not changed will retain their existing issue no.
5. Issue dates will be shown on the sheet index only.
TC-2 PRINT CHARACTER TIMING
MODE TWO CHARACTER BURST AT WELL COLUMN

REQUEST HEAT CHARACTER
MLCT-23

CARRIAGE MOTOR PHASE 1
MLCT-25

CARRIAGE MOTOR PHASE 2
MLCT-24

CARRIAGE MOTOR PHASE 3
MLCT-23

CARRIAGE MOTOR PHASE 4
MLCT-22

PRINT LEVELS 1 THRU 3
MLCT 204 30 THRU 31

E11
MLCT-30

NOTES:
- Indicates Pulse Width Modulation

1. VARIABLE DUTY CYCLE
2. SETTLING POWER DUTY CYCLE
3. COIL POWER DUTY CYCLE
4. PRESENCE OF PULSE ON A GIVEN LEVEL DEPENDS ON CHARACTER PRINTED.
TC-1
DATA INTERCHANGE TIMING

FREQUENCY = 122 kHz
PERIOD = 8.05 ms

RESET SCAN
1st SCAN
2nd SCAN
3rd SCAN
4th SCAN
KEYSWITCH RELEASED
FULLY SHORTED
RELEASED KEY, NOT FULLY SHORTED, NOTE B.

START
EXTEND PARITY

NOTES:
1. FIRST DEPRESSION AND DEPRESSION DO NOT EXIST
   FOR INPUT V0 (Vpp).
2. SEE SHEET 01 FOR MAPPING OF CONSIDERATION.
3. THE NOT FULLY SHORTED CONDITION IS USUAL FOR
   THE CAPACITIVE KEYSWITCHES.
TC-2
CLOCK TIMING

NOTE 1. S1 AND S2, S3 AND S4, HAVE THE SAME TIMING AND LOGIC SEQUENCE, BUT DIFFERENT VALUES OF Vh.
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<td>FE-3 AC-DC INVERTER (SECONDARY)</td>
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<tr>
<td>FE-2 AC-DC CONVERTER (SECONDARY)</td>
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<tr>
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<td>FE-6 INVERTER &amp; CONTROL CIRCUIT (SECONDARY)</td>
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<td>EQUIPMENT NOTES</td>
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<td>VOLTAGE CURRENT WAVE FORMS</td>
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<td>FS BLOCK DIAGRAM</td>
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**CIRCUIT DESCRIPTION FOR ADDED POWER SUPPLY**

**CIRCUIT DESCRIPTION FOR ADDED REAR FRAME ASSEMBLY**

**ACTUAL REVISION SEQUENCE**

**NOTE:** 4700SD 85, 86 & 87 ARE USED FOR CUST. 1.0.5A OR LATER.

4700SD NO. 85 & 84 ARE USED FOR CUST. 1.0.4A OR EARLIER.

**SHEET INDEX NOTES**

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY.
2. THOSE SHEETS AFFECTED WILL BE REVISED.
3. THIS SHEET INDEX WILL BE REVISED AND UPDATED EACH TIME ANY SHEET OF THE DRAWING IS REVISED OR A NEW SHEET IS ADDED.
4. THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF THE SHEET INDEX.
5. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NO.
6. ISSUE DATES WILL BE SHOWN ON THE SHEET INDEX ONLY.
TC-2
VOLTAGE-CURRENT WAVEFORMS
OSCILLATOR DRIVER MODE

DC HART SQUARE WAVE
OSCILLATOR MLZ-2
+12V
0V
--- 50 SEC ---

NULL GENERATOR
MLZ-14
+ 3.5V
0V

CONTROL VOLTAGE
MLZ-9
+ 5V
0V

PULSE WIDTH MODULATOR
MLZ-13
+ 1.0V
0V

PULSE TRANSFER DRIVE
OSCILLATOR
+30V
+12V
+30V
0V
NOTE:
WAVE FORMS MEASURED WITH POWER SUPPLY PLUGGED INTO AN ISOLATION TRANSFORMER AND ("F") TIED TO PROTECTIVE GROUND. ALL VOLTAGES MEASURED WITH RESPECT TO PROTECTIVE GROUND UNLESS OTHERWISE NOTED.
* WAVE FORMS MEASURED WITH RESPECT TO BASE OR QB.
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<td>NOTES</td>
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<td>P1-1 TERMINAL CONTROLLER</td>
<td>3</td>
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<tr>
<td>P1-2 PRINTER TIMING LOGIC</td>
<td>4</td>
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<tr>
<td>P1-3 PRINT HEAD AND BELT DRIVERS</td>
<td>5</td>
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<tr>
<td>P1-4 CARDAGE MOTOR AND LIMTED MOTH DRIVERS</td>
<td>6</td>
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<tr>
<td>P1-5 VOLTAGE DISTRIBUTION</td>
<td>7</td>
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<td>P1-6 TERMINAL CONTROLLER TIMING</td>
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<td>P1-7 PRINT CHARACTER TIMING</td>
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<td>P1-8 CARDAGE RETURN - UNDIPED TIMING</td>
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<tr>
<td>P1-9 TIMING DIAGRAM</td>
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**SHEET INDEX NOTES**

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REVISED AND UPDATED EACH TIME ANY SHEET OF THE DRAWING IS REISSUED OR A NEW SHEET IS ADDED.
3. THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NO.
5. ISSUE DATES WILL BE SHOWN ON THE SHEET INDEX ONLY.
FS-2
LINE AND AUXILIARY 20/60 MA CURRENT I/O

NOTE: WHEN USING THE CURRENT LOOP:
P235 = 3-4-5-6-8 OF J302 MUST BE STRAPPED WHEN USING LINE CURRENT LOOPS
P235 = 2-5-9-0 OF J303 MUST BE STRAPPED WHEN USING AUX CURRENT LOOP
<table>
<thead>
<tr>
<th>OPTION</th>
<th>40674 Z05</th>
<th>40674 Z05</th>
<th>40675 Z04</th>
<th>40675 Z04</th>
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<tr>
<td>END ON EYE</td>
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</table>

**NOTES:**

1. THIS OPTION APPLIES TO BATCH MODE ONLY AND IS DEPENDENT ON THE V/H MODE.

2. THIS OPTION APPLIES TO V/H MODE ONLY. BATCH MODE OPERATION IS ALWAYS HALF DUPLEX REGARDLESS OF OPTION SELECTED.

3. THIS OPTION MUST BE SELECTED FOR PROPER OPERATION.

4. IF THE AT CHARACTER IS PROTECTED, THIS OPTION SHOULD NOT BE USED WITH THE "SEND "SAME" PROTECTED DATA AS 'DELET' OR "SEND UNPROTECTED" DATA ONLY OPTIONS.

5. SENDING OF UNPROTECTED DELETIONS MAY BE ELIMINATED WITH THE OPTION ON 40674.

6. THIS OPTION IS AVAILABLE ONLY ON ISSUE 3A OR LATER ASSEMBLIES OF 40674.

7. THIS OPTION IS REQUIRED WHENEVER A 103 TYPE MODERN INTERFACE AND/OR THE 2ND MOVING LAMP INTERFACE IS BEING USED.

8. THIS OPTION IS REQUIRED FOR EITHER FULL DUMPS OR HALF DUMPS DUMP MODES. WHEN THE 2ND MOVING LAMP INTERFACE IS BEING USED, THIS OPTION WILL BE COMPATIBLE WITH A LOCAL COPY FEATURE (E.G., TRANSMITTED DATA IS WRAPPED ON TO RECEIVE DATA INTERNAL TO THE MODERN).

9. THIS OPTION MAY ONLY BE USED WHEN THE "202 TYPE MODERN INTERFACE" OPTION IS BEING USED.

10. SWITCH PAIR 421, SWITCH 1 IS NORMALLY OPEN FOR 103 DUMP OPERATION EXCEPT WHEN A MODEL 40 NEW "PRINTER" (43A) IS BEING USED, THEN THIS SWITCH MUST BE CLOSED.

11. TO PROVIDE THE INTERRUPT FUNCTION ON KEYBOARD DISPLAY TERMINALS (NO PRINTER) A 40674 CIRCUIT CARD MUST BE USED. IN THIS CASE 40674 CIRCUIT CARDS ISSUE 2 OR EARLIER REQUIRE THE CIRCUIT PATH "COMPONENT SIDE" BETWEEN 825-821-2 AND THE PLATED THROUGHホール IS CUT. LATER ISSUES REQUIRE PROGRAMMING OF OPTION SWITCHES ONLY.

12. Normal operation, this switch must be closed for proper operation. For receive even parity detection in batch mode refer to 40679 page 301.

13. THIS OPTION IS AVAILABLE ONLY ON ISSUE 3A OR LATER ASSEMBLIES OF 40674 CIRCUIT CARDS.

14. THIS OPTION IS AVAILABLE ON ISSUE 3A OR LATER ASSEMBLIES OF 40674 CIRCUIT CARDS.
NOTE: 1. CIRCUIT DESIGN CHANGE AT CUSTOMER D.O. ISSUE 2A
    WIRING DESIGNATORS 2H & 3A ISSUE 1 IN OR LATER.
    CHARGE RELATED TO ISSUE 2A OF 40374G BOARD
    a. ADD R.O.G. CIRCUITRY FOR NUCLEUS V0.80 AND
       MAPL, NEW MACON (4306E)1 AND MAPL (ASID3)addin.
    b. TO IMPROVE NOISE IMMUNITY, CAPACITORS
       C17 REMOVED AND C9 RELOCATED.
TC-1 TERMINAL CONTROLLER TIMING
MODE: LOCAL

NOTE: TIMING FOR RECEIVED CHARACTER FROM THE LINE
IS SIMILAR TO ABOVE EXCEPT THE "PAR" BIT IS
ABSENT AND THE NOMINAL BIT TIME IS 3.33 USEC
(100% SELECTED) OR 3.05 USEC (100% SELECTED).
TC-2 PRINT CHARACTER TIMING
MODE TWO CHARACTER BURST (AT BELL COLUMN)

REQUEST NEXT CHARACTER
MLCT-15

CARriage MOTOR PHASE 1
MLCT-20

CARriage MOTOR PHASE 2
MLCT-24

CARriage MOTOR PHASE 3
MLCT-23

CARriage MOTOR PHASE 4
MLCT-22

PRINT LEVELS 1 THRU 9
MLCT PINS IN TRAM 31

MLCT-30

NOTES:

1. VARIABLE DUTY CYCLE
2. SETTLING TIME DUTY CYCLE
3. ISLE DUTY CYCLE
4. PRESENCE OF PULSE ON A GIVEN LEVEL DEPENDS ON CHARACTER PRINTED.
TC-3 CARRIAGE RETURN-LINEFEED TIMING

(MARKING END OF CARRIAGE RETURN AND BEGINNING OF LINEFEED)

Motor Settle Time

Carriage Motor Phase 1
MLCT-25

Carriage Motor Phase 2
MLCT-24

Carriage Motor Phase 3
MLCT-23

Carriage Motor Phase 4
MLCT-22

Linefeed Motor Phase 1
MLCT-29

Linefeed Motor Phase 2
MLCT-28

Linefeed Motor Phase 3
MLCT-27

Linefeed Motor Phase 4
MLCT-26

Clamp Switch
MLCT-21

Notes: 

1. Settling Power Duty Cycle
2. Idle Power Duty Cycle
3. Linefeed Decor Power Duty Cycle

Indicates Pulse Width Modulation

See Specification 42.2006 for specific timing information.
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**SUPPORTING INFORMATION**

**CATEGORY**

**USE OF SHEET INDEX**

- WHEN CHANGES ARE MADE IN PRODUCTION:
  1. ONLY CHANGED SHEETS WILL BE REVIEWED.
  2. UNCHANGED SHEETS REMAIN IN EXISTING ISSUE NUMBER.
  3. THE LAST COMPLETED COLUMN ON THE SHEET INDEX INDICATES THE LATEST ISSUE NUMBER PER SHEET.
1. ALL VOLTAGES 115VAC.
2. TERMINAL DESIGNATIONS IN PARENTHESES ARE FOR REFERENCE AND ARE NOT MARKED ON COMPONENT.
3. ○ INDICATES FEMALE TERMINAL
   ○ INDICATES MALE TERMINAL
4. ALL WIRE 18 AWG.
5. FUSE 1.0A SL-BL(PART NO. 113431)
<table>
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<th>SHEET ISSUE NUMBER</th>
<th>REVISIONS</th>
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   1.2 Features

2. SUPPORTING INFORMATION

3. OPERATING INFORMATION

4. SECTION II - DETAIL DESCRIPTION AND THEORY OF OPERATION

5. LOGIC CIRCUITS

6. SHORT CIRCUIT PROTECTION

7. POWER-UP MODE

8. AC Line Input

9. DC Line Input

10. Blocking Oscillator

11. Schmitt Circuit

12. Basic Protection

13. Fault Protection

14. Overload Protection

15. Output Voltage Indicator
SECTION I - GENERAL TECHNICAL DATA

1. PURPOSE

1.1 The 430700 Power Supply is designed to provide the DC power required to operate the basic Model 43 ESR Set consisting of the Model 43 Printer, CPONX, Controller, and Terminal Data Unit (TDU) or Terminal Auxiliary Unit (TUA). Line input power may be 115 VAC ± 10%, 48/62 hertz or 165 VDC ± 10%. Four regulated DC output voltages are produced; +5V, +12V, -12V, +42V.

1.2 The input and output ratings are as follows:

- **Input:** 115VAC ±10%, 58/62 Hz - 0.9 A
- **Output:**
  - +5 VDC ± 8% - 0.75A
  - +12 VDC ± 7% - 0.4A
  - -12 VDC ± 7% - 0.4A
  - +42 VDC ± 8% - 1.0A (Average)

1.3 All circuitry for the 430700 Power Supply is contained on the 410700 Power Supply Card. This card and associated heat sinks, brackets, and covers are assembled to form the 430700 Power Supply unit which is mounted in the cabinet rear frame. Line power is applied to the unit through a cable having a three terminal connector. A line fuse is provided in the cabinet rear frame adjacent to the On/Off switch. The output is available through a 10 pin connector located at the top edge of the circuit card in the supply.

2. OPERATION

2.1 The 430700 Power Supply is of the "Off-the-Line" Switching Regulator type utilizing a "Herring Choke" design to accomplish power conversion at a nominal frequency of 20 KHz. This design provides a relatively high power conversion efficiency, and minimizes the size and weight of the supply.

2.2 The AC line voltage is directly converted to DC by a bridge rectifier connected directly to the AC input and filtered by a capacitor on the output side of the bridge rectifier. The primary of a power transformer is connected to the DC source in series with a primary switching transistor. In operation, the transistor is driven into conduction for a controlled period of each cycle during which the current in the primary increases. During the remainder of the cycle, the transistor is non-conducting, but the energy stored in the primary inductance is transferred to four secondary windings. The secondaries each contain a semiconductor diode which provides half wave rectification.

2.3 The +5V, +12V and -12V outputs are derived from three separate windings which provide integrated circuit voltage regulators. These regulators are of the linear type.

2.4 The +42V output is derived from the fourth secondary winding. This output is sensed by a feedback circuit which controls the conduction period of the primary switching transistor so that the output is regulated to the correct voltage in response to line and load variations. A more detailed description of operation is contained in Section II.

2.5 The Protective Ground is not connected to the Primary Circuit ground. Care must be exercised during trouble shooting to prevent direct connection of these grounds because this will effectively by-pass one of the bridge rectifier diodes and cause full line voltage to be directly applied to another diode in the forward direction. This rectifier and other line components will fail under this condition.

2.6 The secondary voltage returns are tied together and directly connected to the Protective Ground. However, isolation is maintained between the AC line and the secondary circuits.

3. SUPPORTING INFORMATION

- 4700SD - Schematic Diagram
- 62,097B - Specification

SECTION II - DETAILED DESCRIPTION AND THEORY OF OPERATION

1. GENERAL

1.1 Operating Modes

1.1.1 During normal operation, the 430700 Power Supply functions as a fixed frequency, pulse width modulated switching regulator. However, whenever power is initially applied, the oscillator and control circuitry which are on the secondary side of the main power transformer, TI, are not operational. An auxiliary mode of operation is provided which is operational only during start-up while the oscillator and control circuitry are non-operating. In this auxiliary mode, the primary switching transistor is driven by an extra winding on transformer TI which is connected such that positive feedback is provided to its base. This results in a blocking oscillator like mode of operation during start-up.

1.1.2 Operation of the Power Supply in the power-up mode results in energy transfer to the secondary windings so that the oscillator and control circuitry, which are powered from the unregulated voltage which drives the +12V Regulator, will commence operation. With a low secondary voltage, the control circuitry provides a maximum pulse width which is constrained to be slightly less than 50% of a cycle. Whenever the oscillator drive has gained sufficient amplitude to reliably drive the primary switching transistor, the blocking oscillator action is automatically terminated and operation continues under oscillator driven control.
1.2 Features

1.2.1 An EFI filter is included in the AC line input to reduce conducted interference resulting from the use of a switching regulator "Off-the-Line".

1.2.2 In-rush currents on start-up are controlled by the use of a series line resistance and by a current limited drive on start-up.

1.2.3 AC line transient protection has also been provided which both tends to limit peak voltages as well as suppress the transfer of the transient to the secondary circuits.

1.2.4 An Output voltage detector circuit is included which will light an LED indicator only whenever all four secondary output voltages are present, although not necessarily within tolerance. This indicator may be viewed for maintenance purposes without removal of the unit.

1.2.5 The +5V, +12V, and -12V logic voltages are protected against accidental load shorts. Upon removal of the short, the power supply will either recover or shut off. To reset following a shut off, input power must be removed for at least 15 seconds. The +42V output is also protected against print head driver shorts by means of a fuse in the output.

1.2.6 All outputs are protected against sustained overvoltages. Detecting circuitry monitors each output and in the event of a fault, the oscillator drive is immediately removed so that the secondary circuits are no longer powered. Reset is accomplished by removing input power for 15 seconds.

2. POWER UP MODE

2.1 AC Line Input (FS-1)

2.1.1 Nominal input voltage (115 VAC) is applied to connector J202. The hot side of the line is applied to terminal #1. Protective earth ground is applied to terminal #2, and line neutral to terminal #3 of J202.

2.1.2 An R.F.I. filter, F21, reduces conducted interference entering and leaving the power supply.

2.1.3 Thermistor RT1 is in the hot side of the line to limit initial inrush current into capacitor C1. Initial resistance of RT1 is 2.5 ohms which after the supply is operational reduces to approximately 1.0 ohm due to self heating.

2.1.4 The transient protector RV1 is a voltage clamping device to limit the potential applied to primary circuits of the power supply. RV1 avalanches at approximately 150 VAC (RMS), limiting the voltage applied to other devices.

2.2 AC Line Rectifier

2.2.1 AC to DC rectification occurs through the full wave bridge consisting of the four diodes CR1, CR2, CR3 and CR4. Capacitor C1 filters the DC.

2.2.2 The anodes of CR3 and CR4 and the negative end of C1 are connected to a common bus for all primary circuits. This bus is not to be confused or connected with any ground bus on the secondary circuits unless the power supply is floated through an isolation transformer. Grounding of the primary bus might cause destruction of diode CR3, as well as thermistor RT1.

2.3 Blocking Oscillator Operation (FB-2)

2.3.1 Upon initial application of DC voltage to R3, current flows to charge C2. The time constant of R3 and C2 delays the start-up until capacitor C1 is fully charged.

2.3.2 The voltage across C2 biases the base of Q1 into the active region by applying DC potential through R8, terminal (J, K) of P2 and diode CR1. This causes current to flow into the base of Q1 tending to turn it on. As Q1 turns on, terminal L of P1 is forced toward primary bus common. Since coil P1 is tightly coupled to P2 an equivalent potential is applied across P2 according to the dot notation shown. R15 is a base bias resistor for Q1.

2.3.3 A portion of P2 is tapped at J to act as a source to further drive the base of Q1 toward saturation. Regenerative action occurs because of positive feedback driving Q1 into saturation.

2.3.4 Base drive into Q1 is limited by resistor R8. The Q1 collector current ramps up due to the magnetizing inductance of T1. This current is limited by the gain hFE of Q1. For constant current base drive, Q1 remains in saturation until IC exceeds hFE times IB.

2.3.5 As Q1 comes out of saturation voltage across J-H is reduced, lowering the base drive to Q1. Regenerative action occurs forcing Q1 off. Q1 remains off until the energy in T1 collapses via dumping energy into the secondaries (S1, S2, S3, S4). The cycle then repeats itself until the pulse width modulator mode takes over.
2.4 Smoothing Circuit (FS-2)

2.4.1 The smoothing network consisting of coil P2 and diodes CR14 and CR12 clamp the collector of transistor Q1 during turn off to twice the DC supply voltage. During turn off terminal L of P1 exceeds the potential at terminal C due to the inductive kick of the transformer T1. The potential across terminals L-G is mirrored on terminals K-H by observing the dot notation polarity.

2.4.2 Upon turn off terminal K becomes more positive than +12VDC in and is clamped by CR14. Terminal H becomes more negative than the -VDC bus common. This forces a clamping of coil P2 which reflects to coil P1 due to tight coupling. The voltage on the collector of Q1 is limited to that across P2 or twice VDD. Diode CR7 prevents capacitor C2 from being reversed biased.

3. OSCILLATOR DRIVEN NODE

3.1 20 kHz Square Wave Oscillator

3.1.1 During start-up, the secondaries of T1 receive a limited amount of power which results in an increasing rectified voltage. The oscillator is fabricated from one of the comparators in ML2 which derives its power from the regulated +12V supply. As the voltage increases to approximately 4 volts, oscillation commences.

3.1.2 If the oscillator output (Pin 2) has just switched to ground, the voltage at the non-inverting input (Pin 5) will be determined by the divider of R35 and R32 in parallel with R32. This voltage is 31% of the +12V supply. The voltage on the inverting input (Pin 4) discharges toward ground at a rate determined by R38 and C11. As this voltage drops to 31% of the +12V supply, the comparator output switches to the high state. Now, the voltage on Pin 5 is essentially determined by the divider of R32 in parallel with R35 and R32. This voltage is 62% of the +12V supply. The voltage on Pin 4 charges toward the +12V supply at a rate determined by R30 and R38 in series, and C11. As this voltage now reaches 62% of the +12V supply, the comparator output (Pin 2) switches to the low state.

3.1.3 Since the comparator switch points are a fixed ratio of the +12V supply, the frequency will be virtually independent of the actual voltage of the +12V supply. In fact, from approximately 4 to +20 volts, the frequency and duty cycle are essentially constant.

3.2.2 Whenever the oscillator output goes to the high state, the output of the Ramp Generator is unclamped. The voltage on C10 begins to charge toward the +12V supply by means of resistor R29. The voltage reaches approximately 3.5 volts during the time that the oscillator output is high. Whenever the oscillator output goes to the low state, C10 is discharged and the Ramp voltage goes to a few tenths of a volt above ground.

3.3 Pulse Width Modulator (FS-4)

3.3.1 A third section of ML2 is used for a Pulse Width Modulator. The output of the Ramp Generator is connected to the non-inverting input (Pin 11) by means of Resistor R29. The inverting input (Pin 10) is connected to a divider network consisting of R47 and R44 which derives a bias of approximately 0.6 volt from the +12V supply.

3.3.2 In the absence of any output from Pin 9 of ML3, the bias voltage of 0.6 volt appears on Pin 10 of ML2. Consequently, whenever the Ramp Generator output is low, the Pulse Width Modulator output (Pin 13) will be low shunting any current flowing through R25. Whenever the Ramp Generator output exceeds the bias voltage, the Pulse Width Modulator will go to a high state. Any current flowing through R25 will now be available to drive the base of transistor Q10.

3.3.3 Resistor R25 is connected to the +12V supply through a 4-Layer Diode CR21. This diode is non-conducting until the +12V supply exceeds approximately 8 volts, at which point the diode triggers into conduction with a drop of approximately one volt. During start-up, even though the oscillator is running and the Pulse Width Modulator producing drive pulses, transistor Q10 will not receive drive pulses until CR21 becomes conducting.

3.3.4 Whenever an output is produced on Pin 9 of ML3 that exceeds the 0.6 volt bias, the pulse width of the output on Pin 13 of ML2 will be reduced. The Pulse Width Modulator output will be in the high state for the time that the Ramp Generator output exceeds the voltage produced on Pin 9 of ML3.

3.3.5 Resistor R60 is connected between the Ramp Generator output and the non-inverting input to provide hysteresis and snap-action switching. Resistor R64 provides a base leakage path for transistor Q10.

3.4 Voltage Reference and Error Amplifier (FS-4)

3.4.1 The Voltage Reference and Error Amplifier is contained in ML3, a Type 723 Precision Regulator. The voltage reference, Vref (Pin 6), is nominally 7.15 volts with a ±3% tolerance. This voltage is applied to a precision divider consisting of R37 and R45 to provide a 3.27 volt reference which is applied to the inverting input (Pin 4) of the Error Amplifier.
3.4.2 The +42V volt rectified DC output is connected to a precision divider consisting of R60 and R59. The resulting voltage is applied to the non-inverting input (Pin 5) of the Error Amplifier. In operation, the voltage at Pin 5 is very close to that at Pin 4. Frequency compensation of the Error Amplifier is accomplished by connection of capacitor C13 between the compensation terminal (Pin 13) and the inverting input (Pin 4).

3.4.3 The DC gain of the Error Amplifier, ML3, is utilized to produce the control signal at Pin 9. Gain of the Error Amplifier is reduced by use of negative feedback from the direct output at Pin 10 through resistor R66. Capacitor C17 is used to bypass any high frequency noise in proximity to the Error Amplifier.

3.5 Primary Power Conversion

3.5.1 As previously noted, the 20 KHz Oscillator will commence operation and produce drive pulses to the base of transistor Q10 whenever the +42V supply exceeds approximately 8 volts. At this point, the pulse transformer T2, in the collector of Q10 will be driven so as to produce a positive pulse of similar duration on its secondary. This pulse is connected through resistor R8 and diode CR10 to the base of the primary switching transistor, Q1.

3.5.2 The positive drive on the base of Q1 causes current to flow in the collector of Q1 and the primary winding (P1) of transformer T1. The current increases, linearly during the duration of the pulse, from its initial value to its final value which is dependent upon the pulse width as well as the DC supply voltage. Diode CR13 effectively prevents Q1 from reaching full saturation, reducing the storage time for Q1.

3.5.3 The positive pulses are also connected through diode CR9 which rectifies the signal to produce a DC signal on capacitor C4 and bleeder resistor R13. When the power supply begins operating in the oscillator driven mode, the DC signal is connected through diode CR8 and resistor R9, to the base of transistor Q7. The collector of Q7 is connected to the feedback winding used to provide the blocking oscillator action. Turning Q7 on will short the signal produced by the feedback winding and effectively inhibit blocking oscillator action. This control is automatically transferred from the start-up mode to the oscillator driven mode.

3.5.4 Whenever the drive to the base of Q10 is shunted by the Pulse Width Modulator, the drive pulse is terminated. The collector of Q10 rises from the saturated value of Q10 to a voltage above the +42V supply. This results in a negative pulse on the secondary of T2. This pulse is connected through resistor R22 to the base of transistor Q5. Transistor Q5 is turned on which effectively grounds the base of Q1. The stored base charges in Q1 is discharged through Q5 resulting in rapid turn-off of Q1.

3.5.5 When Q1 turns OFF, the energy which was stored in the magnetic core of T1, is transferred to the secondary windings. Each winding is driven in proportion to its relative turns ratio.
3.7.3 Zener diode CR5 is provided to permit the latch to clear whenever the rectified primary DC voltage drops below approximately 50 volts. This allows the power supply to automatically restart under the blocking oscillator mode of operation if the oscillator driven mode has also become inoperative.

3.8 Primary Circuit Overcurrent Protection (FS-2)
3.8.1 A resistor, R6, in the emitter of the primary switching transistor, Q1, senses the current conducted during each pulse drive period. If this current should exceed a safe level, the base drive current is shunted for the remainder of that drive pulse.

3.8.2 The voltage developed on R6 is applied through resistor R19 to capacitor C6 which acts to filter spurious transients, to R27 which is in series with the base of transistor Q6, and to the base of transistor Q4. Whenever the voltage developed is high enough to cause Q8 to conduct sufficient current through the collector resistor, R20, which is connected through diode CR15 to the drive pulse transformer T2, to bias transistor Q9 into conduction, a regenerative action is initiated. This allows current to flow through the emitter resistor, R21, of Q9. The current drives both the base of Q8 and the base of Q4. Whenever Q4 conducts, the base drive current to Q1 is shunted to the primary common, effectively terminating the primary switching transistor current pulse for that cycle. Whenever the drive pulse from transformer T2 terminates, transistors Q8, Q9 and Q4 are returned to their non-conducting state.

3.9 Primary Circuit Overvoltage Protection (FS-4)
3.9.1 In the event that a transient spike occurs on the AC line that exceeds the normal voltage range, circuitry has been provided which will maintain the primary switching transistor in the non-conducting state even through base drive pulses are being generated. This protection is accomplished by shunting the oscillator drive pulses during the transient.

3.9.2 Zener diode CR6 cathode is connected to the primary DC power, and anode to resistor R2. Whenever the DC voltage is high enough to exceed the zener diode voltage, current flows to the base of transistor Q2 by means of resistor R7, and the base of Q6 by means of resistor R16. Base bias resistor R5 serves to bypass leakage current for both Q2 and Q6.

4. LOGIC VOLTAGES (FS-3)
4.1 +5V Supply
4.1.1 The +5V supply is derived from a secondary winding of T1. The voltage on winding S4 is half wave rectified by diode CR16 and filtered by capacitors C7 and C18. This unregulated voltage, +5V, is applied to the base connection (B) of a linear regulator, ML5, which is a self contained three terminal integrated circuit located on a common heat sink with ML6 and ML7. A capacitor, C19, on the output (E) of the regulator filters high frequency load transients.

4.1.2 The +5V supply is connected to terminals 5 and 6 of connector J201 on the power supply. Logic supply return is connected to terminals 9 and 10.

4.2 +12 Volt Supply
4.2.1 The +12V supply is derived from a secondary winding of T1. The voltage on winding S2 is half wave rectified by diode CR19 and filtered by capacitors C9 and C23. This unregulated voltage, +12V, is applied to the base connection (B) of a linear regulator, ML7, which is a self contained three terminal integrated circuit located on a common heat sink with ML5 and ML6. A capacitor, C22, on the output (E) of the regulator filters high frequency load transients. The +12V supply is also used to drive the Error Amplifier.

4.2.2 The +12V supply is connected to terminal 7 of connector J201.

4.3 -12 Volt Supply
4.3.1 The -12V supply is derived from a secondary winding of T1. The voltage on winding S3 is half-wave rectified by diode CR18 and filtered by capacitors C8 and C21. This unregulated voltage, -12V, is applied to the collector connection (Q) of a linear regulator, ML6, which is a self contained three terminal integrated circuit located on a common heat sink with ML5 and ML7. A capacitor, C20, on the output (E) of the regulator filters high frequency load transients.

4.3.2 The -12V supply is connected to terminal 8 of connector J201.

5. OUTPUT VOLTAGE INDICATOR (FS-3)
5.1 Each DC output voltage has a divider network which senses the output level. The sensed output level is compared with a voltage reference derived by a divider network composed of R16 and R61 from the 7.15 volt reference voltage, VREF available from ML3. The comparison is done using four comparators in ML4.

5.2 The +5V output voltage sense divider is composed of R58 and R59. The +12V output divider is composed of R62 and R63. The +42V supply is sensed by a diode composed of R52 and R53. The -12V supply is sensed by a diode composed of R55 and R60. These sense voltages are connected to pins 11, 7, 5 and 8 respectively of ML4. The voltage reference is connected to pins 4, 6, 9 and 10.
5.3 The outputs of each comparator (pins 1, 2, 13 and 14) are connected together. Each comparator will go to a high state on the output whenever its sensed input exceeds the reference voltage. If all four comparators outputs are in the high state, then the current which flows through resistor R3/4 from the +4V supply will be available to drive the LED indicator, CR28. If any output voltage should fail, its associated comparator will go to a low state, shunting the current drive to CR28. Note that the sense divider for the +4V supply is located on the load side of the fuse.

6. FAULT PROTECTION ON SECONDARY

6.1 Short Circuit Protection

6.1.1 The +5V, +12V and -12V supply outputs are protected against short circuits to ground by means of the current limiting characteristics inherent in the integrated circuit voltage regulator which is in each of these outputs. Fault currents are limited to approximately 1.5 amperes. Whenever the fault is removed, the output voltage will either recover or shut off.

6.1.2 These regulators are also thermally protected so that in the event that their power dissipation in conjunction with the ambient temperature exceeds their limit, automatic shutdown occurs. Whenever the internal temperature decreases to a safe level, the device will reset and restore the output voltage.

6.1.3 The +42V supply is protected against overloads on the output by means of a 1 amp fast blow fuse, FI. Whenever this fuse opens, the Output Voltage Indicator will go dark even though the supply is otherwise functional.

6.2 Overvoltage Protection (PS-4)

6.2.1 Each secondary output voltage has an overvoltage sense circuit which will cause the power supply to shut down whenever an overvoltage is detected on an output. This is accomplished by means of a voltage comparator in integrated circuit ML2 which clamps the 20 kHz Square Wave Oscillator output to the low state, preventing the generation of drive pulses to the primary switching transistor, Q1.

6.2.2 The inverting input (Pin 6) of the comparator is biased by the divider network consisting of R33 and R36 to approximately one-half the voltage of the +12V supply. The non-inverting input (Pin 7) is normally biased to the voltage of the +12V supply by means of R34. An SCR, CR25, is also connected to Pin 7.
### Circuit Description of the M43 Logic Card

**Basic Rev.**

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CIRCUIT DESCRIPTION OF THE M43 LOGIC CARD
(BASIC KSR)

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SECTION I - GENERAL TECHNICAL DATA

1. GENERAL DESCRIPTION

1.1 The 410740 M43 Logic Card serves a threefold purpose in the M43 Basic KSR. It provides the control logic for the operator console, line interface and printer functions; it provides the drivers for the printer mechanism; and it serves as a harness card into which all the printer subassemblies are connected.

1.2 The 410740 Card controls all information flow among the three terminal subassemblies - operator console (OPCON), line interface (TAU/TDU) and printer. It retains the present terminal state (e.g., LOCAL/TALK) and determines each new terminal state from incoming OPCON or TAU/TDU information.

1.3 The 410740 Card also provides all the necessary timing and drive levels to cause proper operation of the various printer subassemblies.

2. FEATURES

2.1 Basic KSR Operational Features

The 410740 Card, when part of the basic KSR set, can perform a number of operator accessible features activated from either OPCON or TAU/TDU data streams. Detailed descriptions of these features can be found in the Basic KSR Set Specification.

2.2 Set Configuration Features

An 8 position DIP switch pack is provided to configure the terminal for certain optional functions.

2.2.1 Printer Related Options

Two switches select maximum printer line length. The options available are 72, 80 and 132 column line lengths.

Two switches select graphic character font. The options available are TV, ME and M4 fonts.

2.2.2 Line Interface Related Options

One switch enables the automatic new line feature. This feature insures no loss of data received from the TAU/TDU in the event of improper line formatting.

One switch enables the sending of even parity to the TAU/TDU. When disabled the parity bit is forced marking.

One switch enables automatic disconnect of a call up upon receipt of the ASCII EOT character.

2.2.3 Maintenance Related Option

One switch enables a printer test feature, causing the printer mechanism to continuously print its selected character font.

3. SWITCH OPTIONS

3.1 The following convention is used in the schematic wiring diagram and circuit description to designate each switch.

SPD4-SW4

SP  - Refers to switch pack.
D4  - Refers to location D4 on the card assembly.
SW4  - Refers to the fourth switch of package SPD4.
3.2 Detailed Description

ON - Switch Closed (SW1 is always oriented toward center of card.)
OFF - Switch Open

<table>
<thead>
<tr>
<th>Designation</th>
<th>Function</th>
<th>Switch State (To Enable Function)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW1</td>
<td>Automatic New Line</td>
<td>OFF</td>
</tr>
<tr>
<td>SW2</td>
<td>Printer Test</td>
<td>ON</td>
</tr>
<tr>
<td>SW3</td>
<td>Vertical Parity Send</td>
<td>OFF</td>
</tr>
<tr>
<td>SW4</td>
<td>EOT Disconnect</td>
<td>OFF</td>
</tr>
<tr>
<td>SW5</td>
<td>Line Length Select</td>
<td>Unused</td>
</tr>
<tr>
<td>SW6</td>
<td></td>
<td>72 Columns OFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 Columns ON</td>
</tr>
<tr>
<td></td>
<td></td>
<td>128 Columns ON</td>
</tr>
<tr>
<td>SW7</td>
<td>Character Font Select</td>
<td>Unused</td>
</tr>
<tr>
<td>SW8</td>
<td></td>
<td>BU Font OFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Undefined OFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TV Font ON</td>
</tr>
</tbody>
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4. SUPPORTING INFORMATION

M3 Logic Board Schematic - 4740SD
OPCON Schematic, Circuit Description - 4080SD, 4080CD
Print Head Schematic - 4013SD
MACL Spec. - 430641S
MACON Spec. - 430671S

SECTION II - DETAILED DESCRIPTION

1. GENERAL

1.1 The voltage and current requirements of the 410740 Card are as follows:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Voltage Range</th>
<th>Avg. Current Drain</th>
</tr>
</thead>
<tbody>
<tr>
<td>+42V</td>
<td>+37.8V to +46.2V</td>
<td>1.0A (with printer load)</td>
</tr>
<tr>
<td>+12V</td>
<td>+10.8V to +13.2V</td>
<td>450 ms Excluding OPCON and Communications Interface</td>
</tr>
<tr>
<td>-12V</td>
<td>-13.2V to -10.8V</td>
<td>150 ms</td>
</tr>
</tbody>
</table>

1.2 Other supply voltages developed on the card from the -12V supply have the following tolerances:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Voltage Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>-6V</td>
<td>-6.6V to -3.4V</td>
</tr>
<tr>
<td>-5V</td>
<td>-5.5V to -4.5V</td>
</tr>
</tbody>
</table>

1.3 Other voltages referred to in the circuit description have the following tolerances:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Voltage Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>VH</td>
<td>-3.5V to +5.5V</td>
</tr>
<tr>
<td>VL</td>
<td>0V to +5.5V</td>
</tr>
<tr>
<td>VTH</td>
<td>-2.6V to +5.5V</td>
</tr>
<tr>
<td>VTL</td>
<td>0V to +4.0V</td>
</tr>
<tr>
<td>VNH</td>
<td>+4.0V to +2.0V</td>
</tr>
<tr>
<td>VNL</td>
<td>-4.5V to -3.0V</td>
</tr>
</tbody>
</table>

1.4 The following convention is used in the circuit description to designate each circuit entering or leaving a multilogic (ML) pack.

ML - Refers to multilogic.
E1 - Refers to location E1 on card assembly.
3 - Refers to pin number of the associated circuit connection.

1.5 Logic Symbols - Positive logic symbols are used in the associated schematic.

1.6 Complex logic packs are represented by rectangles. These include the terminal controller logic = MACON (MLO) and the printer timing logic = MACL (MLC7).

1.7 Signal Designation - Signal leads are labeled with a title descriptive of the function of the signal. A line drawn over this title indicates that the signal is in its most negative state when the function described by the title of the signal is present.

2. BLOCK DIAGRAM

2.1 The block diagram of Figure 1 shows the interconnection and signal flow between the functional blocks FS-1 to FS-4.

2.2 The Terminal Controller (FS-1) controls overall terminal operation. It retains the present terminal state and displays that state in the light-emitting diode (LED) indicators on the set OCPON. It receives serial data from the OCPON, interprets it for terminal control functions and stores data to either the printer logic or the TAU/TDD or both. It controls serial data streams to and from the TAU/TDD, interprets incoming information for terminal control functions and buffers data before steering it to the printer logic.
2.3 The Printer Timing Logic (PS-2) controls all printer functions. It receives parallel data from the Terminal Controller, decodes it and performs the corresponding operation. The basic printer functions are character print, carriage return, line feed, backspace, bell, margin set, margin clear and margin releases.

2.4 Functional blocks PS-3 and PS-4 contain the power devices which drive the electro-mechanical subassemblies comprising the printer mechanism.

3. THEORY OF OPERATION

3.1 PS-1 Terminal Controller (See TC-1 Timing Diagram.)

3.1.1 General - Functional block PS-1 interfaces the M63 logic card to the set OPCON and the TAU/TEU. It also provides the input data to the printer timing logic and senses various switches for features and options.

3.1.2 OPCON Interface - Both a serial and a parallel data interface exist between OPEC and the TAU/TEU. The serial interface consists of a 560 kHz clock, a repeat mode signal and a serial data signal. The repeat mode signal (J107 pin 7) is active (character repeating) in the high state (VH) and inactive in the low (VIL). The serial data lead (J107 pin 6) is normally marking at VH. The transmission code used on this lead consists of eleven bits - one start bit, eight data bits, one parity bit and one stop bit. The spacing level is VIL. One bit time = 143 microseconds.

The R-C filters (R42, C14 and R43, C15) are present to minimize noise picked up on the interface cable.

The parallel data interface consists of five DC contact switch leads (J107 pins 14, 17, 18, 19, 20) and five LED drive signals (J107 pins 5, 9, 10, 11, 13).

The DC contact switches when depressed (closed) apply ground to the corresponding inputs of a 7417 open collector buffer (ML63). When released (open), 6K resistors (R255) pull the input outputs to VH. These buffers in turn drive the MACON pack (ML04-8, 26, 25, 27, 31) with the non-inverted switch state. VH will be present on the corresponding ML63 pin when the associated switch is open and VIL will be present when the switch is closed.

The printer test signal (ML64-24) is provided with an on-board DC contact switch (SPDA-SW2), wire 'AND'ed with ML63-4, that can enable printer test independent of the OPCON.

The five LED drivers in MACON (ML64-35 thru 38) pull their respective leads to VH when activating an LED. The 1K resistors (R37-R41) limit the LED forward current to 15 ma nominal.

3.1.3 Eleven parallel data leads (ML64-9 thru 19) interface the MACON logic pack with the printer timing logic.

The eight data leads transmit coded information to the printer timing logic. VH (VIL) represents a binary 1(0).

The Request Next Character signal (ML64-18) is an input which goes to VH when the printer timing logic is ready to accept more information. Otherwise it remains at VIL.

The Load Data Printer signal (ML64-9) drives momentarily (>2 microseconds) to VH when information is to be transferred (via data leads) to the printer timing logic. The trailing edge of this pulse causes Request Next Character to be set to VIL.

Right Hand Margin is a bi-directional signal which, during normal operation, is an input to MACON (ML64-19). This signal goes to VH coincident with Request Next Character whenever the print mechanism is at the right hand margin. This signal is driven to VH by MACON (ML64) whenever the power is turned on with the interlock switch (J107 pin 16) open and the TEST SWITCH not activated. It remains at VH until the interlock switch is depressed.

3.1.4 The TAU/TEU interface is comprised of six lines from the MACON (ML64) pack.

Two control lines provide the normal interface control to the line interface. Terminal Ready (ML64-3) is active when driven to VH by MACON. TAU/TEU Ready (ML64-6) is active when driven to VH by ML65-4.

Two data lines provide the bi-directional asynchronous serial data path. Send Data (ML64-39) is marking (spacing) when driven to VH (VIL) by MACON. Receive data is marking (spacing) when driven to VH (VIL) by ML65-4.

Two test signals are provided for maintenance testing. Both Digital Loop (ML64-5) and Analog Loop (ML64-4) are active when driven to VH by MACON.

A seventh signal, Duplex, is provided at the TAU/TEU interface for future use. It is identical to the signal on ML64-31 except that no pullup to +5V is provided on the card.

3.1.5 Paper Out and Low Paper switches are connected to the logic card through J10L. Each switch drives a 7417 buffer (ML64-3, 5) with 6K input pullup resistors (R13, R14). The 7417 buffer drives MACON (ML64-22, 28) to VH when the corresponding switch is closed. Internal resistors in MACON pull these leads to VIL when the corresponding switch is open.
3.1.6 Three option switches (SPD4-SW1, SW3, SW8) are provided for Terminal Controller options.

When a switch is open the associated pin on MACH (ML03-23, 26, 30) is pulled to $V_{TH}$. Closing the switch applies logic ground to the corresponding MACH pin.

3.2 PS-2 Printer Timing Logic (See TC-2 and TC-3 Timing Diagrams.)

3.2.1 General - Functional Block PS-2 receives 8 bit parallel information from the Terminal Controller and in turn generates all the necessary timing to produce the corresponding printer function. This functional block also provides the system clock for the H63 Basic KSR.

3.2.2 System Clock - The clock circuit consists of a crystal controlled oscillator and a divide-by-2 squaring circuit with power-on getting.

One half of the NOR gate pack (MLE1) provides the amplifier section for a series resonant oscillator circuit with a 1.12 MHz crystal in the feedback path. The output at MLE1-2 is buffered by another NOR gate with a disabling input (MLE1-12) provided for testing purposes. In normal operation resistor R46 keeps this gate enabled.

One flip-flop of a 74109 Pack (MLD2) is connected as an RS latch (not clocked). The presence of C20 on the CLR input (MLD2-15) sets this latch (MLD2-10) at $V_{TH}$ on power turn on. Approximately 100 nsec later C20 will have charged positive enough to reach the NOR gate input threshold (MLE1 pins 4, 5), causing the latch preset (MLD2-11) to switch to $V_{TH}$ and setting MLD2-10 to $V_{TH}$ where it will remain till power is removed. This circuit prevents erratic operation of the clock line during the power-up node, when the oscillator is starting.

The second flip-flop of the 74109 pack is connected to divide the clock signal (from the oscillator) by two when the 'J' input (MLD2-2) is at $V_{TH}$. This gives a symmetric 560 KHz clock at MLD2-6 which swings from $V_{TH}$ to $V_{CC}$. Pullup resistor R36 is needed to attain this positive level. When the 'J' input is at $V_{TH}$ the flip-flop output (MLD2-6) will be set to and remain at $V_{TH}$.

3.2.3 Terminal Controller Interface - Eleven parallel data lines interface the MAPL (MC7) logic pack with the Terminal Controller (PS-1). These lines operate as described in Section 3.1.3.

3.2.4 Four option switches are provided for printer options. SPD4-SW7 and SW8 select one of three character fonts. SPD4-SW5 and SW6 select one of three line lengths.

3.2.5 Left Margin Sensor - A DC contact switch is provided on the printer head assembly which when depressed (open) allows the output of a 7417 buffer (ML94 pin 9) to be pulled to $V_{TH}$ by R12. The 7417 output transistor turns off and the MAPL Left Hand Margin signal (MC7-17) is internally pulled to $V_{TH}$ indicating that the print mechanism is at the left margin position.

3.2.6 Velocity Encoder - This circuit is comprised of an optical switch, feedback amplifier and hysteresis amplifier which produce a pulse train with repetition rates proportional to the average carriage motor rotor velocity.

The phototransistor section of the optical switch (PS-2, A1) is connected in a common collector configuration. The emitter (J103 pin 1), with load resistor R5 drives both the feedback amplifier through R6 and the hysteresis amplifier (MLA8-9).

The feedback amplifier with elements R6 and C1 serves as both a low pass filter and current amplifier capable of driving the light emitting diode of the optical switch.

As the optical switch beam is interrupted by a slotted disk mounted on the carriage motor rotor shaft, voltage pulses of approximately 600 microsec period and 1V to 3V peak-to-peak amplitude are developed at MLA8-9. This repetition rate is too fast for the feedback amplifier (with low pass filter) to respond to, so no correction is made for this signal. However all slower variations (including DC offsets due to parameter variations) are cancelled out by the action of the feedback amplifier driving the optical switch LED. Consequently the desired velocity dependent signal is present at the input of the hysteresis amplifier (MLA8-9) centered about OV.

The hysteresis amplifier, with approximately 100 mV hysteresis, amplifies this input signal, supplying a voltage dependent pulse train to the MAPL pack (MC7-18). This signal swings from $V_{TH}$ to $-5V$ to $-OV$ to $+5V$.

3.2.7 Print Mechanism Driver Interface - Nine leads from the MAPL pack (MC7-31 thru 39) supply the print commands to the nine print mechanism coil drivers. When a print command is to be given, MAPL drives the desired print level (s) to $V_{TH}$ for a pre-programmed time. (See TC-2 timing diagram.)

3.2.8 One lead from the MAPL pack (MC7-30) supplies the input to the bell driver. This lead is driven to $V_{TH}$ for the duration of time required to ring the bell.
3.2.9 Line Feed Motor Driver Interface - Four leads from the MAPL pack (ML67-26 thru 29) supply the stator timing for the four line feed motor phases. A fifth lead, the clamp switch (ML67-21), controls a variable clamp in the kickback circuit of the phase 1 coil. To energize a stator coil MAPL drives the appropriate lead to VSH. (See TG-3 Timing Diagram.)

3.2.10 Carriage Motor Driver Interface - Four leads from the MAPL pack (ML67-22 thru 25) supply the stator timing for the four carriage motor phases. To energize a stator coil MAPL drives the appropriate lead to VSH. (See TG-3 for typical stator timing during printing.)

3.3 FS-3 Print Head and Bell Drivers

3.3.1 General - Each print head drive consists of a CMOS pre-driver and Darlington power driver. The bell driver consists of a Darlington power driver only.

3.3.2 When the bell driver input (Q20-B) is driven to VSH by MAPL, the collector (Q20-C) goes to 1.5V nominal, driving approximately 175 ma through the bell coil. When MAPL releases the input, R66 pulls Q20-D to ground turning off the driver. Inductive kickback from the bell coil attempts to drive Q20-C high positive. CR25 however clamps the collector preventing it from going more positive than 43V nominal.

3.3.3 When a print level pre-driver (ML65, E7 or E8) input is driven to VSH by MAPL it in turn drives the base of its associated power driver (Q31-Q39) to VSH. The power driver then turns on to VCE = 1.5V nominal causing a current pulse in the associated print head coil. When MAPL releases the input, the pull down resistor (R27 through R35) brings the pre-driver input to VSH, causing the pre-driver to pull the associated power driver base to VSH turning off the driver. The collector voltage rise due to the inductive kick of each head coil is clamped by diodes CR16 thru CR24 to 43V nominal.

3.4 FS-4 Line Feed Motor and Carriage Motor Drivers

3.4.1 General - Each driver for both the line feed and carriage motor coils consist of a CMOS pre-driver and Darlington power driver. In addition the line feed motor circuit contains a Darlington switch across the phase 1 coil to provide hard clamping of the inductive kick during the idle condition.

3.4.2 Line Feed Motor Circuit - To energize stator coil 4 (J102-1) MAPL drives the corresponding pre-driver input (ML65-9) to VSH, which in turn drives the associated power driver base (Q1-B) to VSH. This turns on the power driver to VCE = 1.5V nominal causing current flow in the stator coil.

3.4.3 Carriage Motor Circuit - The pre-driver and driver circuits for each stator coil (J104-1, 2, 3, 4) operate as described in 3.4.2 for the line feed motor. The coils are again namer clamped as described for the line feed motor. However, the namer in this case is in parallel with resistors R8 and R9, which help the namer dissipate the kickback energy. Because of this the kick voltage will remain below the namer clamp voltage till the coil current at turn off reaches approximately .5 amp.

3.5 FS-5 Voltage Distribution

3.5.1 The power on reset circuit is intended to function during two power states: a) At VGG power up time it will provide a delayed VDD potential and will ensure that the VGG power supply has reached 4.25 ± .250V before turning VDD on. b) At VGG power interruption, VGG = 4.25 ± .250V, the circuit will turn VDD off for the duration of the interrupt and provide a delayed VDD potential only after the return of VGG = 4.25 ± .250V. The delayed VDD potential from VGG and VGG will force both MAPL and HACON into their respective POR routines.

Precision resistors RB9 and RB9 form a voltage divider which determines the value at which VGG must be before MLA4-1 will switch states. Based upon the assumption that VGG holds slightly longer or precedes VGG, the VGG trip voltage is set at 4.25 ± .250V. The power up sequence is as follows: VGG (±5V) precedes or is coincident with VGG (490V) which enables MLA4-1 to track the rising positive supply voltage, VGG, which in turn causes the emitter of Q21, VPP, to also track the rising VGG voltage (VPP = VGG-2.249VR). At such time that VGG reaches 4.25 ± .250V, the timing network of C32, CR29, and C17 continues to hold the plus input
3.5 (Continued)

(MLA8-3) positive with respect to the negative input, hence, forcing MLA8-1 and Q21 emitter (V_{EB}) to continue to track V_{SS}. Approximately 50 msec. later C17 will be charged such that the voltage across R53 (MLA8-3) will drop below that voltage on MLA8-2; at which time, MLA8-1 switches to V_{CC} + 2V (+3V) causing Q21 to saturate and thus forcing V_{DD} = V_{CC} + V_{BE} (SAT) Q21 (transistor Q21 is specified as having a V_{BE} (SAT) of 0.1V max. at I_C = 100 mA and I_B = 10 mA.) Resistor R51 sets the minimum base drive of Q21 at 10mA in the saturated mode and resistor R52 ensures V_{DD} will pull towards V_{SS} in the emitter follower mode. Diode C28 provides a rapid discharge path for C17 in order to ready the detector for future V_{SS} interrupt. Capacitor C23 protects the detector from static discharge. The power interrupt sequence is as follows: V_{CC} (+5V) holds longer than V_{SS} (+5V) which drops to 4.25 ± .250V causing MLA8-2 to go negative with respect to the plus input; MLA8-1 then switches to V_{CC} + 2V and again tracks V_{SS} as does Q21 emitter (V_{EB}) as stated earlier. This positive output step plus initial voltage on C17 is coupled to R53 adding to the voltage difference at MLA8-2 and MLA8-3; thereby causing the timing delay as stated previously if V_{SS} returns immediately. Should V_{SS} continue to drop, MLA8-1 continues to track the fault condition of V_{SS} and the detector would behave as stated earlier upon the return of V_{SS} (power up sequence).

TC-4 Timing diagram illustrates typical waveforms for the power sequences stated previously and depicts the detector parameters of interest:

1) V_{CC} must precede or be coincident with V_{SS} on powering up.
2) V_{DD} must pull-up to within 2V of V_{SS} in the lower V_{SS} power mode.
3) V_{DD} must continue to track V_{SS} for a minimum of 10 msec. after return of V_{SS}.
4) Q21 must saturate at equal to or less than 0.1 volts during normal NOS operation.
5) The trip range on V_{SS} is approximately 4.25 ± .250 volts.

3.5.2 Zener diode CR26 develops a nominal -4V from the -12V supply through limiting resistor R15.

3.5.3 The various 0.1MF capacitors are filters for the logic voltages. C4 is a high frequency bypass for the -42V.

Capacitor C3 is a filter on the -42V used to average out the pulsed energy requirements of the print mechanism.
## Circuit Description of the 410080 Console Logic Card

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|-------------|------------|--------------------|------|----------|--------------|----------|---------|
|             |            |                    | 6/11/76 |          |              |          |         |         |

TC081-1272
SECTION II - DETAILED DESCRIPTION

1. ASSOCIATED DOCUMENTS - 410080 Assembly Drawing, 4080SD Schematic Diagram.

2. THEORY OF OPERATION

2.1 Keyswitches and Sense Amplifiers (FS-1, Sheet B1)

2.1.1 Each capacitive keyswitch is connected to a single input of a Sense Amplifier MLA1, MLA6 or MLA6. The Sense Amplifier determines the logic state applied to an input by comparing the charging time of the keyswitch connected to an input to the charging time of a Reference Capacitor (C2, C10 or C15) which is connected to input 0. Charging current for the Sense Amplifiers is provided by Reference Resistor (R6, R27 or R30) connected to each Sense Amplifier's summing pin (Σ) and returned to Vpp.

2.1.2 When power is first applied to 41080 the Keyswitch Logic MLA5 initializes all Sense Amplifiers by transmitting two consecutive pulses, Master Reset (MR) and SYNC. The I/O leads are active when at Vdd. The MR and SYNC pulses, which last for one complete clock cycle, initiate Master Reset and Synchronizing functions. The Synchronizing pulse forces the Sense Amplifiers to the Reference Input (IO) to begin a scan. (Vdd ≥ Vpp-IV.)

2.1.3 The Sense Amplifiers charge their associated Reference Capacitor to measure a reference charging time. Subsequently, the Keyswitch Logic transmits Data Enable (DE) pulses which advance the Sense Amplifiers to their first keyswitch inputs and places the keyswitches under test. Each Sense Amplifier determines the state of the keyswitch by determining that the keyswitch charges faster or slower than the reference capacitor.

2.1.4 After 12 clock cycles the Keyswitch Logic transmits another Data Enable pulse. The Sense Amplifiers respond by transmitting two Data Bits (active to Vpp when 01 is at Vpp). Data Bit 1 will be active at Vdd when the keyswitch being sensed is first encountered as "depressed". Data Bit 2 will be active at Vdd as long as the keyswitch continues to be depressed. This action continues until the Sense Amplifiers have tested all inputs (21 keyswitches). The Keyswitch logic transmits a number of extra Data Enable pulses (ignored by the Sense Amplifiers) while internal logic functions are being performed. The Keyswitch Logic then re-transmits the SYNC pulse and the scan cycle repeats.

2.2 Keyswitch and Interface Logic (FS-2, Sheet B2)

2.2.1 The Keyswitch Logic (NL5) controls the operation of the Sense Amplifiers (see Section 2.1.3 and 2.1.4) and provides coded output to the interface.
2.2.2 When power is first applied to CO80, Capacitor C8 is discharged. During the time that it is charging (through R22) the Keyswitch Logic will send Master Reset and Sync pulses to the Sense Amplifiers. In addition, the Serial Send Data output will be held to Vss. After C8 has charged beyond the threshold of the Power-On-Reset Input (PORS), the Keyswitch Logic will transmit only Sync and Data Enable pulses to the Sense Amplifiers and normal operation of the CO80 can begin.

2.2.3 Once each scan the Keyswitch Logic transmits a Sync pulse to establish synchronization. After the Sync pulse and a timing interval the Keyswitch Logic transmits a serial of Data Enable pulses, one pulse per every 12 clock cycles. The Sense Amplifiers respond to each Data Enable pulse by transmitting the two data bits corresponding to their input under test. Data Bits are valid on the two consecutive O1 periods following the Data Enable pulse, when O1 is at Vgg2.

2.2.4 After all keyswitches have been tested the scanning cycle repeats. A test signal, End of Scan (RES/ALARM) is provided for use as a timing reference. DSS is active to V0 for 8.9 microseconds with a repetition rate of 4.37 milli-seconds. End of Scan is active twenty-four O1 periods after the Sync pulse.

2.2.5 When a keyswitch has been sensed as "depressed" the Keyswitch Logic will determine if it is to be sent as a character or is to modify the code of another keyswitch (i.e., if the switch is Caps Lock, Shift, Control, or Repeat). If the code is to be sent it will appear as Mark-Space data on the Serial Send Data lead. This lead (pin 6 at J1) is normally high at the high level of both Serial Send Data and Repeat Mode (RPM) is limited to Vgg2 by CR2, CR3, CR6 and CR7. The code consists of 11 bits: one start bit, 8 code bits, one parity bit and one stop bit. The low level (space) is \( \frac{1}{2} \) Vgg2. One bit time = 163 us. Output impedance for both Serial Data and RPM shall be \( \leq 5000 \) ohms in either logic state.

2.2.6 Repeat Mode (RPM) is \( \frac{1}{2} \) Vgg2 \( +5V \), as long as the Repeat key is not depressed. When the Repeat key is depressed, the RPM lead of MLA5 goes to Vgg2 and RPM (pin 7 of J1) goes to \( \frac{1}{2} \) Vgg2 \( +5V \), RPM will return to Vgg2 when the Repeat key is released. If any other keyswitch is depressed while the Repeat key is depressed, the character associated with that keyswitch will be sent once per scan (4.57 ms.).

2.2.7 Switches S0, S1, and S2 are normally open B.G.S. with latch switches. The depressed (latched) state connects the corresponding pin in J1 to Vgg2. S3 and S4 are normally open B.G.S. Contact switches. When S3 or S4 is depressed, the corresponding pin in J1 is connected to Vgg2.

2.2.8 Light Emitting Diodes (LED's) in the indicating keyswitches are controlled by their respective pins in J1. On current shall be \( > 10 \) ma but \( < 15 \) ma.

2.3 Clock Generation and Drivers (FS-3, Sheet B3)

2.3.1 The 560 KHz. clock from pin 12 of J1 is divided by 5 by MLB3. The Q output of MLB3 is a 104 duty cycle waveform with a 112 KHz. repetition rate. R22, R29, C11 and C12 delay appropriate edges of the 112 KHz signal and are recombined in MLB1 and MLB2 to produce a non-overlapping \( O1 \) and \( O2 \) pre-drive signals at pins 11 of MLB1 and MLB2. The non-overlap time is \( 3 \) usec to 1.2 usec max. for both non-overlaps.
## Circuit Notes:

### Voltage Range

- **12V**: +10.8 to 13.2
- **9V**: +9.0 to 6.8
- **12V**: -10.8 to 13.3

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### Information Notes:

201. All resistors 1/4 WATT and resistance value in Ohms, unless specified.

202. All capacitor values in Microfarad, unless specified.

### Logic Designation:

1. PLUG
2. SOCKET
3. DESIGNATES MALE TERMINAL
4. DESIGNATES FEMALE TERMINAL
5. DESIGNATES PACKAGE PIN NO.
6. DESIGNATES LOCATION ON CIRCUIT BOARD

### Ground Designation:

- **Logic Ground**
- **Frame Ground**

### Connector Information:

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### Operational Notes - 20/60 mA Current J60:

A. FOR LINE OPERATION OF 20/60 mA CURRENT, J50 AND J60 MUST BE STRAPPED TOGETHER.

B. FOR OPERATION OF AUX CURRENT, select 2.5 and 12.5 and the AUX REQUEST TO SEND A301 PIN 12 AND THE AUX REQUEST TO SEND A301 PIN 12 ARE 12.5 LEVEL (12V).

C. THE FRONT INDICATOR ON A301 PIN 12 AND THE AUX REQUEST TO SEND A301 PIN 12 ARE 12.5 LEVEL (12V).